SONY

CXA1784AS

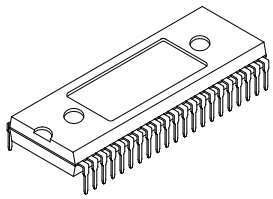
US Audio Multiplexing Decoder

For the availability of this product, please contact the sales office.

Description

The CXA1784AS is an IC designed as a decoder for the Zenith TV Multi-channel System and also corresponds with I²C BUS. Functions include stereo demodulation, SAP (Separate Audio Program) demodulation, dbx noise reduction and sound processor. Various kinds of filters are built in while adjustment, mode control and sound processor control are all executed through I²C BUS.

42 pin SDIP (Plastic)



Features

- Audio multiplexing decoder, dbx noise reduction decoder and sound processor are all included in a single chip. Almost any sort of signal processing is possible through this IC.
- All adjustments are possible through I²C BUS to allow for automatic adjustment.
- Various built-in filter circuits greatly reduce external parts.
- There are two systems for both inputs and outputs, and each mode control is possible.

Standard I/O Level

- Input level

COMPIN (Pin 17)	245 mVrms
AUXIN-L/R (Pins 38 and 37)	490 mVrms

- Output level

TVOUT-L/R (Pins 35 and 34)	490 mVrms
LSOUT-L/R (Pins 6 and 5)	490 mVrms

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	11	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	2.2	W

Range of Operating Supply Voltage

9±0.5 V

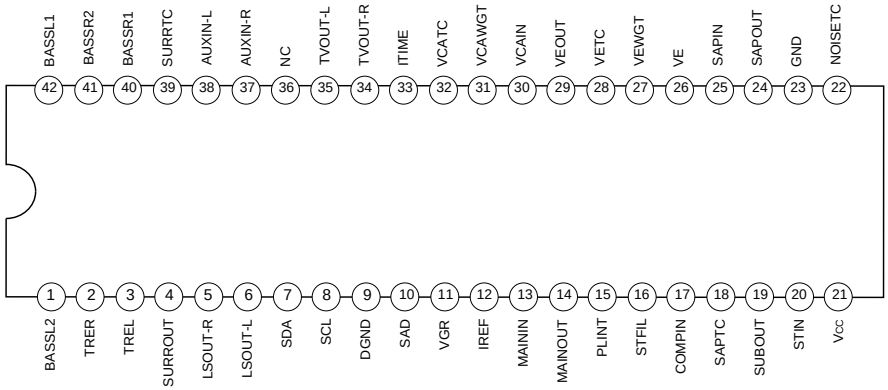
Applications

TV, VCR and other decoding systems for US audio multiplexing TV broadcasting

Structure

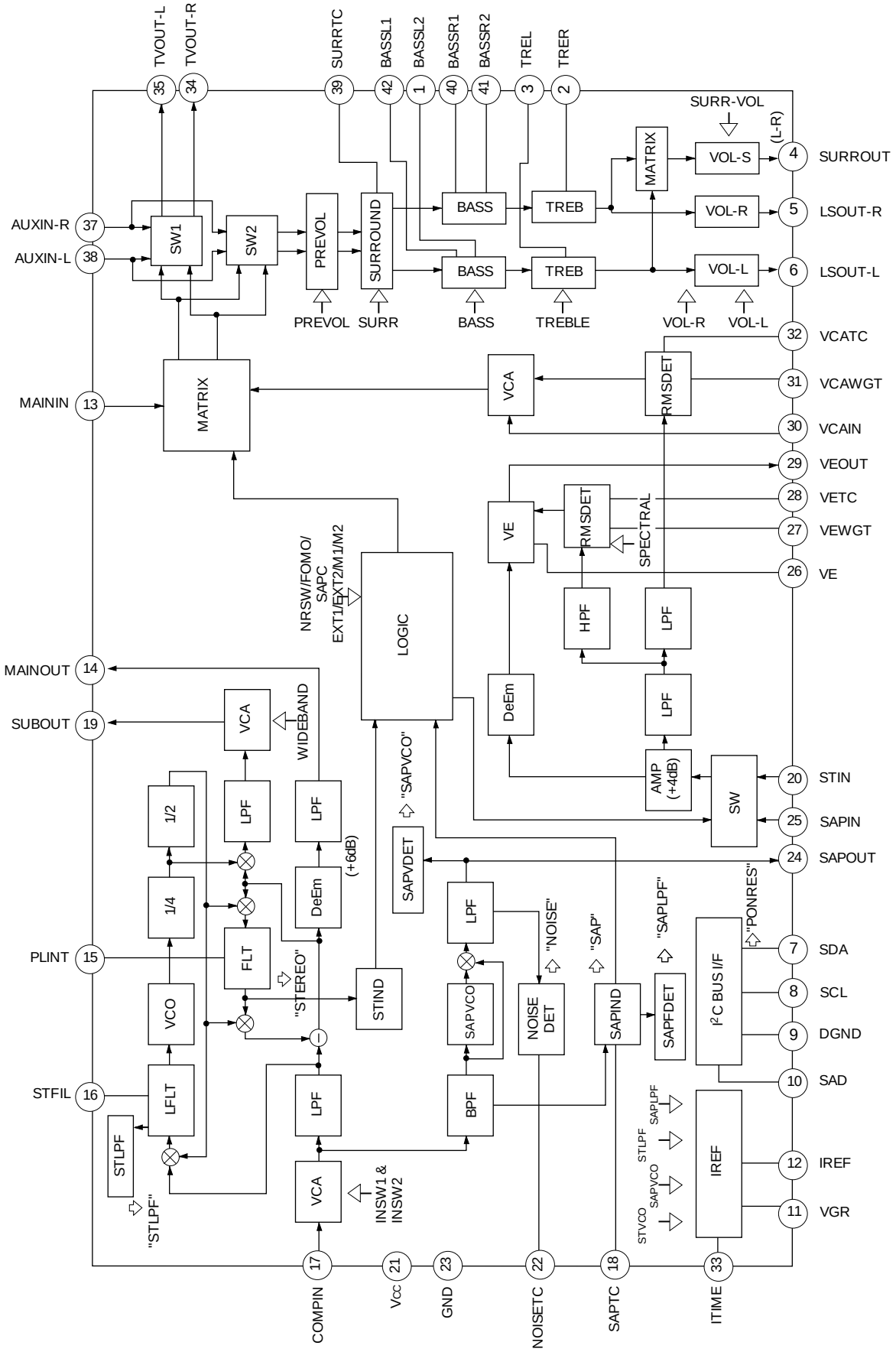
Bipolar silicon monolithic IC

Pin Configuration (Top View)

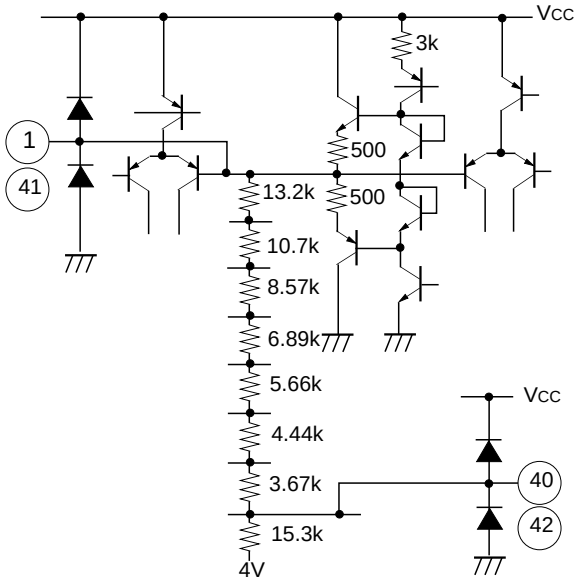
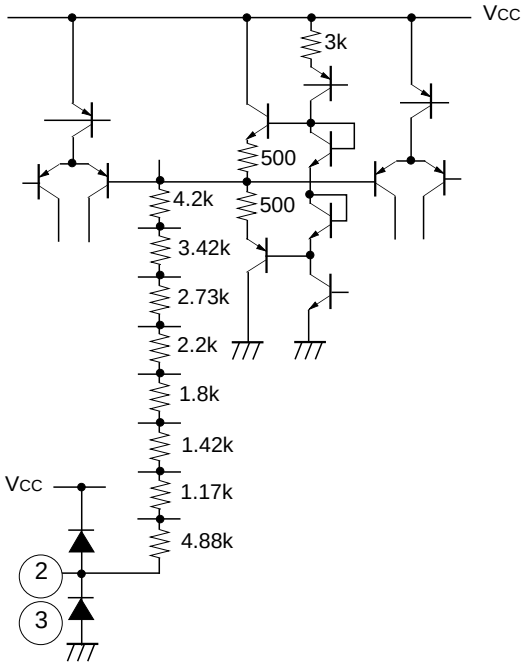
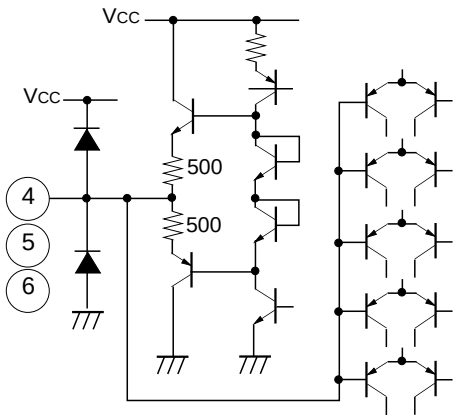


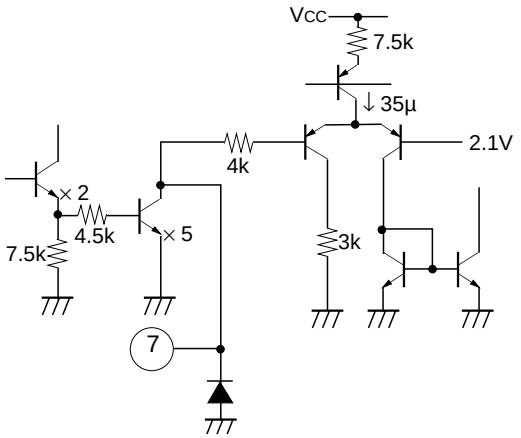
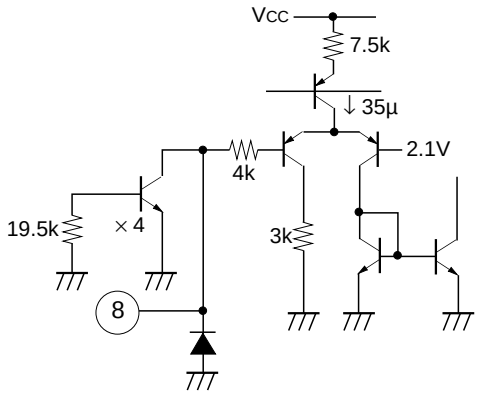
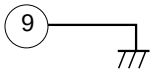
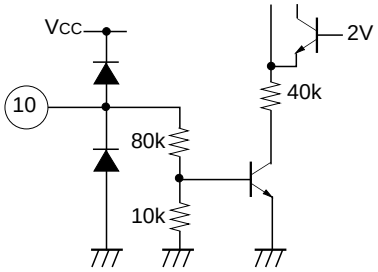
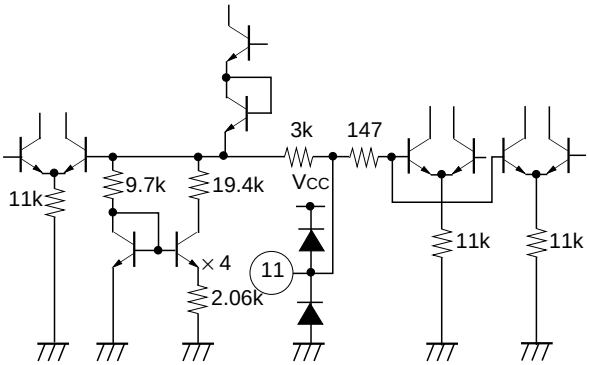
E95430A5Z-PK

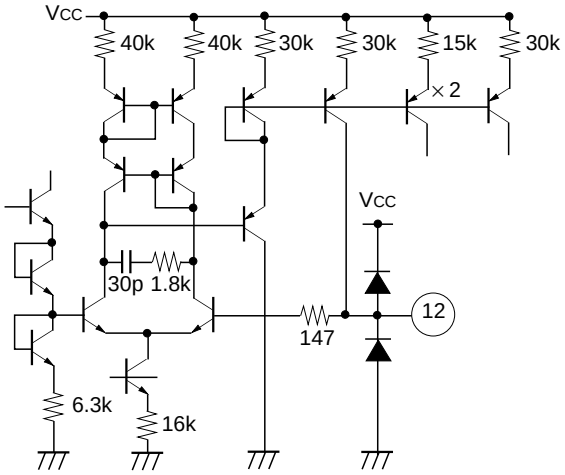
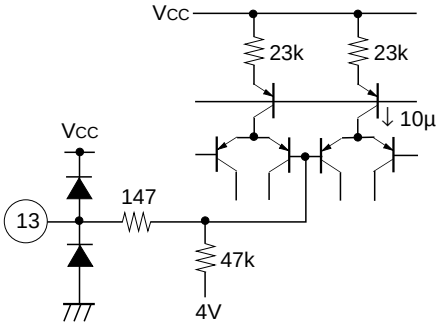
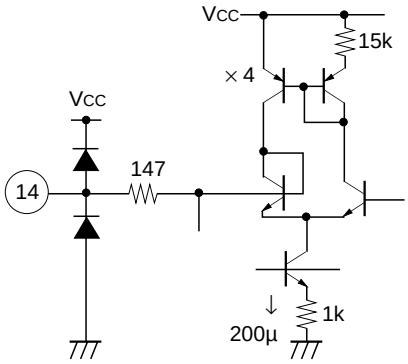
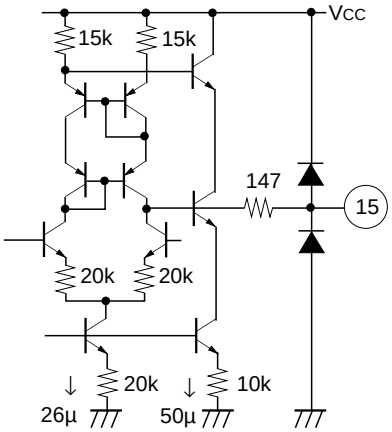
Block Diagram

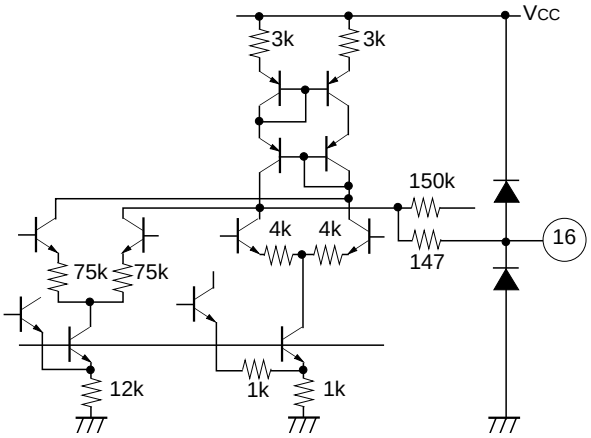
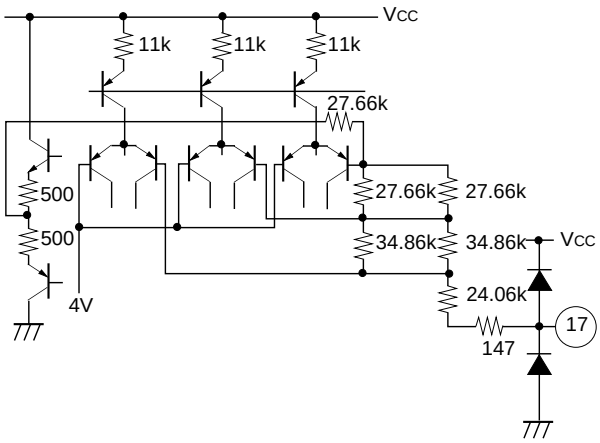
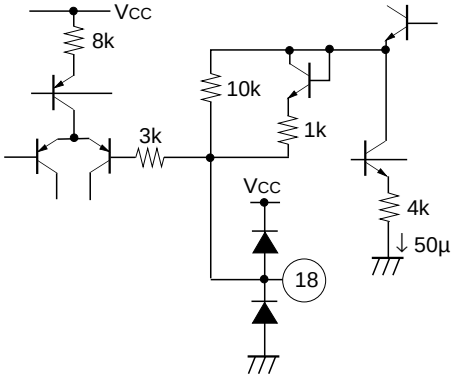
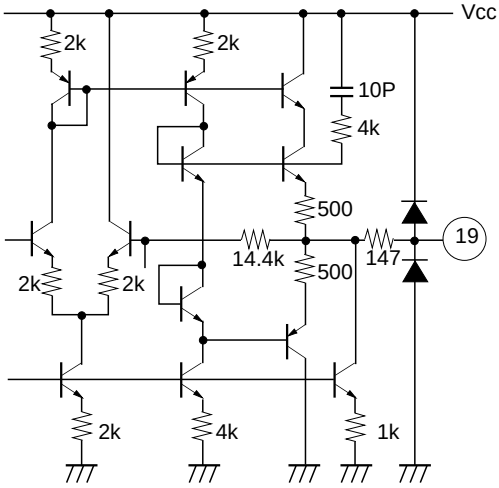


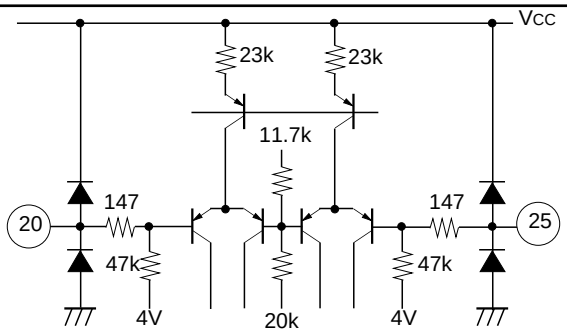
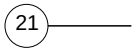
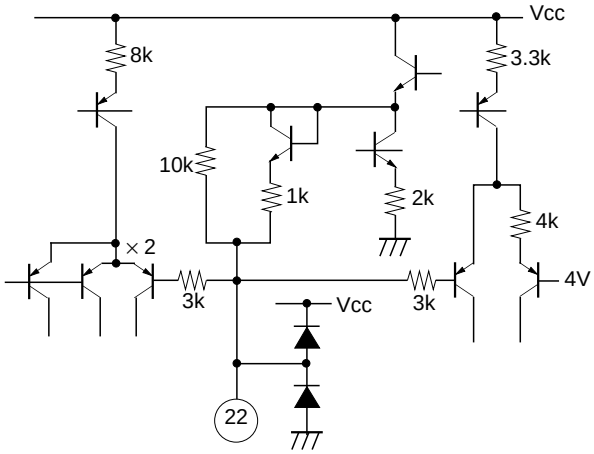
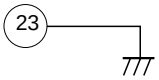
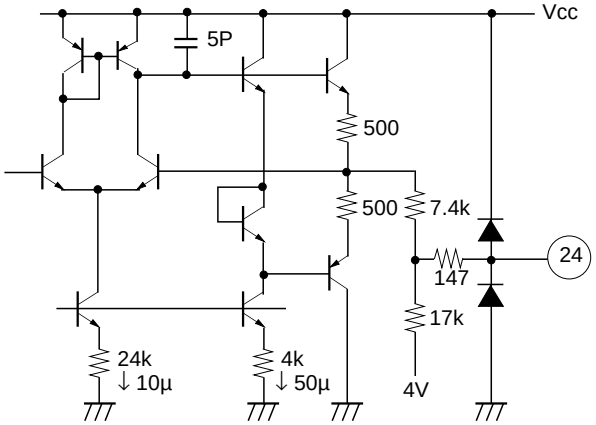
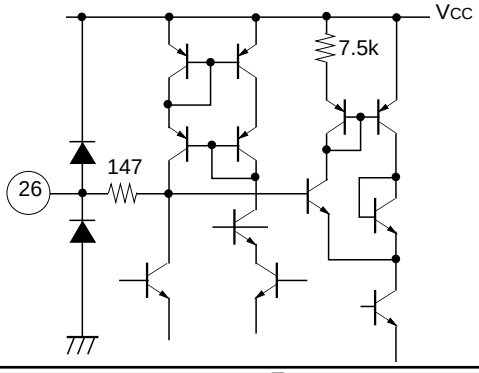
Pin Description (Ta = 25 °C, VCC = 9 V)

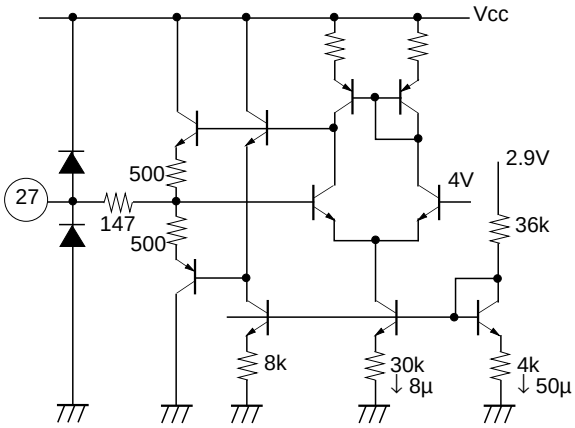
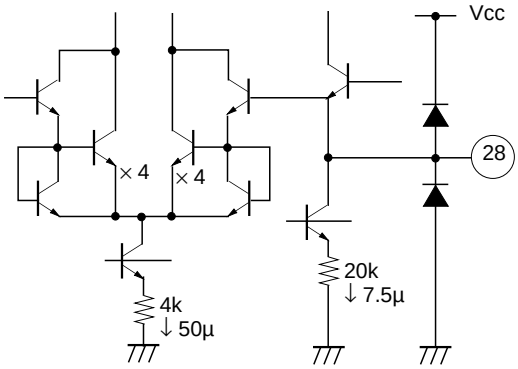
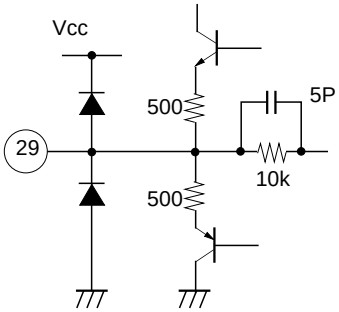
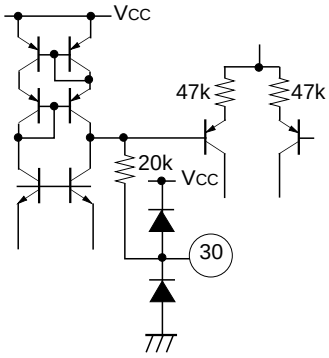
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	BASSL2	4.0		BASS filter pin. (Left channel) (Connect a 15 nF capacitor between Pins 1 and 42.) The cutoff frequency is determined by the built-in resistor and the external capacitance.
42	BASSL1	4.0		
41	BASSR2	4.0		BASS filter pin. (Right channel) (Connect a 15 nF capacitor between Pins 41 and 40.) The cutoff frequency is determined by the built-in resistor and the external capacitance.
40	BASSR1	4.0		
2	TRER	4.0		TREBLE filter pin. (Right channel) (Connect a 6.8 nF capacitor between this pin and GND.)
3	TREL	4.0		TREBLE filter pin. (Left channel) (Connect a 6.8 nF capacitor between this pin and GND.)
4	SURROUT	4.0		(L - R) signal output pin.
5	LSOUT-R	4.0		LSOUT right channel output pin.
6	LSOUT-L	4.0		LSOUT left channel output pin.

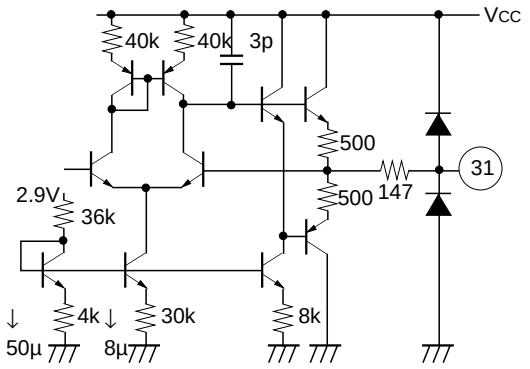
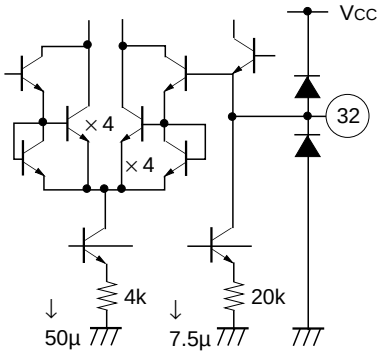
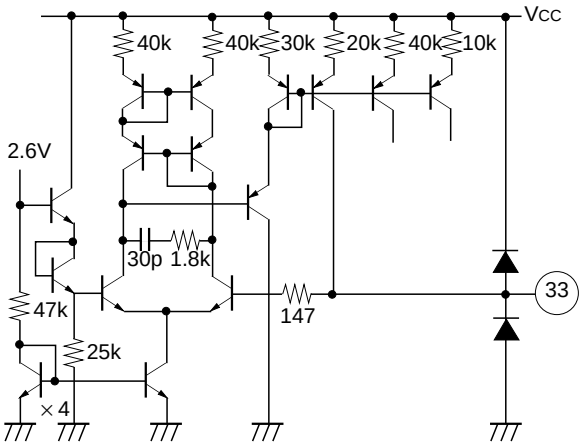
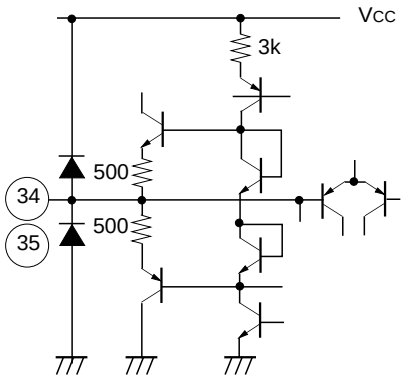
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
7	SDA	—		Serial data I/O pin. VIH > 3.0 V VIL < 1.5 V
8	SCL	—		Serial clock input pin. VIH > 3.0 V VIL < 1.5 V
9	DGND	—		Digital block GND.
10	SAD	—		Slave address control switch. The slave address is selected by changing the voltage applied to this pin.
11	VGR	1.3V		Band gap reference output pin. (Connect a 10 µF capacitor between this pin and GND.)

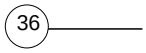
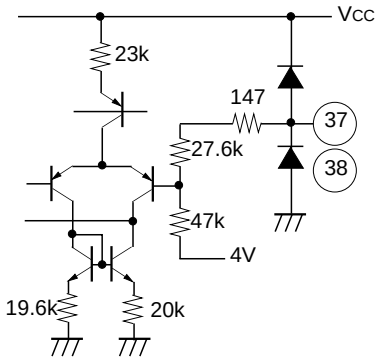
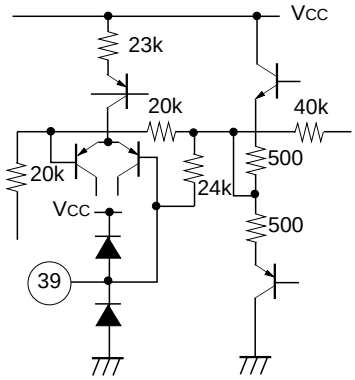
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
12	IREF	1.3V		Set the filter and VCO reference current. The reference current is adjusted with the BUS DATA based on the current which flows to this pin. (Connect a 62 kΩ (±1%) resistor between this pin and GND.)
13	MAININ	4.0V		Input the (L + R) signal from MAINOUT (Pin 14).
14	MAINOUT	4.0V		(L + R) signal output pin.
15	PLINT	6.3V		Pilot cancel circuit loop filter integrating pin. (Connect a 1 µF capacitor between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
16	STFIL	5.3V		Stereo block PLL loop filter integrating pin.
17	COMPIN	4.0V		Audio multiplexing signal input pin.
18	SAPTC	4.5V		Set the time constant for the SAP carrier detection circuit. (Connect a 4.7 µF capacitor between this pin and GND.)
19	SUBOUT	4.0V		(L - R) signal output pin.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
20	STIN	4.0V		Input the (L - R) signal from SUBOUT (Pin 19).
25	SAPIN	4.0V		Input the (SAP) signal from SAPOUT (Pin 24).
21	Vcc	—		Supply voltage pin.
22	NOISETC	3.0V		Set the time constant for the noise detection circuit. (Connect a 4.7 µF capacitor and a 200 kΩ resistor between this pin and GND.)
23	GND	—		Analog block GND.
24	SAPOUT	4.0V		SAP FM detector output pin.
26	VE	4.0V		Variable de-emphasis integrating pin. (Connect a 2700 pF capacitor and a 3.3 kΩ resistor in series between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
27	VEWGT	4.0V		Weight the variable de-emphasis control effective value detection circuit. (Connect a 0.047 µF capacitor and a 3 kΩ resistor in series between this pin and GND.)
28	VETC	1.7V		Determine the restoration time constant of the variable de-emphasis control effective value detection circuit. (The specified restoration time constant can be obtained by connecting a 3.3 µF capacitor between this pin and GND.)
29	VEOUT	4.0V		Variable de-emphasis output pin. (Connect a 4.7 µF non-polar capacitor between Pins 29 and 30.)
30	VCAIN	4.0V		VCA input pin. Input the variable de-emphasis output signal from Pin 29 via a coupling capacitor.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
31	VCAWGT	4.0V		Weight the VCA control effective value detection circuit. (Connect a 1 µF capacitor and a 3.9 kΩ resistor in series between this pin and GND.)
32	VCATC	1.7V		Determine the restoration time constant of the VCA control effective value detection circuit. (The specified restoration time constant can be obtained by connecting a 10 µF capacitor between this pin and GND.)
33	ITIME	1.3V		Set the reference current for the effective value detection timing current. The reference current is adjusted with the BUS DATA “SPECTRAL” based on the current which flows to this pin. The timing current determines the restoration time constant of the detection circuit and the variable de-emphasis characteristics. (Connect a 43 kΩ (±1%) resistor between this pin and GND.)
34	TVOUT-R	4.0V		TVOUT right channel output pin.
35	TVOUT-L			TVOUT left channel output pin.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
36	NC	—		—
37	AUXIN-R	4.0V		Right channel external input pin.
38	AUXIN-L	4.0V		Left channel external input pin.
39	SURRTC	4.0V		Set the central frequency of the SURROUND circuit phase shifter. The frequency is determined by the built-in resistor and the external capacitance. (Connect a 0.022 µF capacitor between this pin and GND.)

Electrical Characteristics

COMPIN input level
(100% modulation level)

	INSW1 = 0, = 1 INSW2 = 0, = 1	INSW1 = 1 INSW2 = 0	INSW1 = 0 INSW2 = 1
Main (L + R) (Pre-Emphasis : OFF)	= 245mVrms	= 490mVrms	= 100mVrms
SUB (L – R) (dbx-TV :OFF)	= 490mVrms	= 980mVrms	= 200mVrms
Pilot	= 49mVrms	= 98mVrms	= 20mVrms
SAP Carrier	= 147mVrms	= 294mVrms	= 60mVrms

f_H = 15.734kHz

(Ta = 25°C, Vcc = 9V)

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
1	Current consumption	Icc			No signal				35	44	53	mA
2	Main output level	Vmain	MONO	17	Mono 1kHz 100% mod. Pre-em. on			34/35	440	490	540	mVrms
3	Main de-emphasis frequency characteristic	FCdeem	MONO	17	Mono 5kHz 30% mod. Pre-em. on	20 log ('5k'/'1k')		34/35	-1.2	0	1.0	dB
4	Main LPF frequency characteristic	FCmain	MONO	17	Mono 12kHz 30% mod. Pre-em.on	20 log ('12k'/'1k')		34/35	-3.0	-1.0	1.0	
5	Main distortion	THDm	MONO	17	Mono 1kHz 100% mod. Pre-em. on		15kLPF	34/35	—	0.1	0.5	%
6	Main overload distortion	THDmmax	MONO	17	Mono 1kHz 200% mod. Pre-em off		15kLPF	34/35	—	0.15	0.5	
7	Main S/N	SNmain	MONO	17	Mono 1kHz, Pre-em on	20 log ('100%'/'0%')	15kLPF	34/35	61	69	—	dB
8	Sub output level	Vsub	ST	17	SUB (L-R), 1kHz, 100% mod., NR OFF			19	150	190	230	mVrms
9	Sub LPF frequency characteristic	FCsub	ST	17	SUB (L-R) 12kHz, 30% mod., NR OFF	20 log ('12k'/'1k')		19	-3.0	-0.5	1.0	dB
10	Sub distortion	THDsub	ST	17	SUB (L-R) 1kHz, 100% mod., NR OFF		15kLPF	19	—	0.1	1.0	%
11	Sub overload distortion	THDsmax	ST	17	SUB (L-R), 1kHz, 200% mod., NR OFF		15kLPF	19	—	0.2	2.0	
12	Sub S/N	SNsub	ST	17	SUB (L-R) 1kHz, NR OFF	20 log ('100%'/'0%')	15kLPF	19	56	64	—	dB
13	Sub pilot leak	PCsub	ST	17	PILOT (f_H) 0dB	20 log ('out'/'in')	f_H BPF	19	—	-30	-22	dB
14	Stereo ON level	THst	ST	17	Change PILOT (f_H) Level	0dB=49mVrms		BUS RETURN	-9.0	-6.0	-3.0	dB
15	Stereo ON/OFF hysteresis	HYst				20 log ('on level'/'off level')			2.0	4.0	8.0	

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
16	SAP output level	Vsap1	SAP	17	SAP 1kHz 100% mod. NR OFF			24	150	190	230	mVrms
17		Vsap2			SAP 1kHz 100% mod. NR ON			34/35	370	490	610	
18	SAP LPF frequency characteristic	FCsap	SAP	17	SAP 10kHz, 30% mod. NR OFF	20 log ('10k'/'1k')		24	-3.0	0	2.5	dB
19	SAP distortion	THDsap1	SAP	17	SAP 1kHz 100% mod. NR OFF		15kLPF	24	—	2.5	6.0	%
20		THDsap2			SAP 1kHz 100% mod. NR ON		15kLPF	34/35	—	0.6	1.5	
21	SAP S/N	SNsap	SAP	17	SAP 1kHz, NR OFF	20 log ('100%'/'0%')	15kLPF	24	46	55	—	dB
22	SAP soft mute	Smute	SAP	17	SAP 1kHz, 100% mod. NR OFF			24	-8.5	-7.0	-5.5	
23	dbx out noise level	Ndbx	SAP		No signal		15kLPF	34/35	—	-75	-54	dBm
24	SAP ON level	THsap	SAP	17	Change	0dB=147mVrms		BUS RETURN	-12.0	-9.0	-6.0	dB
25	SAP ON/OFF hysteresis	HYsap			SAP Carrier ($5f_H$) Level	20 log('on level'/'off level')			2.0	4.0	6.0	
26	ST separation 1 L → R	STLsep1	ST	17	ST-L 300Hz 30% mod. NR ON		15kLPF	34/35	23	35	—	
27	ST separation 1 R → L	STRsep1	ST	17	ST-R 300Hz 30% mod. NR ON		15kLPF	34/35	23	35	—	
28	ST separation 2 L → R	STLsep2	ST	17	ST-L 3kHz 30% mod. NR ON		15kLPF	34/35	23	35	—	
29	ST separation 2 R → L	STRsep2	ST	17	ST-R 3kHz 30% mod. NR ON		15kLPF	34/35	23	35	—	
30	TVOUT output level	Vtv	EXT	37/38	Sine wave 1kHz, 490mVrms	0dB=490mVrms		34/35	-0.5	0	0.5	
31	TVOUT cross talk	CTtv1	INT	37/38	Sine wave 1kHz, 490mVrms	0dB=490mVrms EXT → INT	1kBPF	34/35	—	-75	-59	
		CTtv2	EXT	17	MONO 1kHz, 100%, Pre-em. on	0dB=490mVrms INT → EXT						
32	TVOUT muted amount	MUtv1	INT	17	MONO 1kHz, 100%, Pre-em. on	20 log (M1="0"/M1="1")	1kBPF	34/35	—	-75	-70	
33		MUtv2	EXT	37/38	Sine wave 1kHz, 490mVrms	20 log (M1="0"/M1="1")			—	-80	-70	

No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
34	TVOUT DC offset	OStv	INT EXT	—	No signal	Mute (M1=0)/DC difference when there is no signal		34/35	-25	0	25	mV
35	TVOUT distortion	THDtv	EXT	37/38	Sine wave 1kHz, 490mVrms		15kLPF	34/35	—	0.01	0.5	%
36	TVOUT S/N	SNtv	EXT	37/38	Sine wave 1kHz, 490mVrms/No signal	20 log ('490mVrms'/'No signal')	15kLPF	34/35	74	77	—	dB
37	TVOUT overload distortion	THDtvmax	EXT	37/38	Sine wave 1kHz, 2Vrms		15kLPF	34/35	—	0.1	1.0	%
38	LSOUT output level	Vls1	INT	17	MONO 1kHz 100%, Pre-em. on	0dB=490mVrms		5/6	-0.9	0	0.9	dB
		Vls2	EXT	37/38	Sine wave 1kHz, 490mVrms	0dB=490mVrms						
39	LSOUT cross talk	CTls1	INT	37/38	Sine wave 1kHz, 490mVrms	0dB=490mVrms EXT → INT	1kBPF	5/6	—	-75	-59	
		CTls2	EXT	17	MONO 1kHz 100%, Pre-em. on	0dB=490mVrms INT → EXT						
40	LSOUT muted amount	MUls	EXT	37/38	Sine wave 1kHz, 490mVrms	20 log (M2="0"/M2="1")	1kBPF	5/6	—	-80	-70	
41	LSOUT DC offset	OSls	INT EXT	—	No signal	Mute (M2=0)/DC difference when there is no signal		5/6	-25	0	25	mV
42	LSOUT distortion	THDls	EXT	37/38	Sine wave 1kHz, 490mVrms		15kLPF	5/6	—	0.01	0.5	%
43	LSOUT S/N	SNls	EXT	37/38	Sine wave 1kHz, 490mVrms	20 lgo ('490mVrms'/'No signal')	15kLPF	5/6	74	77	—	dB
44	LSOUT overload distortion	THDlsmax	EXT	37/38	Sine wave 1kHz, 2Vrms		15kLPF	5/6	—	0.1	1.0	%
45	BASS maximum value	TBmax	EXT	37/38	Sine wave 100Hz, 245mVrms	BASS="F" 0dB=245mVrms		5/6	11	12	13	dB
46	BASS minimum value	TBmin	EXT	37/38	Sine wave 100Hz, 245mVrms	BASS="0" 0dB=245mVrms		5/6	-13	-12	-11	
47	TREBLE maximum value	TTmax	EXT	37/38	Sine wave 10kHz, 245mVrms	TREBLE="F" 0dB=245mVrms		5/6	11	12	13	
48	TREBLE minimum value	TTmin	EXT	37/38	Sine wave 10kHz, 245mVrms	TREBLE="0" 0dB=245mVrms		5/6	-13	-12	-11	
49	Volume minimum value	VOLmin	EXT	37/38	Sine wave 1kHz, 490mVrms	VOL-L="0", VOL-R="0" 0dB=490mVrms	1kBPF	5/6	—	-80	-70	
50	SURROUT volume minimum value	SVOLmin	EXT	37/38	Sine wave 1kHz, 490mVrms	VOL-SURR="0" 0dB=490mVrms	1kBPF	4	—	-80	-70	

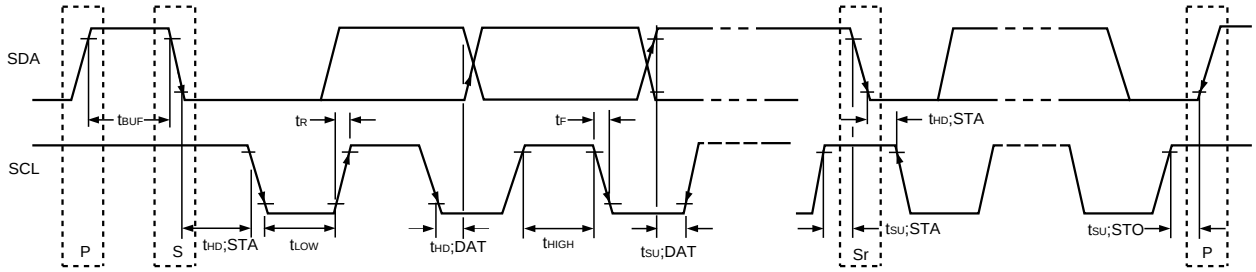
No.	Item	Symbol	Mode	Input pin	Input signal	Measurement conditions	Filter	Output pin	Min.	Typ.	Max.	Unit
51	SURROUND frequency characteristic 1	Sr1	EXT	38	Sine wave 330Hz, 490mVrms	SURR="1" 0dB=490mVrms		6	1.5	3.0	4.6	dB
52	SURROUND frequency characteristic 2	Sr2	EXT	38	Sine wave 10kHz, 490mVrms	SURR="1" 0dB=490mVrms		6	4.5	6.0	7.5	

I²C BUS block items (SDA, SCL)

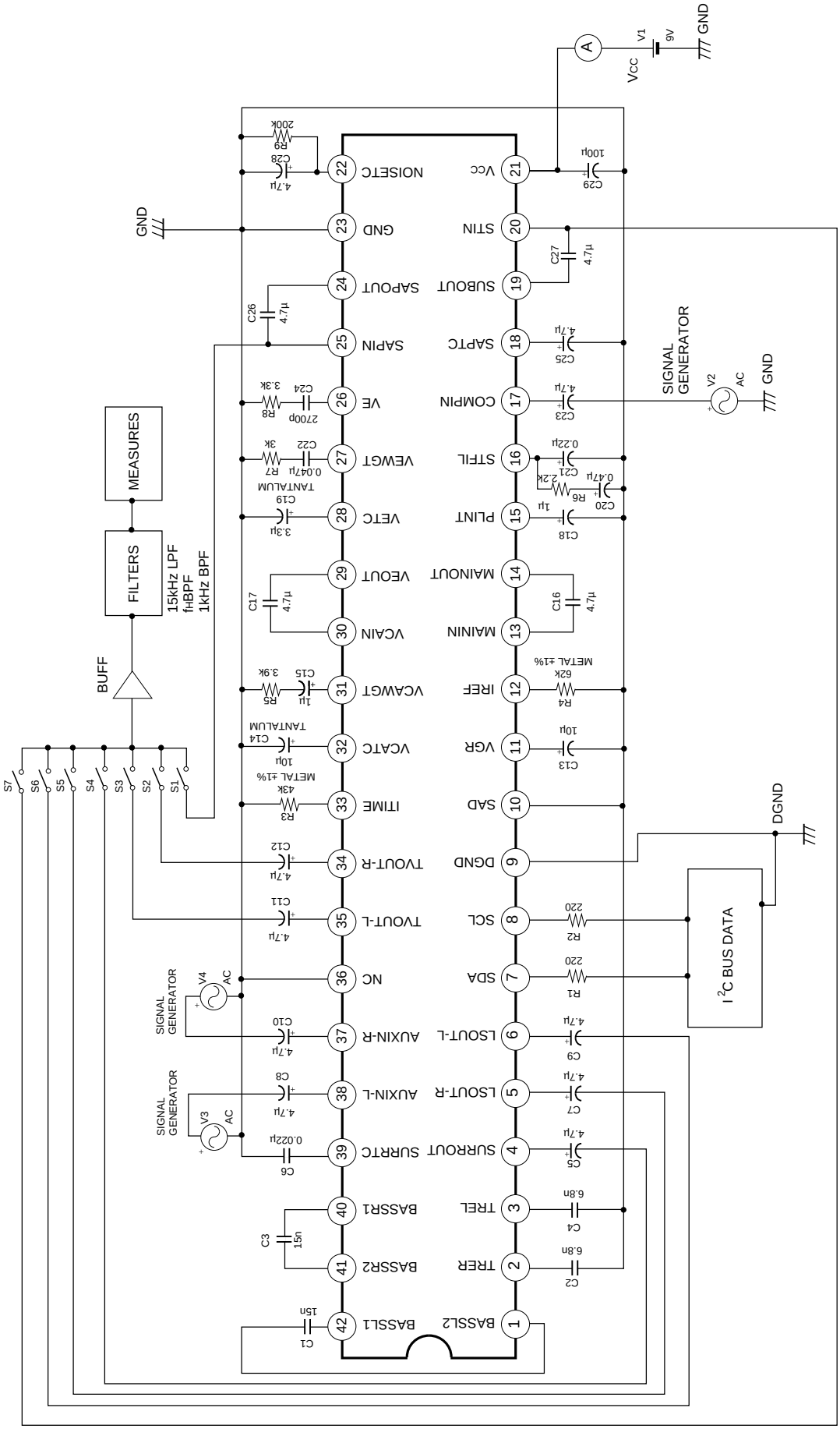
No.	Item	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	V_{IH}	3.0	—	5.0	V
2	Low level input voltage	V_{IL}	0	—	1.5	
3	High level input current	I_{IH}	—	—	10	µA
4	Low level input current	I_{IL}	—	—	10	
5	Low level output voltage SDA (Pin 7) during 3 mA inflow	V_{OL}	0	—	0.4	V
6	Maximum inflow current	I_{OL}	3	—	—	mA
7	Input capacitance	C_I	—	—	10	pF
8	Maximum clock frequency	f_{SCL}	0	—	100	kHz
9	Minimum waiting time for data change	t_{BUF}	4.7	—	—	µs
10	Minimum waiting time for start of data transfer	t_{HD}:STA	4.0	—	—	
11	Low level clock pulse width	t_{LOW}	4.7	—	—	
12	High level clock pulse width	t_{HIGH}	4.0	—	—	
13	Minimum waiting time for start preparation	t_{SU}:STA	4.7	—	—	
14	Minimum data hold time	t_{HD}:DAT	0	—	—	
15	Minimum data preparation time	t_{SU}:DAT	250	—	—	ns
16	Rise time	t_R	—	—	1	µs
17	Fall time	t_F	—	—	300	ns
18	Minimum waiting time for stop preparation	t_{SU}:STO	4.7	—	—	µs

I²C BUS load conditions: Pull-up resistor 4 kΩ (Connect to +5 V)
Load capacity 200 pF (Connect to GND)

I²C BUS Control Signal



Electrical Characteristics Measurement Circuit



I²C BUS Register Data Standard Setting Values

Register	Number of bits	Classifi-cation	Standard setting	Contents	Setting value when electrical characteristics are measured
ATT	4	A	9	Center point	Adjustment point
STVCO	6	A	1F		
SAPVCO	4	A	8		
SAPLPF	4	A	8		
STLPF	6	A	1F		
SPECTRAL	6	A	1F		
WIDEBAND	6	A	1F		
TEST-DA	1	T	0	Normal mode	Standard setting value
TEST1	1	T	0		
PRE-VOL	4	U	F	F=0dB	
VOL-L	6	U	3F	3F=0dB	
VOL-R	6	U	3F	3F=0dB	
VOL-SURR	6	U	3F	3F=0dB	
TREBLE	4	U	8	7 or 8=0dB	
BASS	4	U	8	7 or 8=0dB	
SURR	1	U	0	Surround OFF	
NRSW	1	U	—	According to the modecontrol table	
FOMO	1	U	—		
EXT1	1	U	0	TV decoder output selection	Standard setting value
EXT2	1	U	0		
EXTFOMO	1	U	0	External forced MONO OFF	Standard setting value
M1	1	U	1	Mute OFF	
M2	1	U	1		
INSW1	1	S	—	Fixed by the set specifications	Standard setting value
INSW2	1	S	—		
SAPC	1	S	—		

Classification A: Adjustment
U: User control
S: Proper to set
T: Test

List of Adjustment Contents

	Adjustment item	Adjustment data	Input pin	*Input signal data	Measurement	Adjustment contents	Test mode setting
1	MAIN VCA	ATT	COMPIN (Pin 17)	100Hz 245mVrms	TVOUT-L output level	Adjust as close to 490 mVrms as possible	
2	ST VCO	STVCO	None	None	TVOUT-R output frequency	Adjust as close to 62.936 kHz as possible	TEST-DA=1
3	SAP VCO	SAPVCO	COMPIN (Pin 17)	$5f_H$ (78.67k) 147mVrms	STA7 (SAPVCO1) STA8 (SAPVCO2)	Adjust to the center of the SAPVCO1 = 0, SAPVCO2 = 1 condition	
4	ST & dbx FILTER	STLPF	COMPIN (Pin 17)	9.4kHz 600mVrms	STA3 (STLPF)	Adjust to the center of the STLPF = 1 condition	TEST1=1
5	SAP FILTER	SAPLPF	COMPIN (Pin 17)	88kHz 110mVrms	STA4 (SAPLPF)	Adjust to the center of the SAPLPF = 1 condition	TEST1=1
6	Low frequency ST separation	WIDEBAND	COMPIN (Pin 17)	ST-L 30% 300Hz	TVOUT-R output level	Minimize the output level	
	High frequency ST separation	SPECTRAL	COMPIN (Pin 17)	ST-L 30% 3kHz	TVOUT-R output level	Minimize the output level	

* This is the case when standard input level is 245mVrms. When this level is 100mVrms or 490mVrms, input signal during adjustment is varied according to the ratio of these level.

Adjustment Method (Input signal level is the case when standard input signal level is 245mVrms)

1 ATT adjustment

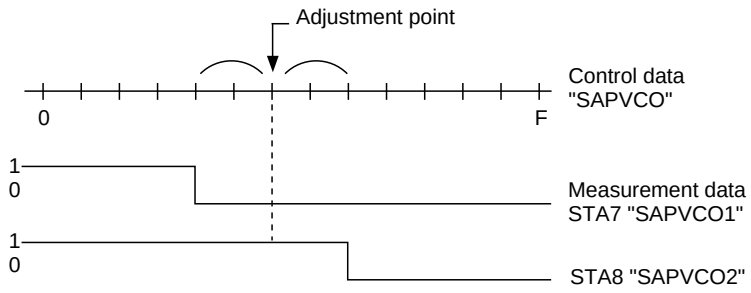
1. TEST BIT is set to “TEST1 = 0” and “TEST-DA = 0”.
2. Input a 100 Hz, 245 mVrms sine wave signal to COMPIN and monitor the TVOUT-L output level. Then, adjust the “ATT” data for ATT adjustment so that the TVOUT-L output goes to the standard value.
3. Adjustment range: ±30%
   Adjustment bits: 4 bits

2 Stereo VCO adjustment

1. TEST BIT is set to “TEST1 = 0” and “TEST-DA = 1”.
2. Monitor the TVOUT-R output ($4f_H$ free running) frequency in a no input state, and adjust “STVCO” adjustment data so that this frequency is as close to $4f_H$ (62.936 kHz) as possible.
3. Adjustment range: ±20%
   Adjustment bits: 6 bits

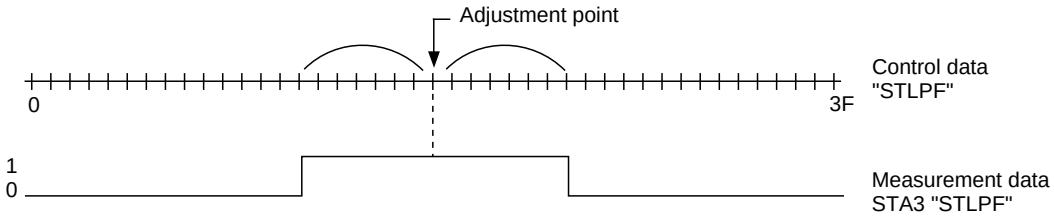
3 SAPVCO adjustment

1. TEST BIT is set to “TEST1 = 0” and “TEST-DA = 0”.
2. Input a $5f_H$ (SAP carrier , 78.67 kHz) , 147 mVrms sine wave signal to COMPIN. While monitoring the STATUS FLAG (STA7, STA8) condition, adjust “SAPVCO” adjustment data.
3. Adjustment range: ±20%
   Adjustment bits: 4 bits
   Align SAPVCO with the center of the STA7 = 0 and STA8 = 1 (adjustment OK) condition range.



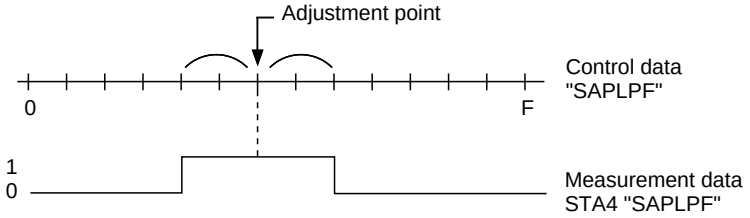
4 Stereo block dbx filter adjustment

1. TEST BIT is set to “TEST1 = 1” and “TEST-DA = 0”.
2. Input a 9.4 kHz, 600 mVrms sine wave signal to COMPIN. While monitoring the STATUS FLAG (STA3) condition, adjust the “STLPF” adjustment data.
3. Adjustment range: ±20%
   Adjustment bits: 6 bits
   Align STLPF with the center of the STA3 = 1 (adjustment OK) condition range.



5 SAP block filter adjustment

1. TEST BIT is set to “TEST1 = 1” and “TEST-DA = 0”.
2. Input a 88 kHz, 110 mVrms sine wave signal to COMPIN. While monitoring the STATUS FLAG (STA4) condition, vary and adjust the “SAPLPF” adjustment data.
3. Adjustment range: ±20%
   Adjustment bits: 4 bits
   Align SAPLPF with the center of the STA4 = 1 (adjustment OK) condition range.



6 Separation adjustment

1. TEST BIT is set to “TEST1 = 0” and “TEST-DA = 0”.
2. Set the unit to stereo mode and input the left channel only signal (modulation factor 30%, frequency 300 Hz NR-ON) to COMPIN. At this time, adjust the “WIDEBAND” adjustment data to reduce TVOUT-R output to the minimum.
3. Next, set the frequency only of the input signal to 3 kHz and adjust the “SPECTRAL” adjustment data to reduce TVOUT-R output to the minimum.
4. Then, the adjustments in 2 and 3 above are performed to optimize the separation.
5. “WIDEBAND” “SPECTRAL”
   Adjustment range: ±30% Adjustment range: ±15%
   Adjustment bits: 6 bits Adjustment bits: 6 bits

Description of Operation

The US audio multiplexing system possesses the base band spectrum shown in Fig. 1.

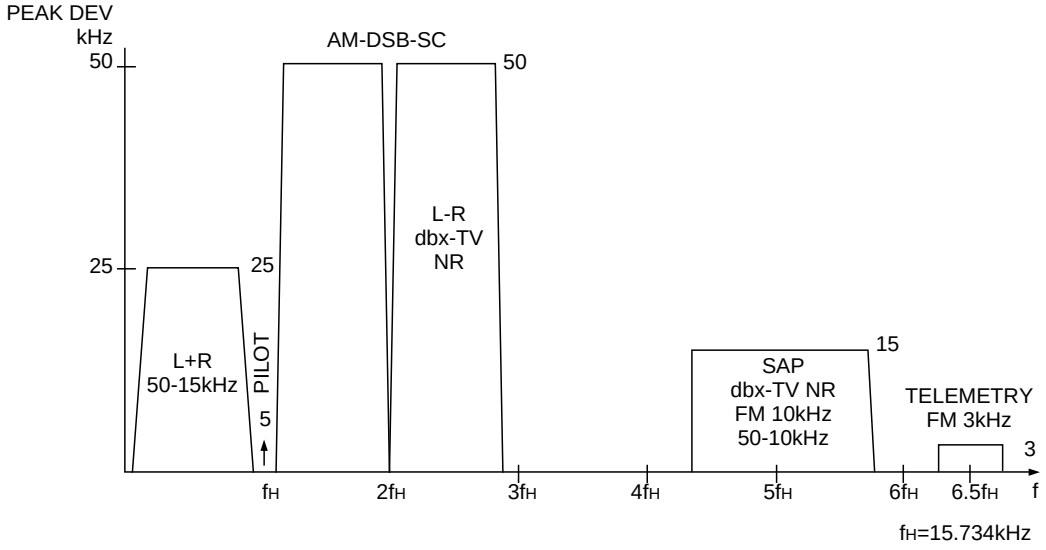


Fig. 1. Base band spectrum

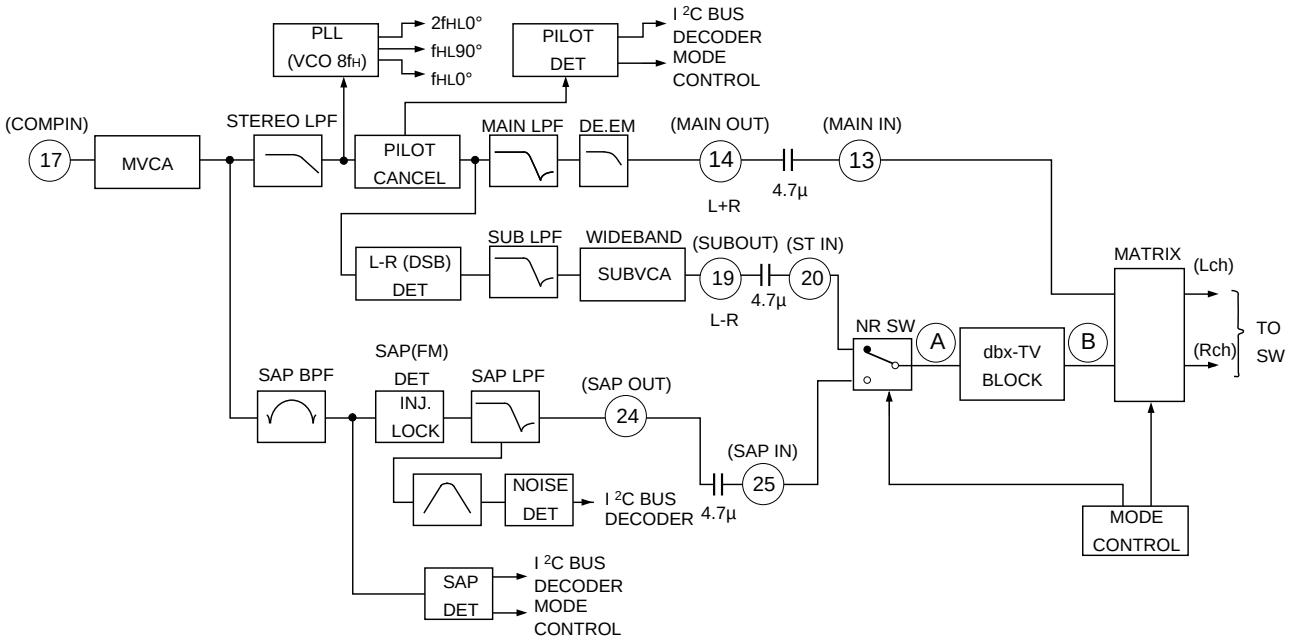


Fig. 2. Overall block diagram (See Fig. 3 for the dbx-TV block)

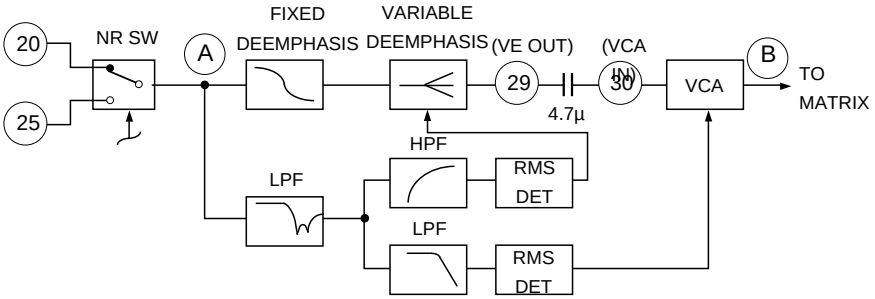


Fig 3. dbx-TV block

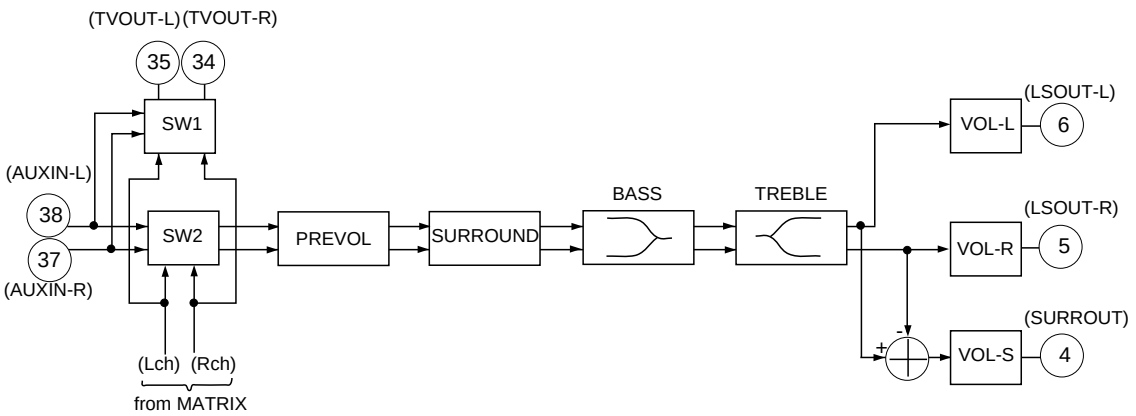


Fig. 4. Sound processor block

(1) L + R (MAIN)

After the audio multiplexing signal input from COMPIN (Pin 17) passes through MVCA, the SAP signal and telemetry signal are suppressed by STEREO LPF. Next, the pilot signals are canceled. Finally, the L - R signal and SAP signal are removed by MAIN LPF, and frequency characteristics are flattened (de-emphasized) and input to the matrix.

(2) L - R (SUB)

The L - R signal follows the same course as L + R before the pilot signal is canceled. L - R has no carrier signal, as it is a suppressed-carrier double-sideband amplitude modulated signal (DSB-AM modulated). For this reason, the pilot signal is used to regenerate the carrier signal (quasi-sine wave) to be used for the demodulation of the L - R signal. In the last stage, the residual high frequency components are removed by SUB LPF and the L - R signal is input to the dbx-TV block via the NRSW circuit after passing through SUBVCA.

(3) SAP

SAP is an FM signal using $5f_H$ as a carrier as shown in the Fig. 1. First, the SAP signal only is extracted using SAP BPF. Then, this is subjected to FM detection. Finally, residual high frequency components are removed and frequency characteristics flattened using SAP LPF, and the SAP signal is input to the dbx-TV block via the NRSW circuit. When there is no SAP signal, the Pin 24 output is soft muted.

(4) Mode discrimination

Stereo discrimination is performed by detecting the pilot signal amplitude. SAP discrimination is performed by detecting the $5f_H$ carrier amplitude. NOISE discrimination is performed by detecting the noise near 25 kHz after FM detection of SAP signal.

(5) dbx-TV block

Either the SAP signal or L - R signal input respectively from ST IN (Pin 20) or SAP IN (Pin 25) is selected by the mode control and input to the dbx-TV block.

The input signal then passes through the fixed de-emphasis circuit and is applied to the variable de-emphasis circuit. The signal output from the variable de-emphasis circuit passes through an external capacitor and is applied to VCA (voltage control amplifier). Finally, the VCA output is converted from a current to a voltage using an operational amplifier and then input to the matrix.

The variable de-emphasis circuit transmittance and VCA gain are respectively controlled by Each of effective value detection circuits. Each of the effective value detection circuits passes the input signal through a predetermined filter for weighting before the effective value of the weighted signal is detected to provide the control signal.

(6) Matrix, SW1, SW2

The signals (L + R, L - R, SAP) input to “MATRIX” become the outputs for the ST-L, ST-R, MONO and SAP signals according to the BUS data and whether there is ST/SAP discrimination.

“SW1” and “SW2” switch the “MATRIX” output signal, external input signal (input to AUXIN-L, R (Pins 38 and 37)) and external forced MONO.

Signals selected by “SW1” are output to TVOUT.

Signals selected by “SW2” pass through the sound processor and are output to LSOUT.

(7) Sound processor block

The sound processor block contains “PREVOL”, “BASS/TREBLE” tone control functions, “SURROUND” (quasi-surround function) and “VOLUME”.

BASS: ±12 dB (±1.7 dB/STEP at 100 Hz)
TREBLE: ±12 dB (±1.7 dB/STEP at 10 kHz)
VOLUME: 0 to -80 dB (-1.25 dB/STEP)

“PREVOL” controls the input signal level of the sound processor block. When turning on the bass boost, treble boost or surround, attenuate the input signal to the sound processor block using “PREVOL” so that the signal is not dissipated inside the processor.

PREVOL: 0 to -13.75 dB (-1.25 dB/STEP)

(8) Surround

At “SURROUND”, the L and R differential components are phase-shifted and these components are added to the left and right channels.

When surround is OFF (SURR = 0)

Inputs are output as is.

$$\begin{cases} Lout = Lin \\ Rout = Rin \end{cases}$$

When surround is ON (SURR = 1)

$$\begin{cases} Lout = Lin - \dfrac{1-j\omega RC}{1+j\omega RC}(Lin-Rin) \\ Rout = Rin + \dfrac{1-j\omega RC}{1+j\omega RC}(Lin-Rin) \end{cases}$$

$$\begin{cases} R = 24\ k\Omega \text{ (IC on-chip)} \\ C = 0.022\ \mu F \text{ (Externally attached to Pin 39)} \end{cases}$$

(Lin, Lout) and (Rin, Rout) indicate the left- and right- channel I/O of the surround circuit.

(9) Others

"MVCA" is a VCA which adjusts the input signal level to the standard level of this IC.
Standard input level can be selected by INSW1 or INSW2.
"Bias" supplies the reference voltage and reference current to the other blocks. The current flowing to the resistor connecting IREF (Pin 12) and ITIME (Pin 33) with GND become the reference current.

Standard input and output levels

Input pin	INSW1	INSW2	Input level	TVOUT output level	LSOUT output level*3
COMPIN	0	0	245mVrms*1	490mVrms*2	490mVrms*2
	1	1			
	1	0	490mVrms*1		
	0	1	100mVrms*1		
AUXIN	—	—	490mVrms	490mVrms	490mVrms

*1 MONO, 25kHz Deviation, Pre-Em. off
*2 MONO, 25kHz Deviation, Pre-Em. on
*3 VOLUME MAX, PREVOL MAX

Register Specifications

Slave address

SAD pin	SLAVE RECEIVER	SLAVE TRANSMITTER
GND	80H	81H
Vcc	8AH	8BH

Register table

SUB ADDRESS	DATA							
MSB LSB	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
****0000	INSW2	INSW1	TEST-DA	TEST1	ATT (4) INPUT LEVEL adj			
****0001	*		STVCO (6) STEREO VCO adj					
****0010	(SAPVCO (4) SAP VCO adj)				(SAPLPF (4) SAP FILTER adj)			
****0011	*		STLPF (6) ST FILTER adj					
****0100	*		SPECTRAL (6)					
****0101	*		WIDEBAND (6)					
****0110	EXTFOMO	EXT1	EXT2	M2	NRSW	FOMO	SAPC	M1
****0111	*			SURR	PR-VOL (4) Pre vol cont.			
****1000	*		VOL-L (6) Lch vol cont.					
****1001	*		VOL-R (6) Rch vol cont.					
****1010	*		VOL-SURR (6) Surr vol cont.					
****1011	*				TREBLE (4)			
****1100	*				BASS (4)			

*: Don't Care

Status Registers

When TEST1 = 0

STA1	STA2	STA3	STA4	STA5	STA6	STA7	STA8
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
POWER ON RESET	STEREO	SAP	NOISE	—	—	SAP VCO1	SAP VCO2

When TEST1 = 1

STA1	STA2	STA3	STA4	STA5	STA6	STA7	STA8
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
POWER ON RESET	STEREO	STLPF	SAPLPF	—	—	—	—

Description of Registers

Control registers

Register	Number of bits	Classification*	Contents
ATT	4	A	Input level adjustment
STVCO	6	A	STEREO VCO free running frequency adjustment
SAPVCO	4	A	SAP VCO free running frequency adjustment
SAPLPF	4	A	SAP filter adjustment
STLPF	6	A	STEREO and dbx filter adjustment
SPECTRAL	6	A	Adjustment of stereo separation (3 kHz)
WIDEBAND	6	A	Adjustment of stereo separation (300 Hz)
TEST-DA	1	T	Turn to DAC test mode and STVCO adjustment mode by means of TEST-DA = 1.
TEST1	1	T	Turn to test mode by means of TEST = 1. (Adjustment of STLPF and SAPLPF)
PRE-VOL	4	U	Input signal level control of sound processor block
VOL-L	6	U	LSOUT-L output signal level control
VOL-R	6	U	LSOUT-R output signal level control
VOL-SURR	6	U	SURROUT output signal level control
TREBLE	4	U	LSOUT output treble control
BASS	4	U	LSOUT output bass control
SURR	1	U	Selection of quasi-surround function ON/OFF (0: OFF, 1: ON)
NRSW	1	U	Selection of the output signal (Stereo mode, SAP mode)
FOMO	1	U	Turn to forced MONO by means of FOMO = 1. (Left channel only is MONO during SAP output.)
EXT1	1	U	Selection of TV mode or external input mode for TVOUT output
EXT2	1	U	Selection of TV mode or external input mode for LSOUT output
EXTFOMO	1	U	Forced MONO for external input (1: forced MONO ON)
M1	1	U	Selection of TVOUT mute ON/OFF (0: mute ON, 1: mute OFF)
M2	1	U	Selection of LSOUT mute ON/OFF (0: mute ON, 1: mute OFF)
INSW1	1	S	Select of standard input level.
INSW2	1	S	Select of standard input level.
SAPC	1	S	Selection of SAP mode or L + R mode according to the presence of SAP broadcasting

* Classification U: User control
A: Adjustment
S: Proper to set
T: Test

Status registers

Register	Number of bits	Contents	
PONRES	1	POWER ON RESET detection;	1: RESET
STEREO	1	Stereo discrimination of the COMPIN input signal;	1: Stereo
SAP	1	SAP discrimination of the COMPIN input signal;	1: SAP
NOISE	1	Noise level discrimination of the SAP signal;	1: Noise
STLPF	1	Status of STEREO filter adjustment;	1: OK range
SAPLPF	1	Status of SAP filter adjustment;	1: OK range
SAPVCO1	1	Status 1 of SAP VCO free running frequency adjustment;	0: OK range
SAPVCO2	1	Status 2 of SAP VCO free running frequency adjustment;	1: OK range

Description of Control Registers

ATT (4): Adjust the signal level input to COMPIN (Pin 17) to the standard input level.
Variable range of the input signal: standard input level -5.0 dB to +3.0 dB
0 = Level min.
F = Level max.

STVCO (6): Adjust STEREO VCO free running frequency (fo).
Variable range: fo ±20%
0 = Free running frequency min.
3F= Free running frequency max.

SAPVCO (4): Adjust SAPVCO free running frequency (fo).
Variable range: fo ±20%
0 = Free running frequency min.
F = Free running frequency max.

SAPLPF (4): Adjust the filter fo of the SAP block.
Variable range: fo ±20%
0 = Frequency min.
F = Frequency max.

STLPF (6): Adjust the filter fo of the ST and dbx blocks.
Variable range: fo ±20%
0 = Frequency min.
3F= Frequency max.

SPECTRAL (6): Perform high frequency (fs = 3 kHz) separation adjustment.
0 = Level max.
3F= Level min.

WIDEBAND (6): Perform low frequency (fs = 300 Hz) separation adjustment.
0 = Level min.
3F= Level max.

TEST1 (1): Set filter adjustment mode.
0 = Normal mode
1 = STLPF (STA3) and SAPLPF (STA4) adjustment mode
In addition, the following outputs are present at Pins 35 and 34.
TVOUT-L (Pin 35): SAP BPF OUT
TVOUT-R (Pin 34): NR BPF OUT

TEST-DA (1): Set DAC output test mode and STVCO adjustment mode.
0 = Normal mode
1 = DAC output test mode and STVCO adjustment mode
In addition, the following outputs are present at Pins 35 and 34.
TVOUT-L (Pin 35): DA control DC level
TVOUT-R (Pin 34): STEREO VCO oscillation frequency (4fH)

PRE-VOL (4): Input signal level control of sound processor block
When turning on the bass boost, treble boost or surround, attenuate the input signal to the sound processor block using “PREVOL” so that the signal is not dissipated inside the processor.
4 = Volume Min. (-13.75 dB)
F = Volume Max. (0 dB)
-1.25 dB/STEP

VOL-L (6): LSOUT-L output signal level control
0 = Volume Min. (-80 dB)
3F= Volume Max. (0 dB)
-1.25 dB/STEP

VOL-R (6): LSOUT-R output signal level control
0 = Volume Min. (-80 dB)
3F= Volume Max. (0 dB)
-1.25 dB/STEP

VOL-SURR (6): SURROUT output signal level control
0 = Volume Min. (-80 dB)
3F= Volume Max. (0 dB)
-1.25 dB/STEP

TREBLE (4): LSOUT output treble control
0 = Treble Min.
7 & 8 = Treble Center (0 dB)
F = Treble Max.

BASS (4): LSOUT output bass control
0 = Bass Min.
7 & 8 = Bass Center (0 dB)
F = Bass Max.

SURR (1): Surround function selection
0 = Surround OFF
1 = Surround ON

NRSW (1): Select stereo mode or SAP mode
0 = Stereo mode
1 = SAP mode

FOMO (1): Select forced MONO mode
0 = Normal mode
1 = Forced MONO mode

SAPC (1): Select the SAP signal output mode
When there is no SAP signal, the conditions for selecting SAP output are selected by SAPC.
0 = L + R output is selected
1 = SAP output is selected

INSW1 (1) & INSW2 (1): Select standard input level of COMPIN(Pin 17)

	Standard input level
INSW1 = 0 , INSW2 = 0	245mVrms
= 1 , = 1	245mVrms
INSW1 = 1 , INSW2 = 0	490mVrms
INSW1 = 0 , INSW2 = 1	100mVrms

EXT1 (1): Select TV mode or external input mode for TVOUT output.
0 = TV mode
1 = External input mode

EXT2 (1): Select TV mode or external input mode for LSOUT output.
0 = TV mode
1 = External input mode

EXT-FOMO (1): Turn external input to forced MONO.
0 = Normal mode
1 = External input is forced MONO.
Input the same signal to both AUXIN-L and AUXIN-R.

M1 (1): Mute the TVOUT-L and TVOUT-R output.
0 = Mute ON
1 = Mute OFF

M2 (1): Mute the LSOUT-L and LSOUT-R output.
0 = Mute ON
1 = Mute OFF

Description of Mode Control

Priority ranking: M1/M2 > EXT1/EXT2 > TEST-DA > TEST1 > (NRSW & FOMO & SAPC)

Mode control	SAPC=0	SAPC=1
NRSW	"Select dbx input and TV decoder output" Conditions: FOMO = 0 NRSW = 0 (MONO or ST output) • During ST input: left channel:L, right channel: R • During other input: left channel:L + R, right channel: L + R NRSW = 1 (SAP output) • When there is "SAP" during SAP discrimination - left channel: SAP, right channel: SAP • When there is "No SAP", output is the same as when NRSW = 0.	"Select dbx input and TV decoder output" Conditions: FOMO = 0 NRSW = 0 (MONO or ST output) As on the left NRSW = 1 (SAP output) • Regardless of the presence of SAP discrimination, dbx input: "SAP" left channel: SAP, right channel: SAP However, when there is no SAP, SAPOUT output is soft muted (-7 dB)
FOMO	"Forced MONO" FOMO = 1 • During SAP output: left channel: L + R, right channel: SAP • During ST or MONO output: left channel: L + R, right channel: L + R	
SAPC	Change the selection conditions for "MONO or ST output" and "SAP output". SAPC = 0: Switch to SAP output when there is SAP discrimination. Do not switch to SAP output when there is no SAP discrimination. SAPC = 1: Switch to SAP output regardless of whether there is SAP discrimination.	
M1/M2	"MUTE" M1 = 0: TVOUT output is muted. M2 = 0: LSOUT output is muted.	
EXT1/EXT2	"TV mode/external input mode selection" EXT1 = 0: Set TVOUT output to TV mode. EXT1 = 1: Set TVOUT output to external input mode. EXT2 = 0: Set LSOUT output to TV mode. EXT2 = 1: Set LSOUT output to external input mode.	
TEST1	"TEST1" TEST1 = 1 Return adjustment data with STATUS REGISTER as an adjustment mode. In addition, outputs are as follows. left channel: SAP BPF OUT right channel: NR BPF OUT	
TEST-DA	"TEST-DA" TEST-DA = 1 Used to adjust the D/A TEST and STVCO. left channel: D/A output right channel: STVCO oscillation frequency ($4f_H$)	

Decoder Output and Mode Control Table 1 (SAPC = 1)

Input signal mode	Mode detection			Mode control			dbx	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC	input	Lch	Rch
MONO 1)	0	0	0	0	*	1	MUTE	L+R	L+R
	0	0	0	1	0	1	SAP	SAP	SAP
	0	0	0	1	1	1	SAP	L+R	SAP
	0	*	1	0	*	1	MUTE	L+R	L+R
	0	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	*	1	1	1	1	(SAP)	L+R	(SAP)
STEREO 1)	1	0	*	0	0	1	L-R	L	R
	1	0	*	0	1	1	MUTE	L+R	L+R
	1	1	1	0	0	1	L-R	L	R
	1	1	1	0	1	1	MUTE	L+R	L+R
	1	0	0	1	0	1	SAP	SAP	SAP
	1	0	0	1	1	1	SAP	L+R	SAP
	1	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	*	1	1	1	1	(SAP)	L+R	(SAP)
MONO & SAP	0	1	*	0	0	1	MUTE	L+R	L+R
	0	1	*	0	1	1	MUTE	L+R	L+R
	0	1	0	1	0	1	SAP	SAP	SAP
	0	1	0	1	1	1	SAP	L+R	SAP
	0	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	1	(SAP)	L+R	(SAP)
STEREO & SAP	1	1	*	0	0	1	L-R	L	R
	1	1	*	0	1	1	MUTE	L+R	L+R
	1	1	0	1	0	1	SAP	SAP	SAP
	1	1	0	1	1	1	SAP	L+R	SAP
	1	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	1	(SAP)	L+R	(SAP)

Note

(SAP) : The SAPOUT output signal is soft muted (approximately -7 dB).
The signal is soft muted when NOISE = 1.

* : Don’t care.

1): SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.
"NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

Decoder Output and Mode Control Table 2 (SAPC = 0)

Input signal mode	Mode detection			Mode control			dbx	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC	input	Lch	Rch
MONO 1)	0	0	*	*	*	0	MUTE	L+R	L+R
	0	1	1	0	0	0	MUTE	L+R	L+R
	0	1	1	0	1	0	MUTE	L+R	L+R
	0	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	0	(SAP)	L+R	(SAP)
STEREO 1)	1	0	*	0	0	0	L-R	L	R
	1	0	*	0	1	0	MUTE	L+R	L+R
	1	0	*	1	0	0	L-R	L	R
	1	0	*	1	1	0	MUTE	L+R	L+R
	1	1	1	0	0	0	L-R	L	R
	1	1	1	0	1	0	MUTE	L+R	L+R
	1	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	0	(SAP)	L+R	(SAP)
MONO & SAP	0	1	0	0	0	0	MUTE	L+R	L+R
	0	1	0	0	1	0	MUTE	L+R	L+R
	0	1	0	1	0	0	SAP	SAP	SAP
	0	1	0	1	1	0	SAP	L+R	SAP
	0	1	1	0	0	0	MUTE	L+R	L+R
	0	1	1	0	1	0	MUTE	L+R	L+R
	0	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	0	(SAP)	L+R	(SAP)
STEREO & SAP	1	1	0	0	0	0	L-R	L	R
	1	1	0	0	1	0	MUTE	L+R	L+R
	1	1	0	1	0	0	SAP	SAP	SAP
	1	1	0	1	1	0	SAP	L+R	SAP
	1	1	1	0	0	0	L-R	L	R
	1	1	1	0	1	0	MUTE	L+R	L+R
	1	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	0	(SAP)	L+R	(SAP)

Note

(SAP) : The SAPOUT output signal is soft muted (approximately -7 dB).
The signal is soft muted when NOISE = 1.

* : Don't care.

1): SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.
"NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

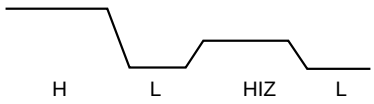
Mode Control Table 3

EXT1	EXT2	EXTFOMO	M1	M2	TV OUT-L	TV OUT-R	LS OUT-L	LS OUT-R
0	0	*	1	1	TV mode L channel	TV mode R channel	TV mode L channel	TV mode R channel
1	0	0	1	1	EXT mode L channel	EXT mode R channel	TV mode L channel	TV mode R channel
1	0	1	1	1	EXT mode L channel	EXT mode L channel	TV mode L channel	TV mode R channel
0	1	0	1	1	TV mode L channel	TV mode R channel	EXT mode L channel	EXT mode R channel
0	1	1	1	1	TV mode L channel	TV mode R channel	EXT mode L channel	EXT mode L channel
1	1	0	1	1	EXT mode L channel	EXT mode R channel	EXT mode L channel	EXT mode R channel
1	1	1	1	1	EXT mode L channel	EXT mode L channel	EXT mode L channel	EXT mode L channel
*	*	*	0	1	MUTE	MUTE	Selected according to the EXT1, EXT2, EXTFOMO conditions	Selected according to the EXT1, EXT2, EXTFOMO conditions
*	*	*	1	0	Selected according to the EXT1, EXT2, EXTFOMO conditions	Selected according to the EXT1, EXT2, EXTFOMO conditions	MUTE	MUTE

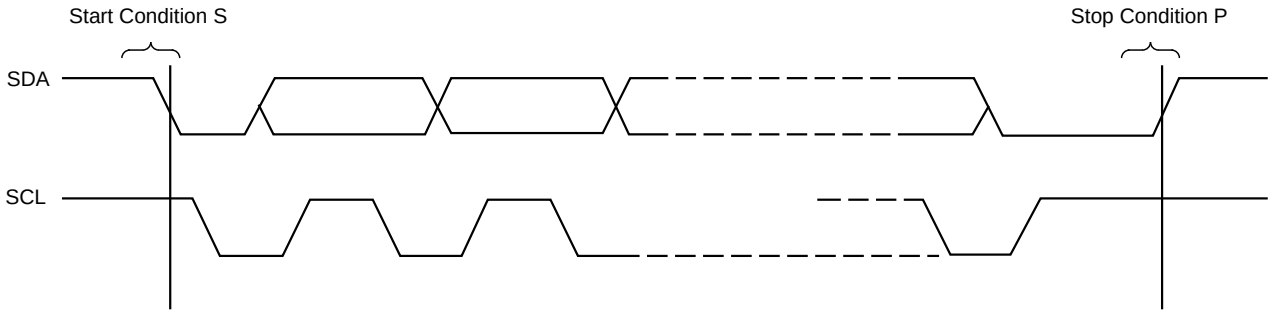
I²C BUS Signal

There are two I²C signals, SDA (Serial DATA) and SCL (Serial CLOCK) signals. SDA is a bidirectional signal.

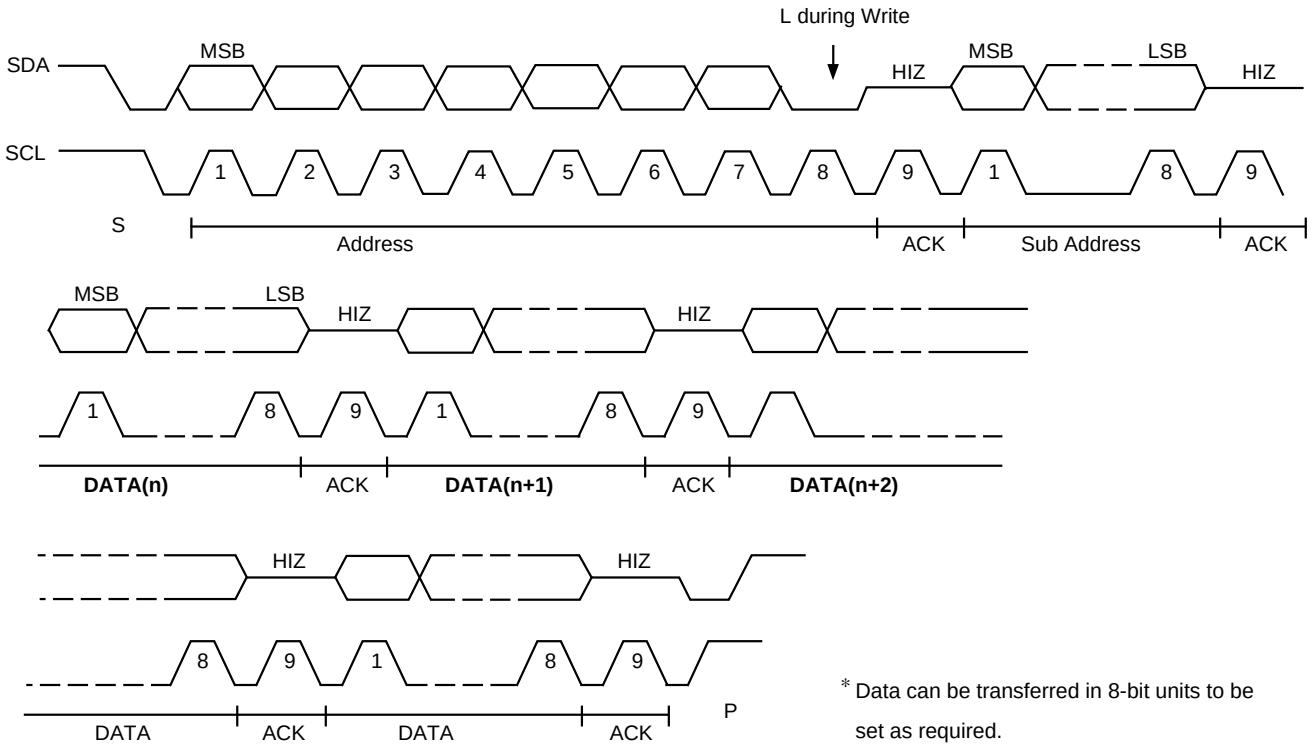
• Accordingly there are 3 values outputs, H, L and HIZ.



• I²C transfer begins with Start Condition and ends with Stop Condition.

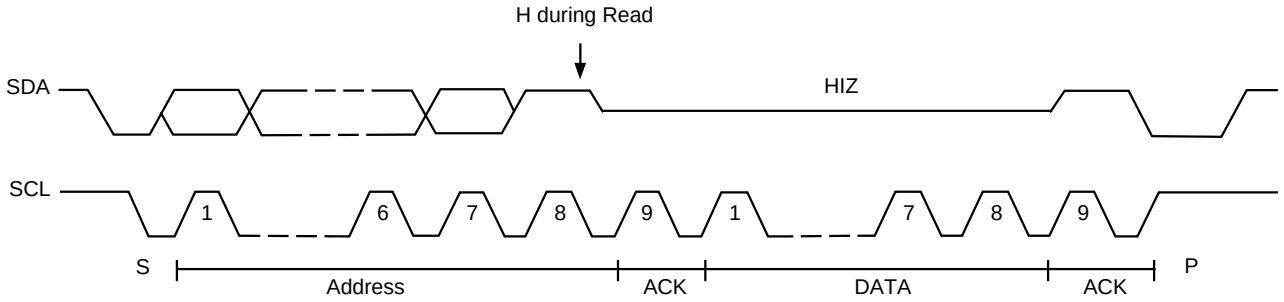


• I²C data Write (Write from I²C controller to the IC)

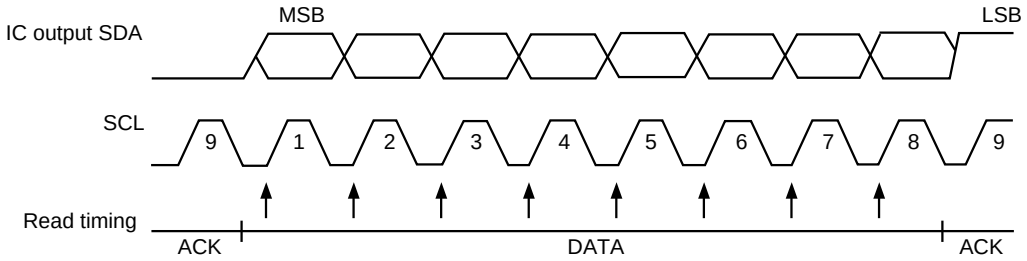


* Data can be transferred in 8-bit units to be set as required.
Sub address is incremented automatically.

• I²C data Read (Read from the IC to I²C controller)

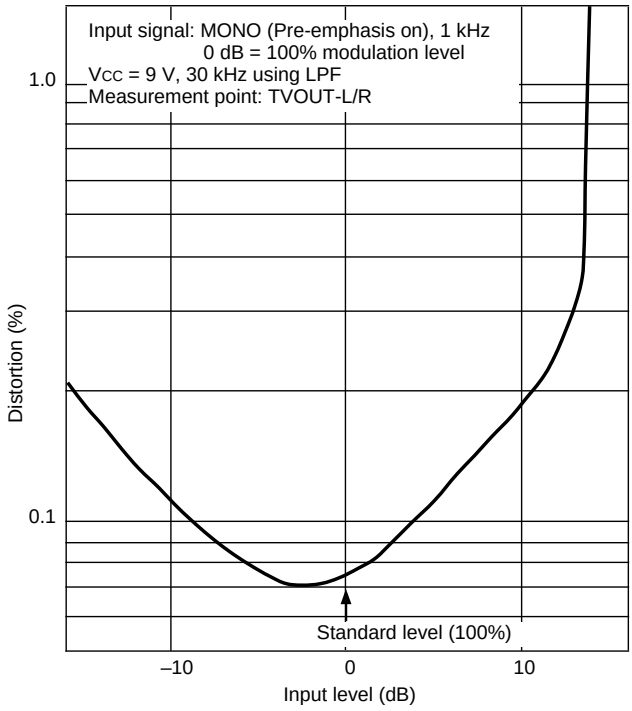


• Read timing

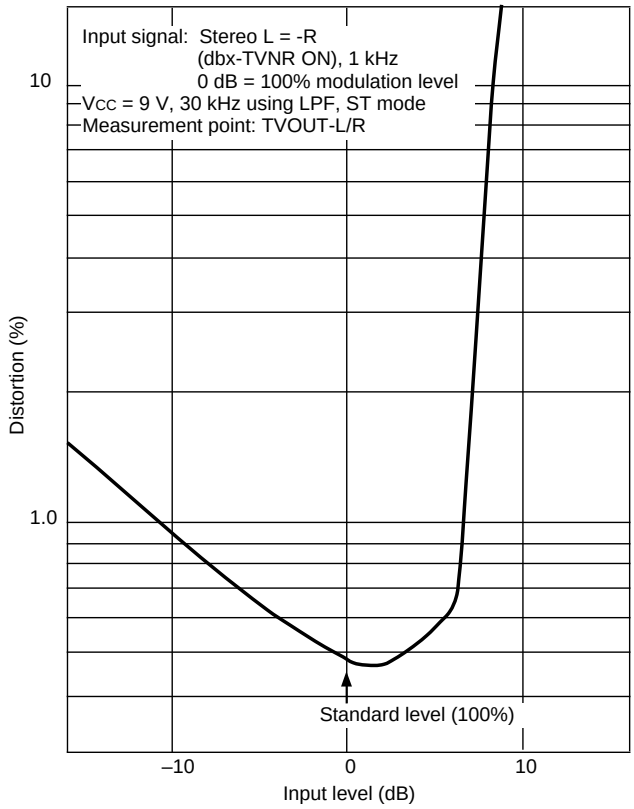


* Data Read is performed during SCL rise.

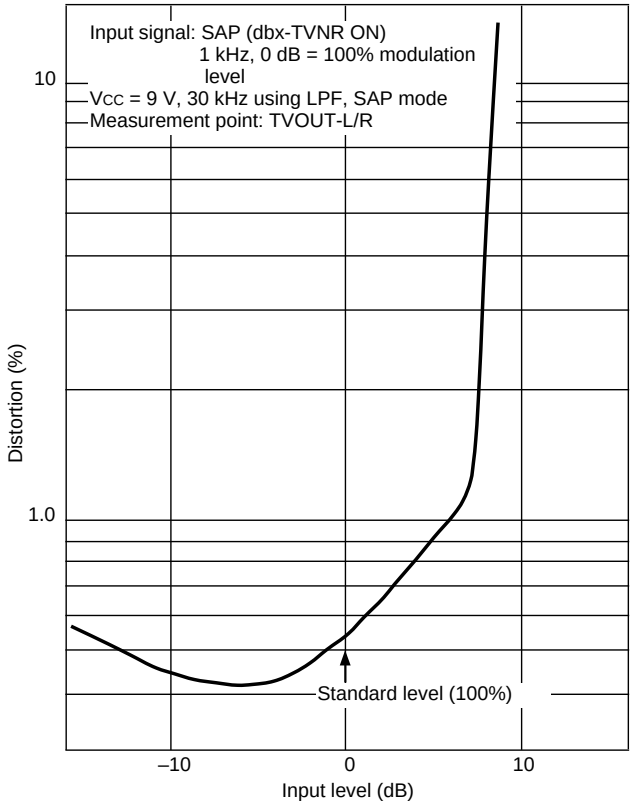
Input level vs. Distortion characteristics 1 (MONO)



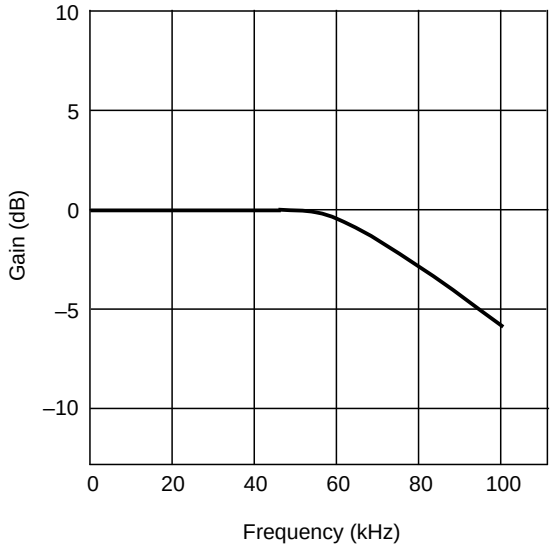
Input level vs. Distortion characteristics 2 (Stereo)



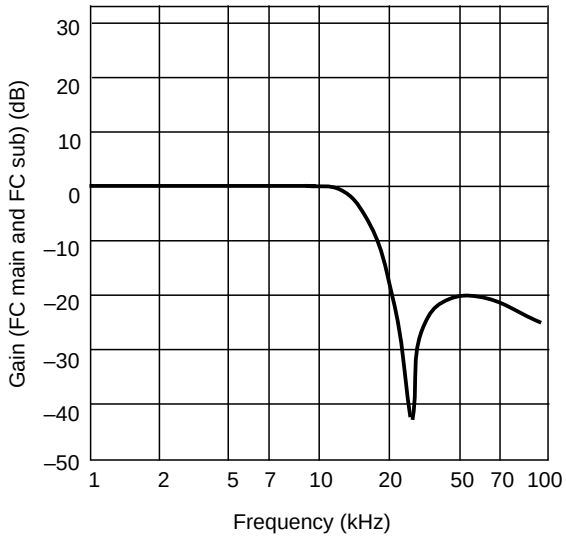
Input level vs. Distortion characteristics 3 (SAP)



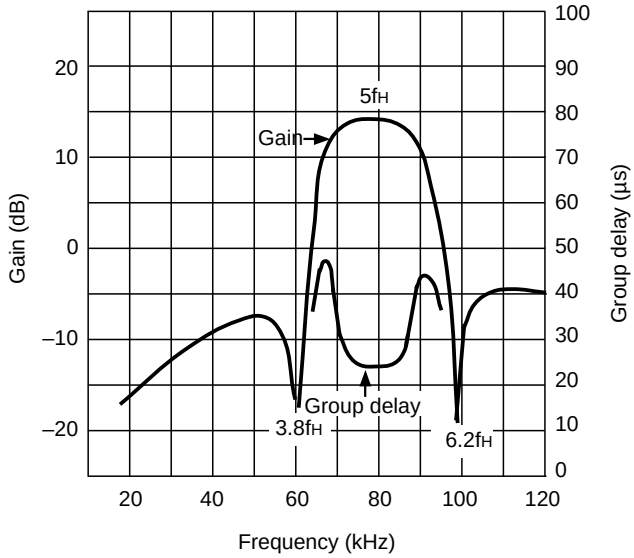
Stereo LPF frequency characteristics



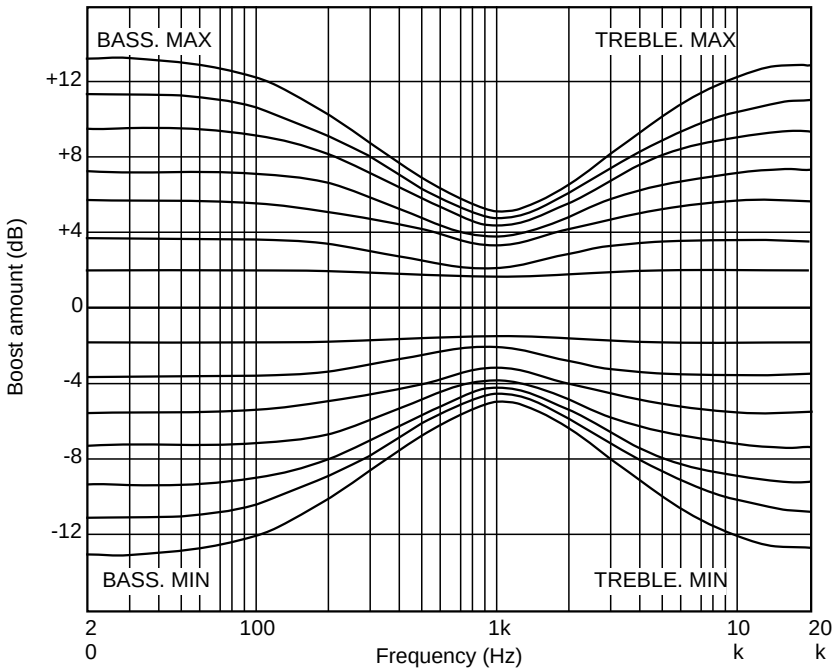
Main LPF and Sub LPF frequency characteristics



SAP frequency characteristics and group delay

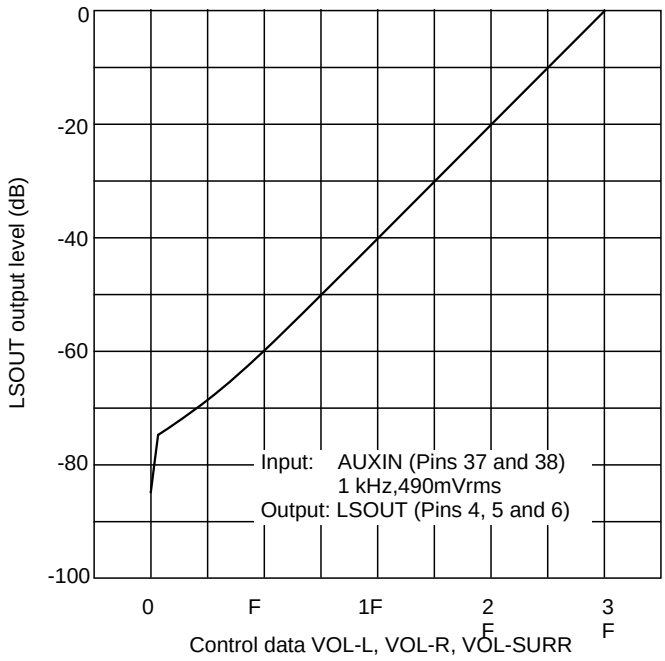


BASS - TREBLE
characteristics



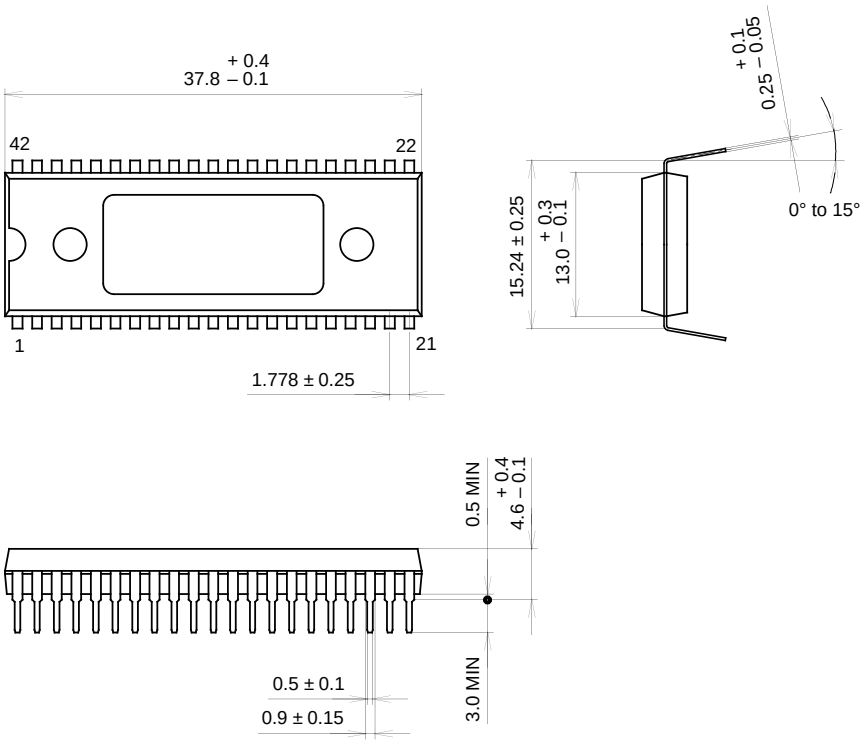
Input: AUXIN (Pins 37 and 38) 245 mVrms
Output: LSOUT (Pins 4, 5 and 6)

Volume
characteristics



Package Outline Unit: mm

42PIN SDIP (PLASTIC) 600mil



SONY CODE	SDIP-42P-02
EIAJ CODE	SDIP042-P-0600-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	4.4g