SONY

# CXA1995N

## Filterless IC for Pager Reception

### Description

The CXA1995N is a filterless IC for pager reception. This IC incorporates functions from the 1st mixer to FSK comparator and is suitable for reduction in set size.

### Features

- External select filter not required
- External detect discriminator not required
- Two operational amplifiers to compose the data LPF
- Coupling capacitor not required between detector output buffer and LPF operational amplifier
- Reduced-voltage detection function
- Battery saving function
- Reference power supply for operational amplifier and comparator
- Low current consumption ($I_{CC}1$ = 0.4mA at $V_{CC}1$ = 1.3V, $I_{CC}2$ = 2.1mA at $V_{CC}2$ = 2.3V)

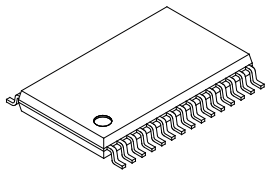
### Absolute Maximum Ratings

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{CC}$ | 7 | V |
| • Operating temperature | Topr | –20 to +75 | °C |
| • Storage temperature | Tstg | –65 to +150 | °C |
| • Allowable power dissipation | $P_D$ | 500 | mW |

### Operating Conditions

| | | | |
|---|---|---|---|
| Supply voltage | $V_{CC}1$ | 1.0 to 3.4 | V |
| | $V_{CC}2$ | 2.0 to 4.0 | V |

30 pin SSOP (Plastic)



### Applications

Receivers of paging system

### Structure

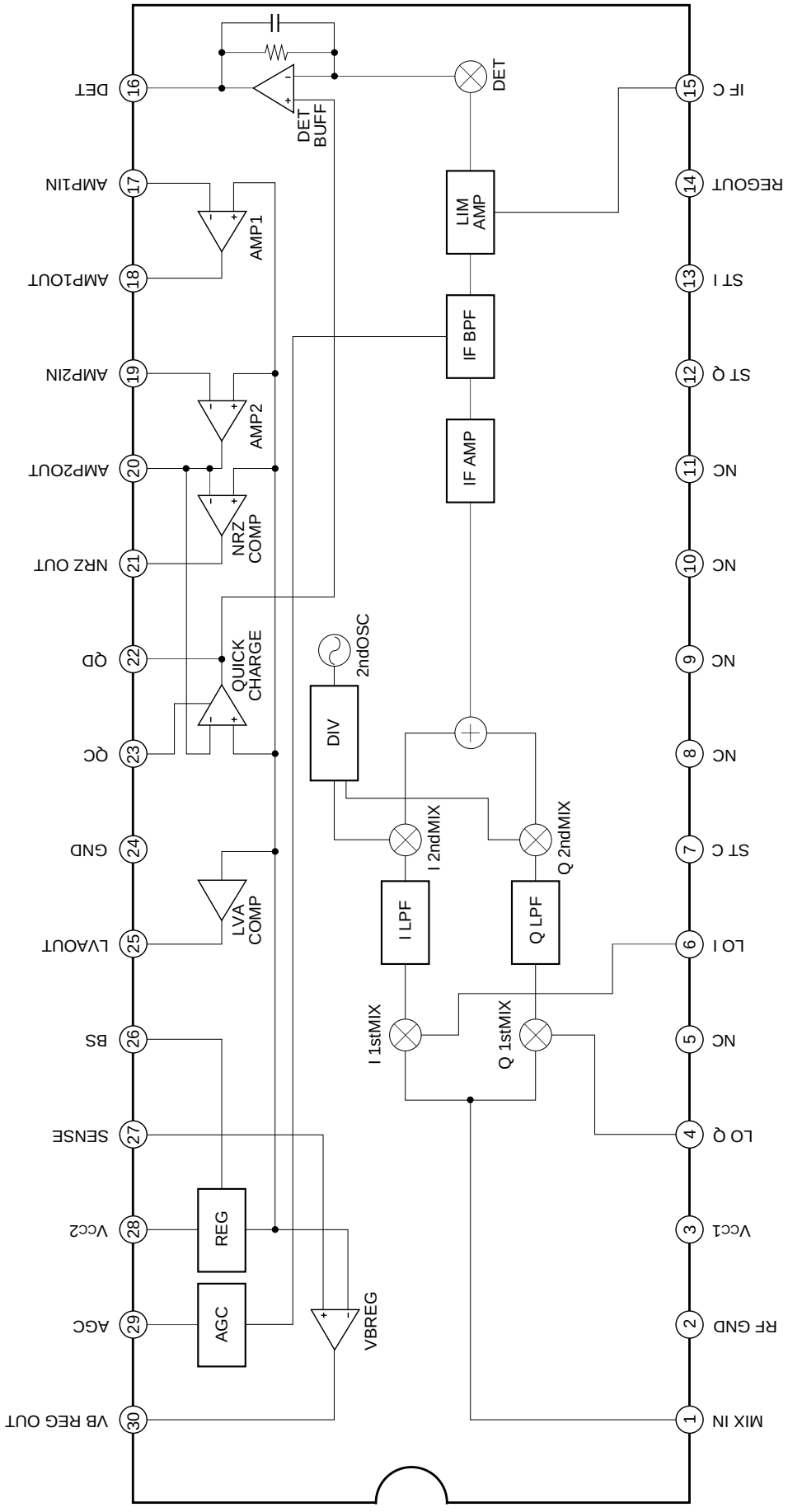
Bipolar silicon monolithic IC



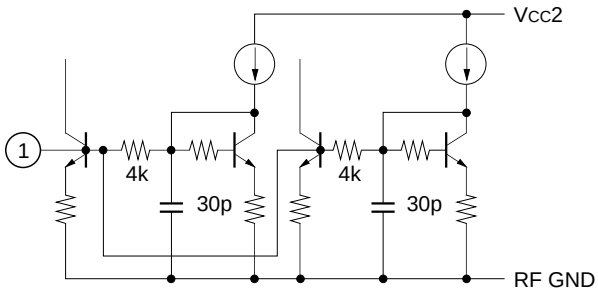
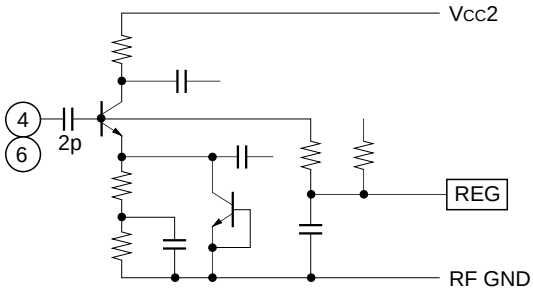
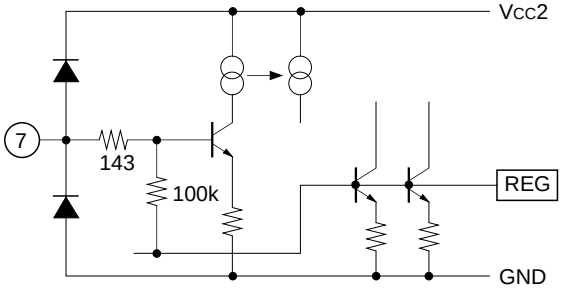


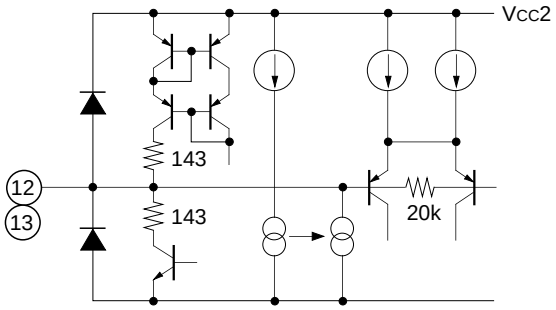
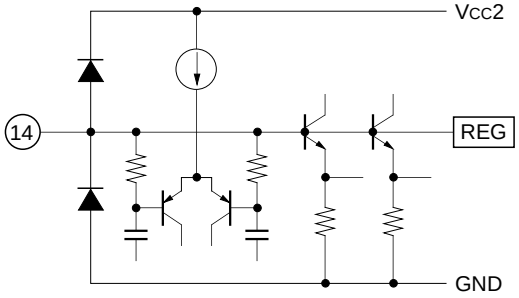
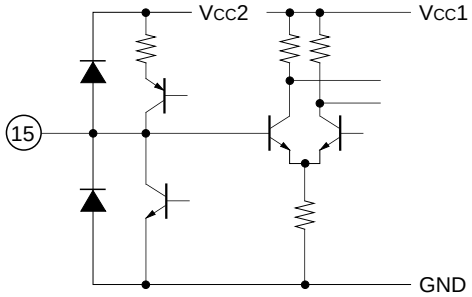
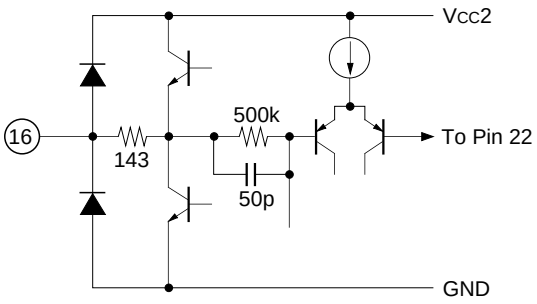
E95126A68-PS

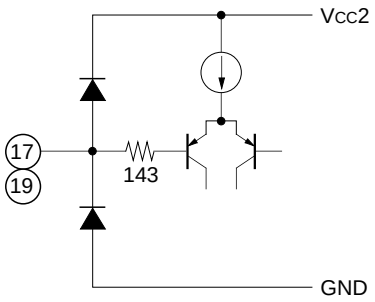
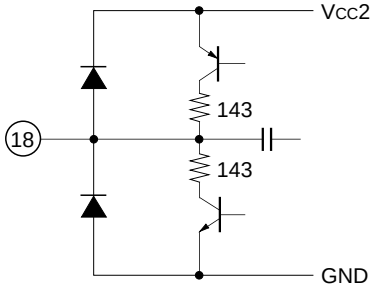
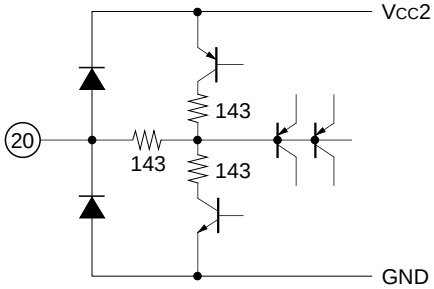
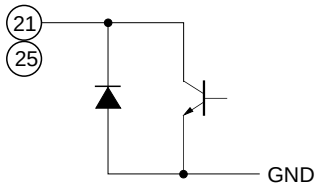
**Block Diagram**

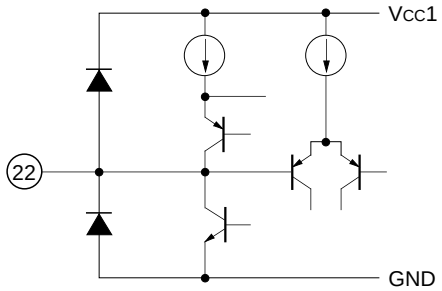
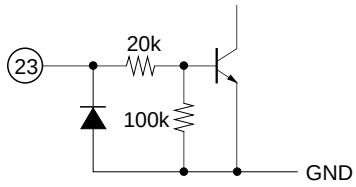
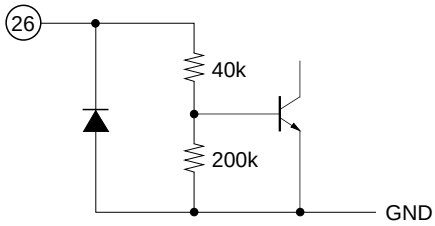
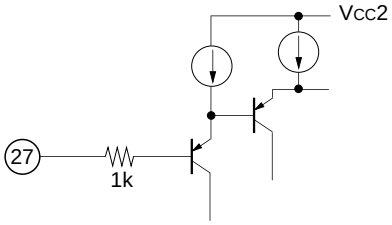


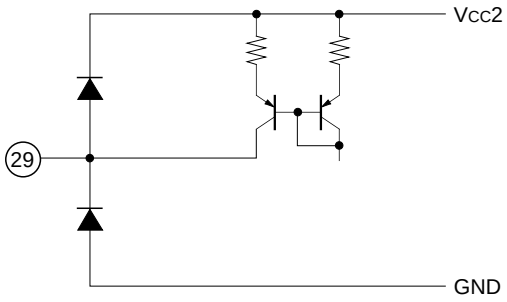
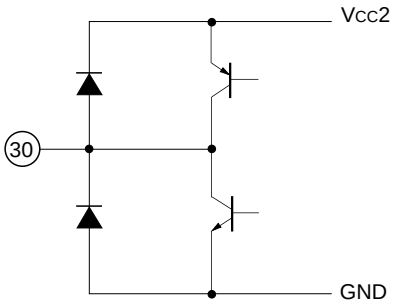
**Pin Description**

| Pin No. | Symbol | Pin voltage | Equivalent circuit | Description |
|---|---|---|---|---|
| 1 | MIX IN | 0.9V |  | 1st mixer input. |
| 2 | RF GND | | | GND for 1st mixer |
| 3 | Vcc1 | | | Vcc1. |
| 4<br>6 | LO Q<br>LO I | |  | 1st mixer local signal input. A phase shifter which shifts the phase 90° is composed by connecting this pin to Pin 6. Adjust so that the input levels of Pins 4 and 6 are equal. |
| 5<br>8<br>9<br>10<br>11 | NC | | | Not connected. |
| 7 | ST C | 0.8V |  | Determines the capacitor quick charge time connected to Pins 12 and 13. When the capacitance is larger, the quick charge time gets longer. |

| Pin No. | Symbol | Pin voltage | Equivalent circuit | Description |
|---|---|---|---|---|
| 12<br>13 | ST Q<br>ST I | 0.8V |  | Determines the 2nd mixer rise time and the low-band high-pass characteristics, so that this pin has an effect on the reception sensitivity and band-pass width. |
| 14 | REG OUT | 0.8V |  | Regulator output. |
| 15 | IF C | 0.8V |  | LIM AMP decoupling. |
| 16 | DET | 0.2V |  | FM detector output. |

| Pin No. | Symbol | Pin voltage | Equivalent circuit | Description |
|---|---|---|---|---|
| 17<br>19 | AMP1IN<br>AMP2IN | 0.2V |  | Operational amplifier AMP1 and AMP2 inputs. |
| 18 | AMP1OUT | 0.2V |  | Operation amplifier AMP1 output. |
| 20 | AMP2OUT | 0.2V |  | NRZ comparator input. Connects the operational amplifier AMP2 output. |
| 21<br>25 | NRZ OUT<br>LVAOUT | |  | NRZ and LVA comparator outputs and they are open collectors. |

| Pin No. | Symbol | Pin voltage | Equivalent circuit | Description |
|---|---|---|---|---|
| 22 | QD | 0.2V |  | Connects the capacitor that determines the low cut-off frequency for the entire system. |
| 23 | QC | |  | Controls the ON/OFF of the quick charge circuit. |
| 24 | GND | | | GND. |
| 26 | BS | |  | Controls the buttery saving. Setting this pin low suspends the operation of IC. |
| 27 | SENSE | 0.2V |  | Built-in amplifier input for the constant voltage supply.<br>Controlled so as that this pin becomes 200mV. |
| 28 | Vcc2 | | | Vcc2. |

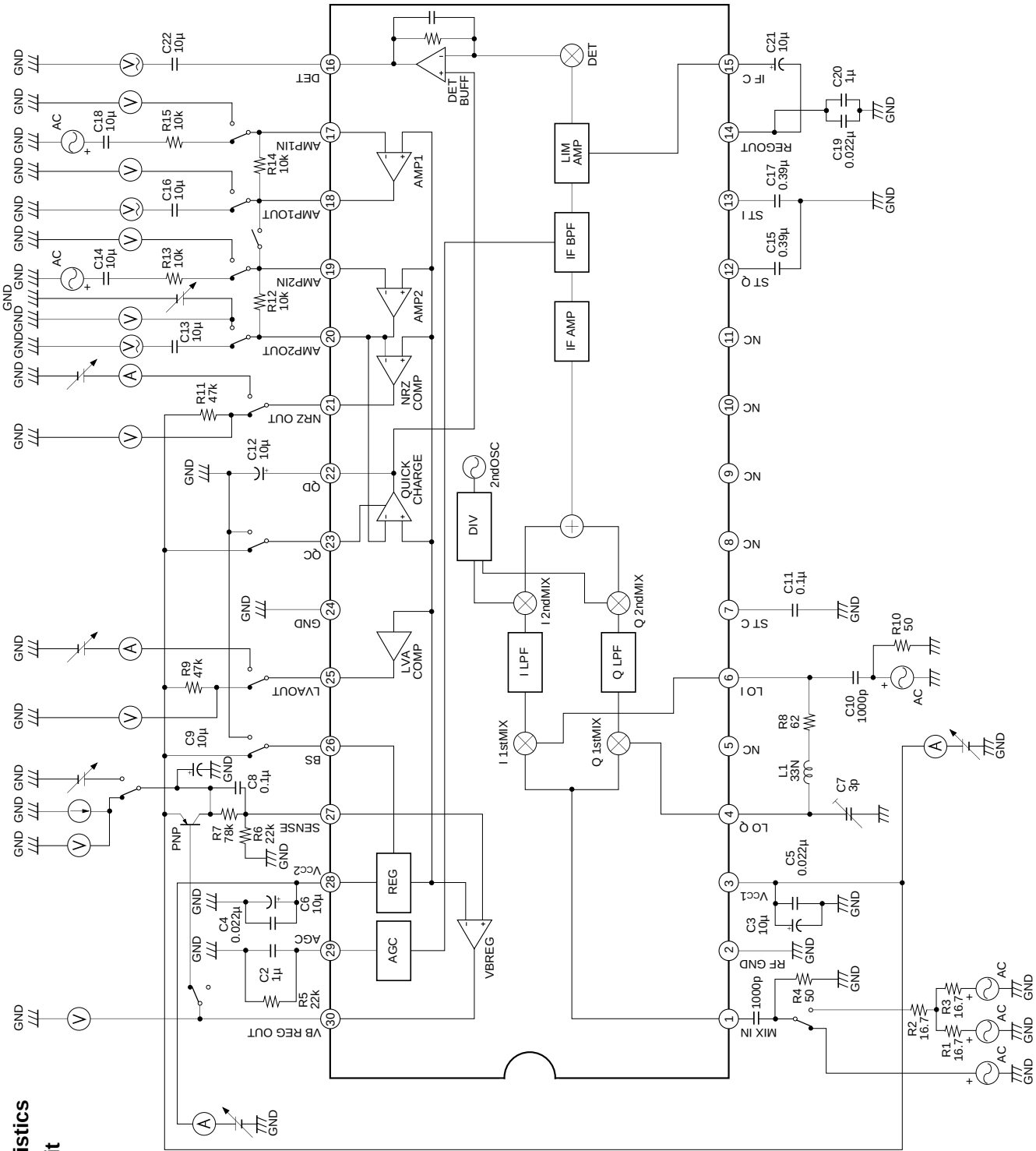
| Pin No. | Symbol | Pin voltage | Equivalent circuit | Description |
|---|---|---|---|---|
| 29 | AGC | |  | Sets the AGC time constant.<br>Grounding this pin turns AGC OFF. |
| 30 | VB REG OUT | |  | Built-in amplifier output for the constant voltage supply.<br>Connects the PNP transistor base.<br>(100µA current capacitance) |

**Electrical Characteristics**

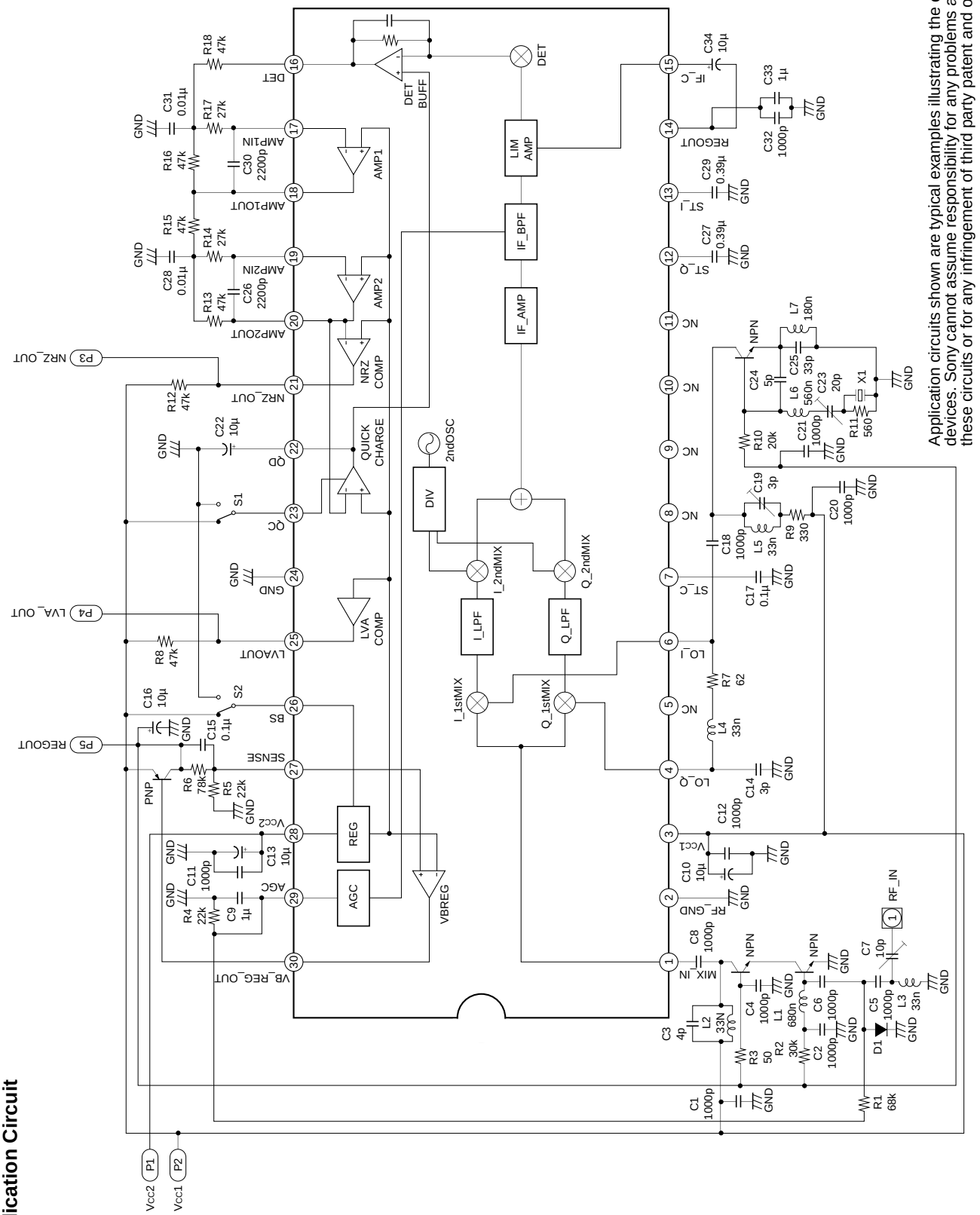
Unless otherwise specified, $V_{CC}1$ = 1.3V, $V_{CC}2$ = 2.3V, Ta = 25°C, $f_S$ = 280MHz, $f_{MOD}$ = 600Hz, $f_{DEV}$ = 4.5kHz

| Item | Symbol | Measurement conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Current consumption 1 (Vcc1) | $I_{CC}1$ | $V_{CC}1$ current consumption for $V_{CC}1$ = 1.3V<br>Excluding the current of Pins 21, 25, 26, external RF amplifier and oscillator current consumption. | 200 | 400 | 650 | µA |
| Current consumption 2 (Vcc2) | $I_{CC}2$ | $V_{CC}2$ current consumption for $V_{CC}2$ = 2.3V | 1.3 | 2.1 | 3.0 | mA |
| Current consumption 3 (BS) | $I_{CCS}$ | Current consumption for buttery saving | | 4 | 20 | µA |
| Op amp. input bias current | $I_{BIAS}$ | | | 40 | 200 | nA |
| Op amp. output voltage amplitude | $V_O$ | | 140 | | | mVp-p |
| NRZ output saturation voltage | $V_{SATNRZ}$ | | | | 0.4 | V |
| NRZ output leak current | $I_{LNRZ}$ | | | | 5.0 | µA |
| LVA output saturation voltage | $V_{SATLVA}$ | | | | 0.4 | V |
| LVA output leak current | $I_{LLVA}$ | | | | 5.0 | µA |
| LVA operating voltage | $V_{LVA}$ | | 1.10 | 1.15 | 1.20 | V |
| VB output saturation voltage | $V_{SATVB}$ | | | | 0.4 | V |
| VB output current | $I_{OUT}$ | | 100 | | | µA |
| Logic input high voltage | $V_{THBSV}$ | | 0.9 | | | V |
| Logic input low voltage | $V_{TLBSV}$ | | | | 0.4 | V |
| Detector output voltage | $V_{ODET}$ | | 25 | 50 | 80 | mVrms |

**Electrical Characteristics**
**Measurement Circuit**



## Application Circuit




Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

## Description of Operation

### 1. Power Supply

This IC has two power supplies, $V_{CC}2$ and $V_{CC}1$, to save the electric power. Vcc2 should be used in the condition where its voltage is 600mV or higher than that of Vcc1.

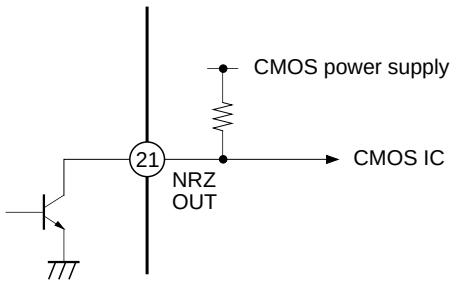
$V_{CC}2 \geq 600mV + V_{CC}1$

### 2. Rise Time

The 2nd mixer circuit should rise earlier than the AGC circuit for the IC's stable operation.
Take care to determine the capacitor values connected to Pins 7, 12, 13 and 29.

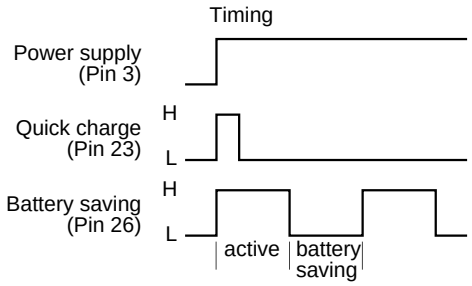
### 3. AMP1, AMP2, NRZ, COMP

Two operational amplifiers are built in this IC. One of them is connected internally to an NRZ comparator. These amplifiers are used to compose the LPF which removes the noise in the demodulating signal, and the resulting signal is input to the next-stage NRZ comparator.
The NRZ comparator performs the waveform shaping of this input signal and outputs it as a rectangular wave.
The output stage of the NRZ comparator is an open collector. When the CPU is a CMOS device and the supply voltage is different, the direct interface is possible with the usage shown below.




### 4. Quick Charge

In order to hasten the rise time from when the power supply is turned On or when reception standby, the CXA1995N features a quick charge circuit.
Therefore, the quick charge circuit eliminates the need to insert a capacitor between the detector output and the LPF as is the case with conventional ICs, but connects a capacitor to Pin 22 to determine the average signal level during steady-state reception. The electrostatic capacitance of the capacitor connected to Pin 22 should be chosen such that the voltage does not vary much due to discharge during battery saving.
Connect a signal for controlling the quick charge circuit to Pin 23. Setting this pin high enables the quick charge mode, setting this pin low enables the steady-state reception mode. Quick charge is used when the power supply is turned on. The battery saving must be set high at the time. Quick charge is also used according to need during battery saving.
Connect Pin 23 to GND when quick charge is not being used.



**5. LVACOMP**

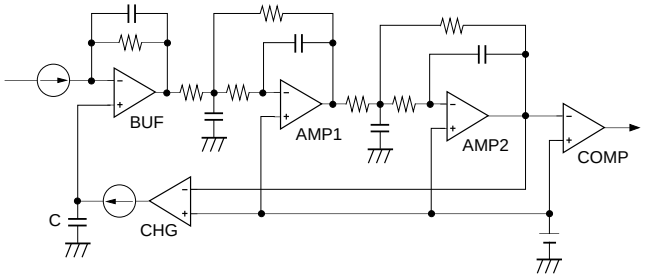
Pin 25 goes high (open) when the supply voltage becomes lower. Since the output is an open collector, it can be used to directly drive a CMOS device as Pin 21.

**Principle of Quick Charge Operation**

BUF shown below is the detector buffer amplifier, and AMP1 and AMP2 are the operational amplifiers to construct an LPF. COMP is the NRZ comparator. Coupling on conventional system is performed by placing a capacitor between the detector output buffer and the LPF operational amplifier, so coupling of DC is not performed. Thus, this coupling capacitor must be charged when restoring the system from reception standby mode to reception mode, it takes a little time when the NRZ signal comes from the comparator.

To shorten this rise time, as shown below, the CXA1995N adds a feedback loop from the comparator input to the input circuit of the detector output buffer. This equalizes the average value of the comparator input voltage to the reference voltage, with the quick charge circuit of CHG being set in the feedback loop. Switching the current of the quick charge circuit enables reduction of the rise time.

In this block, CHG is a comparator which compares input voltages and outputs a current based on this comparison. The current on CHG is switched between high and low at Pin 4. When changing reception standby mode to reception mode, switch the current to high to increase the charge current at C shown below and shorten the time constant. During steady-state reception mode, switch the current to low, lengthening the charge time constant and allowing for stable data retrieval.




**S Curve Characteristics**

Even if the input frequency is deviated, the feedback is applied to the detector output operating point so as to match it to the comparator reference voltage by the quick charge operation shown above. Therefore, this feedback must be halted in order to evaluate the S curve characteristics.

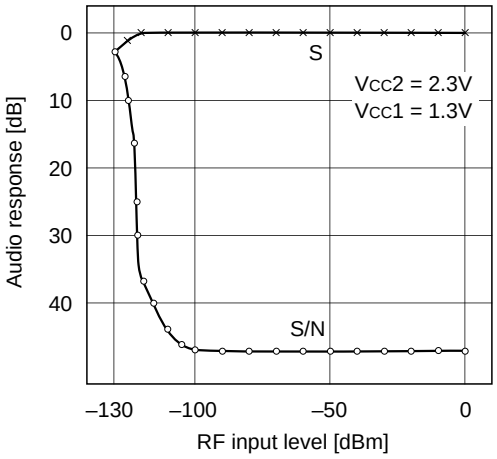
To execute the evaluation, measure the average voltage on Pin 20 first and input this voltage to Pin 7 from the external power supply, leaving Pin 16 open.

**Note on Operation**

Great care must be taken because this IC treats the high-frequency signals and the electrostatic discharge strength is weak.

## Example of Representative Characteristics

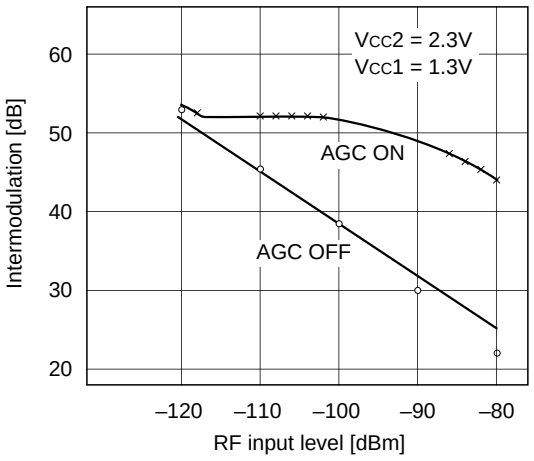
### Input/output characteristics with external RF AMP




RF 280MHz
FM 4.5kHz
600Hz rectangular wave

Lo 280MHz
–12dBm SG input

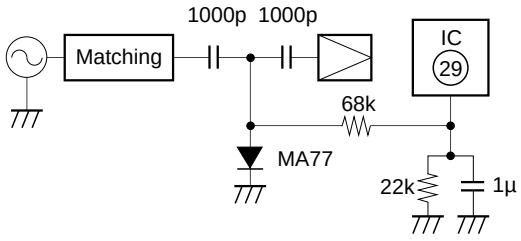
### Intermodulation characteristics with external RF AMP



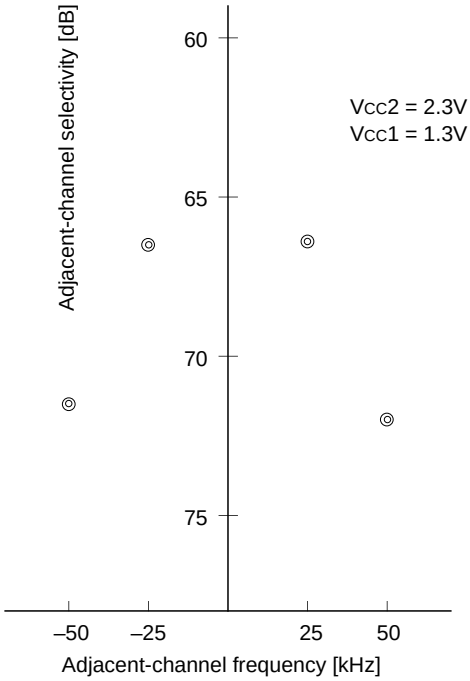

RF 280MHz
FM 4.5kHz
600Hz rectangular wave

Lo –12dBm SG input

Conditions
fr ± 25kHz Dev 3kHz Audio 400Hz
fr ± 50kHz Cw



**Adjacent-channel selectivity characteristics with external RF AMP**

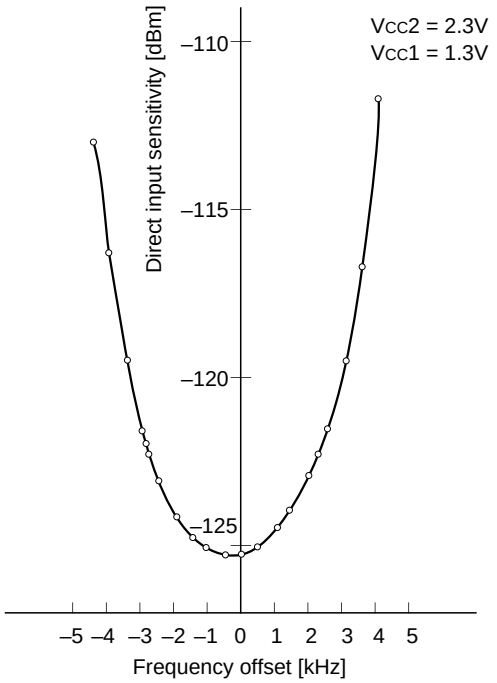



RF 280MHz
FM 4.5kHz
600Hz rectangular wave

Lo –12dBm SG input

Conditions
fr ± 25kHz, fr ± 50kHz
Dev 3kHz, Audio 400Hz

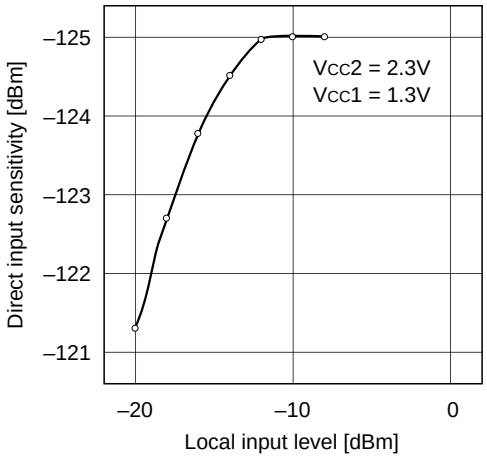
**Sensitivity band width with external RF AMP**




RF
FM 4.5kHz
600Hz rectangular wave

Lo 280MHz
–12dBm input

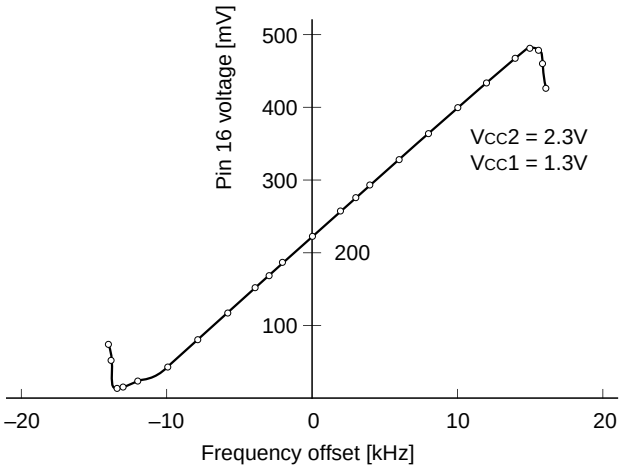
**Local input vs. Sensitivity characteristics with external RF AMP**




RF 280MHz
FM 4.5kHz
600Hz rectangular wave

Local input level is values of Pins 4 and 6 actually measured.

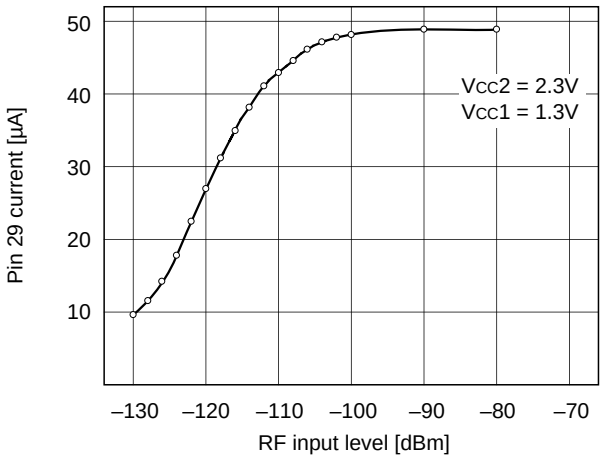
**S curve characteristics with external RF AMP**




RF –50dBm Cw
Lo 280MHz
–12dBm SG input

Pin 16 Open
Pin 22 225mV fixed (external power supply)

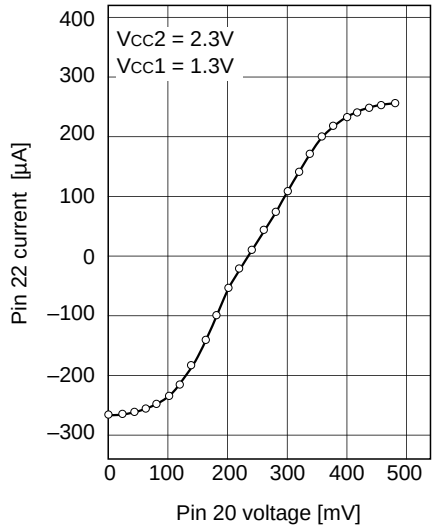
**AGC control characteristics with external RF AMP**




RF 280MHz
FM 4.5kHz
600Hz rectangular wave
Lo 280MHz
–12dBm

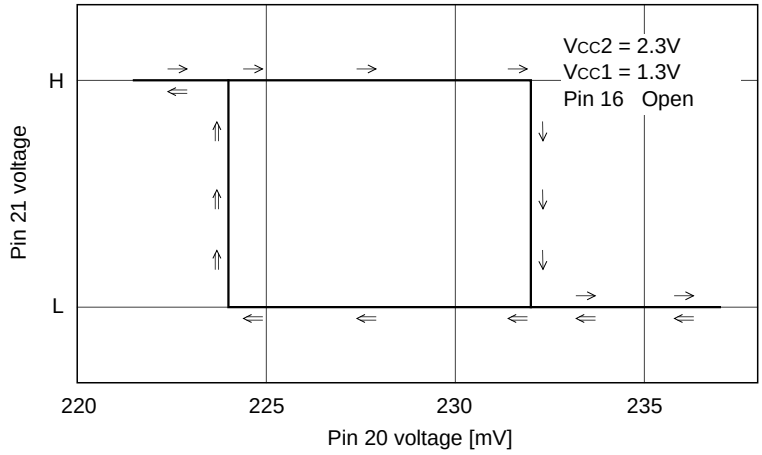
Pin 29 Open

**Quick charge control characteristics**

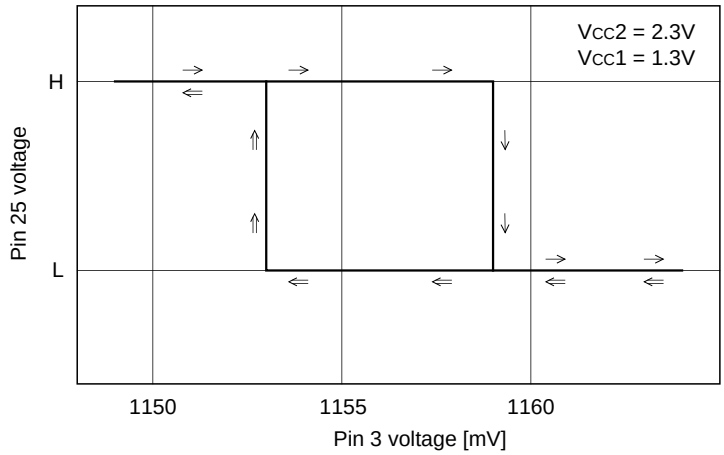



Pin 16 Open
Pin 22 225mV fixed (external power supply)
Pin 23 [H]

**NRZ comparator hysteresis characteristics**

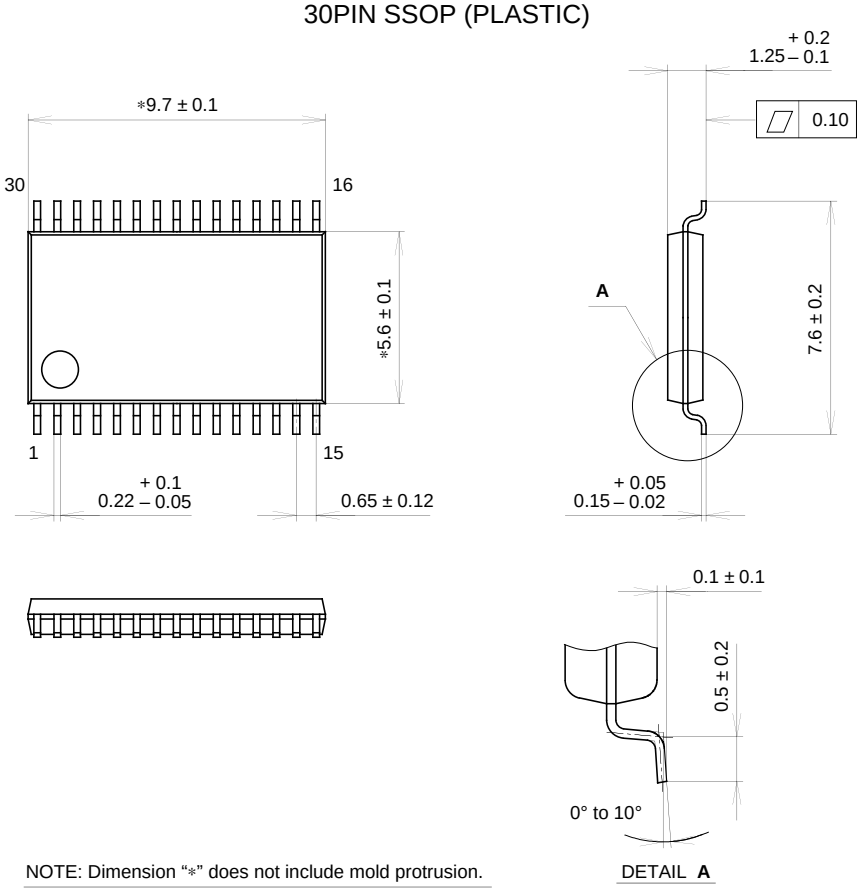



**LVA comparator hysteresis characteristics**



**Package Outline** Unit: mm

30PIN SSOP (PLASTIC)




NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

| | |
|---|---|
| SONY CODE | SSOP-30P-L01 |
| EIAJ CODE | SSOP030-P-0056-A |
| JEDEC CODE | ———————— |

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE WEIGHT | 0.1g |