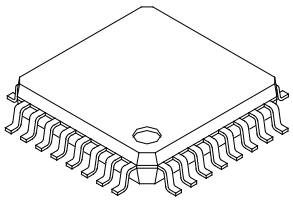
SONY

CXA2056Q

Digital CCD Camera Head Amplifier

32 pin QFP (Plastic)



Description

The CXA2056Q is a bipolar IC developed as a head amplifier for digital CCD cameras. This IC provides the following functions: correlated double sampling, AGC for the CCD signal, GCA for the low-band chroma signal, AMP for high-band chroma and line signals, A/D sample and hold, blanking, A/D reference voltage, and an output driver.

Features

- High sensitivity made possible by a high-gain AGC amplifier
- Blanking function provided for the purpose of calibrating the CCD output signal black level
- Regulator output pin provided for A/D converter reference voltage
- Built-in GCA and AMP for amplifying video signals (chroma and line signals) from external sources
- Built-in sample-and-hold circuits for camera signals required by external A/D converters

Absolute Maximum Ratings

• Supply voltage	V_{CC}	11	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1160	mW

Operating Conditions

Supply voltage	V_{CC}1, 2, 3	3 to 3.3	V

Applications

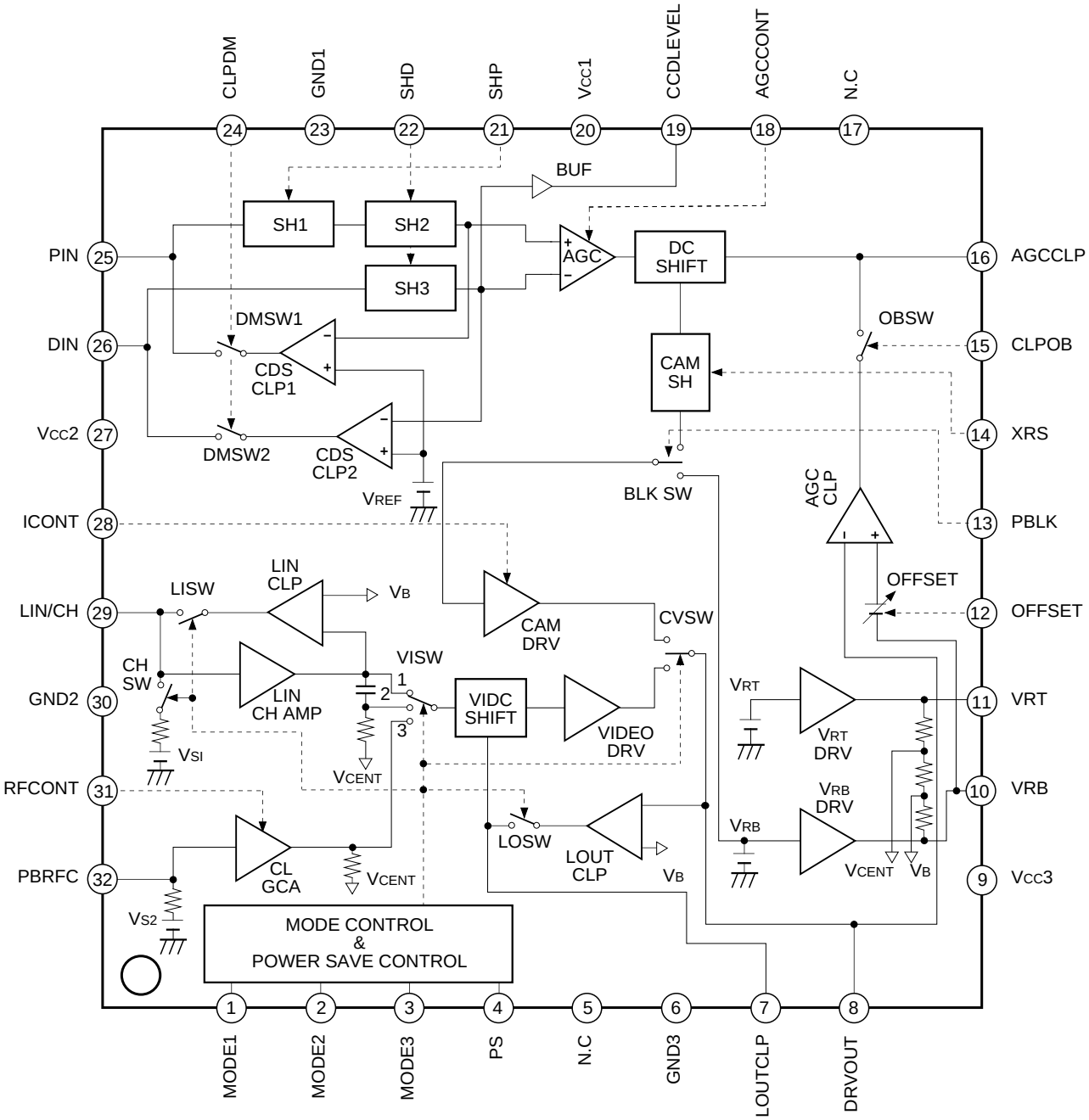
Digital CCD cameras

Structure

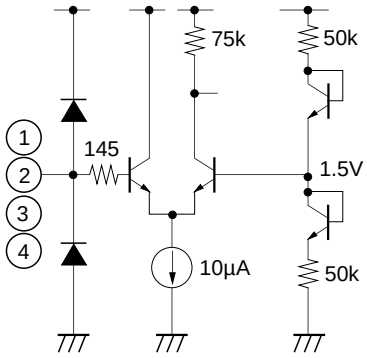
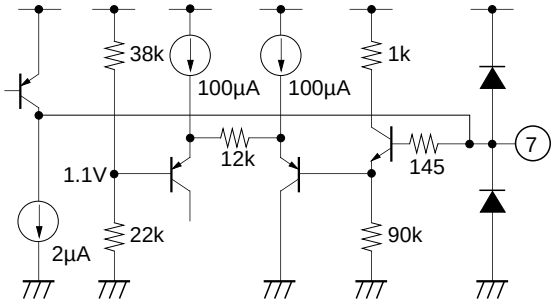
Bipolar silicon monolithic IC

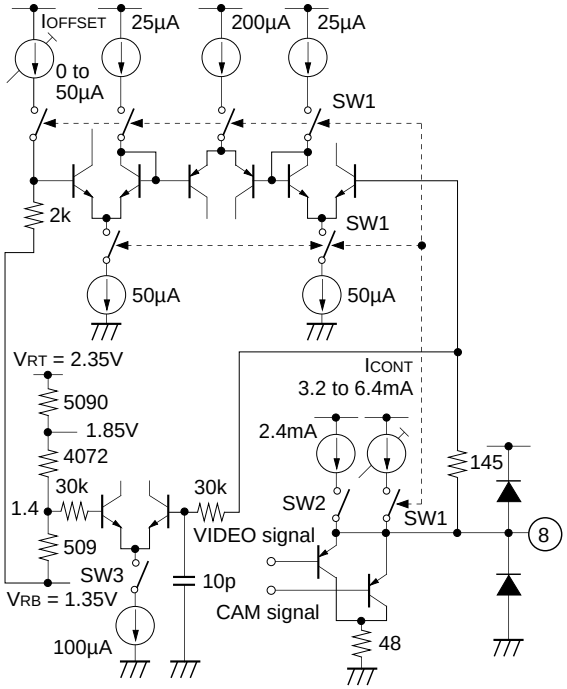
E96119-PS

Block Diagram and Pin Configuration

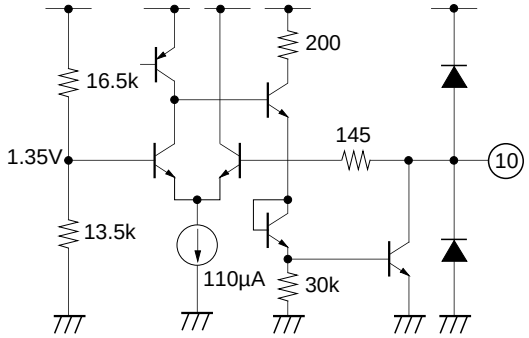
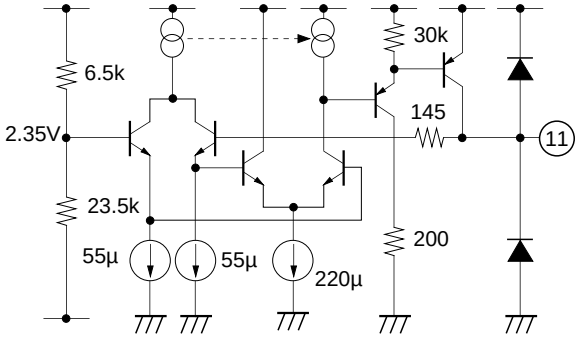


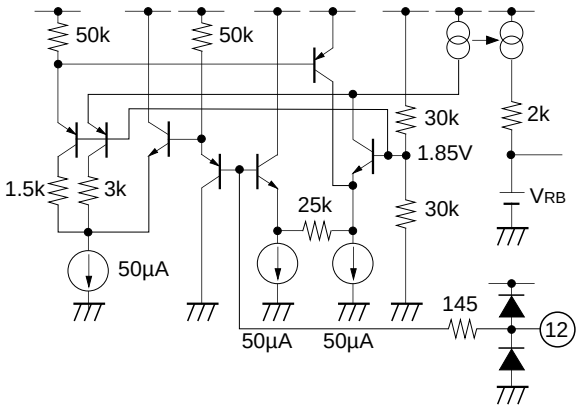
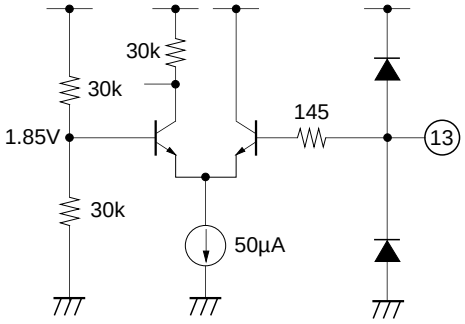
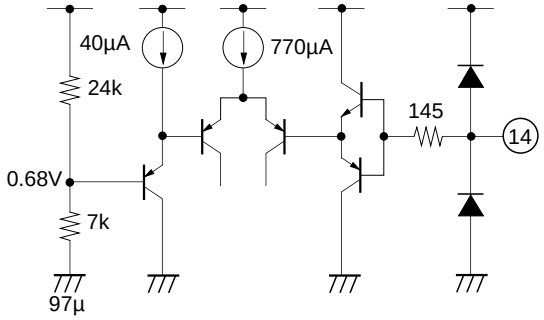
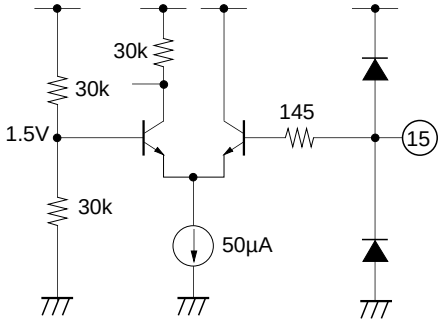
Pin Description (V_{CC}1, 2, 3 = 3V)

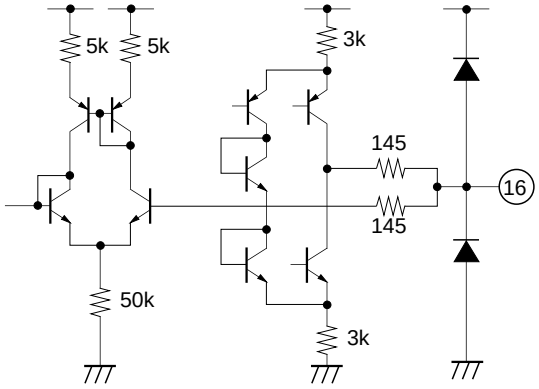
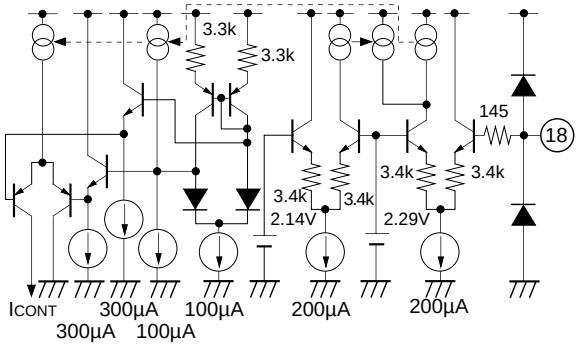
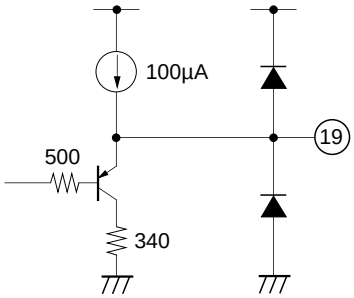
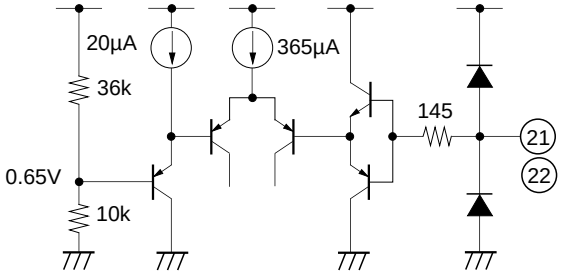
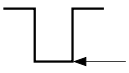
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	MODE1	VTH = 1.5V		Camera and video signal selector. Composite video signal and high-band chroma/low-band chroma signal selector of the video signal. For details on the selection conditions for each mode, refer to the diagram of the Electrical Characteristics Measurement Circuit.
2	MODE2			
3	MODE3			
4	PS			Power saving mode.
5 17	N.C			No connection; normally ground.
6 23 30	GND3 GND1 GND2	GND		Ground.
7	LOUTCLP	Approx. 1.1V		Capacitor connection for LOUTCLP which clamps the output minimum level in modes which pass the composite video signal. (Recommended value: 0.1µF)

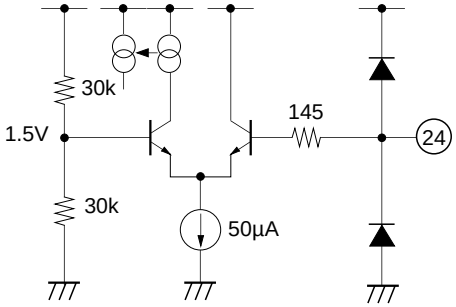
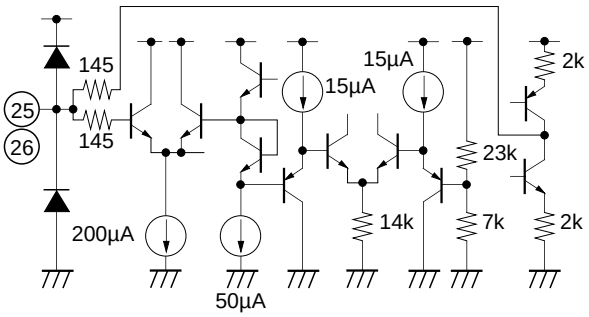
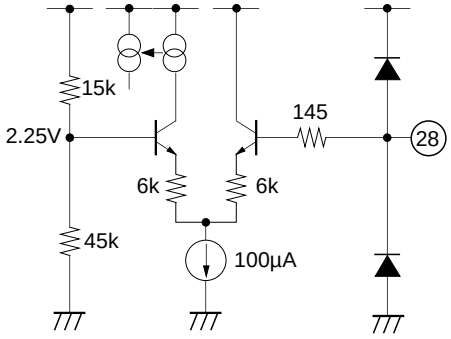
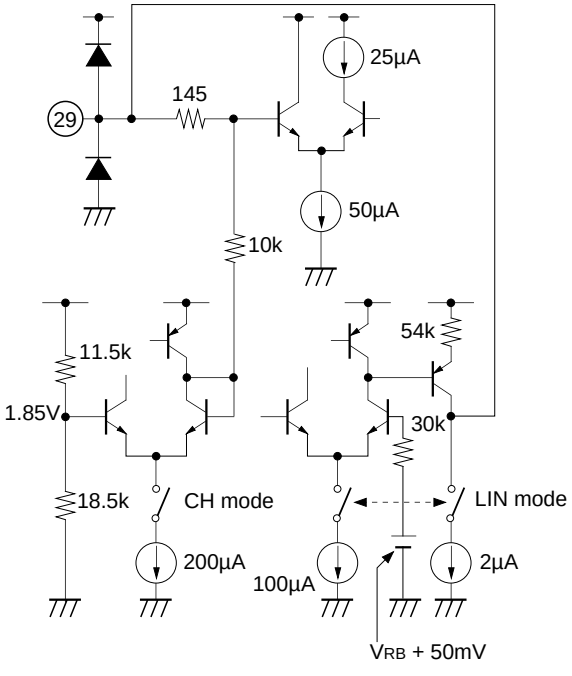
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Pin voltage</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>8</td><td>DRVOUT</td><td>• Camera mode (CAM) V_{RB} to V_{RB} + 100mV
• Composite video mode (LIN) V_{RB} + 50mV = approx. 1.4V
• Chroma mode (CH, CL) Center voltage = (V_{RT} – V_{RB})/2 = approx. 1.85V</td><td> 
</td><td>Driver output for A/D converter capable of DC coupling.

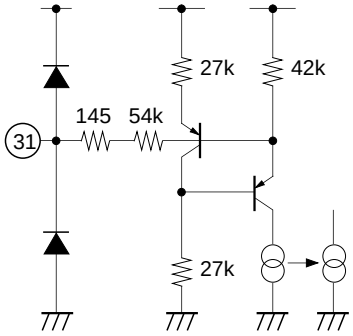
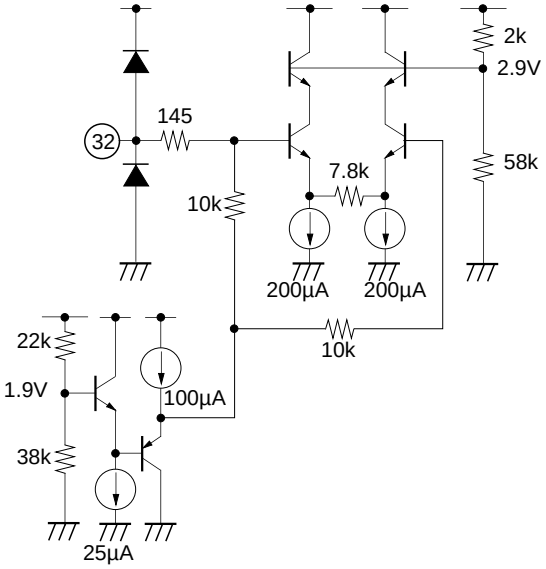
Dynamic range = 1Vp-p

<table>
<tr><th>Mode</th><th>SW1</th><th>SW2</th><th>SW3</th></tr>
<tr><td>CAM</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>LIN</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>CH, CL</td><td>0</td><td>1</td><td>0</td></tr>
</table>
0: Open
1: Closed</td></tr>
<tr><td>9
20
27</td><td>V_{CC}3
V_{CC}1
V_{CC}2</td><td>V_{CC}</td><td></td><td>Power supply.</td></tr>
<tr><td>10</td><td>VRB</td><td>1.35V</td><td> 
</td><td>1.35V regulator output.</td></tr>
<tr><td>11</td><td>VRT</td><td>2.35V</td><td> 
</td><td>2.35V regulator output.</td></tr>
</table>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
12	OFFSET	1.5 to 3V & 0V		Controls the output offset during camera mode. When 3V: V_{RB} When 1.5V: V_{RB} + 100mV When 0V (preset mode): V_{RB} + 35mV
13	PBLK	VTH = 1.85V Active: Low		Camera signal preblanking pulse input. Active when Low only during camera mode. Calibrates the black level of the AGC output waveform. When PBLK is Low, the DRVOUT potential is forced to V_{RB}.
14	XRS	VTH = 0.68V Sampling		Camera signal sample-and-hold pulse input.
15	CLPOB	VTH = 1.5V Active: Low		Clamp pulse used to clamp the optical black portion of the camera signal after it passes through the AGC amplifier.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
16	AGCCLP	Approx. 1.3V		AGC clamp capacitor. (Recommended value: 0.1µF)
18	AGCCONT	1.5 to 3.0V		AGC gain control. When 1.5V: –1dB (Minimum gain) When 3.0V: +31.5dB (Maximum gain)
19	CCDLEVEL	DIN input CCD signal black level: approx. 2.2V		Enables monitoring of the SH3 output camera signal.
21	SHP	VTH = 0.65V		Preset level sample-and-hold pulse input.
22	SHD			Data level sample-and-hold pulse input.

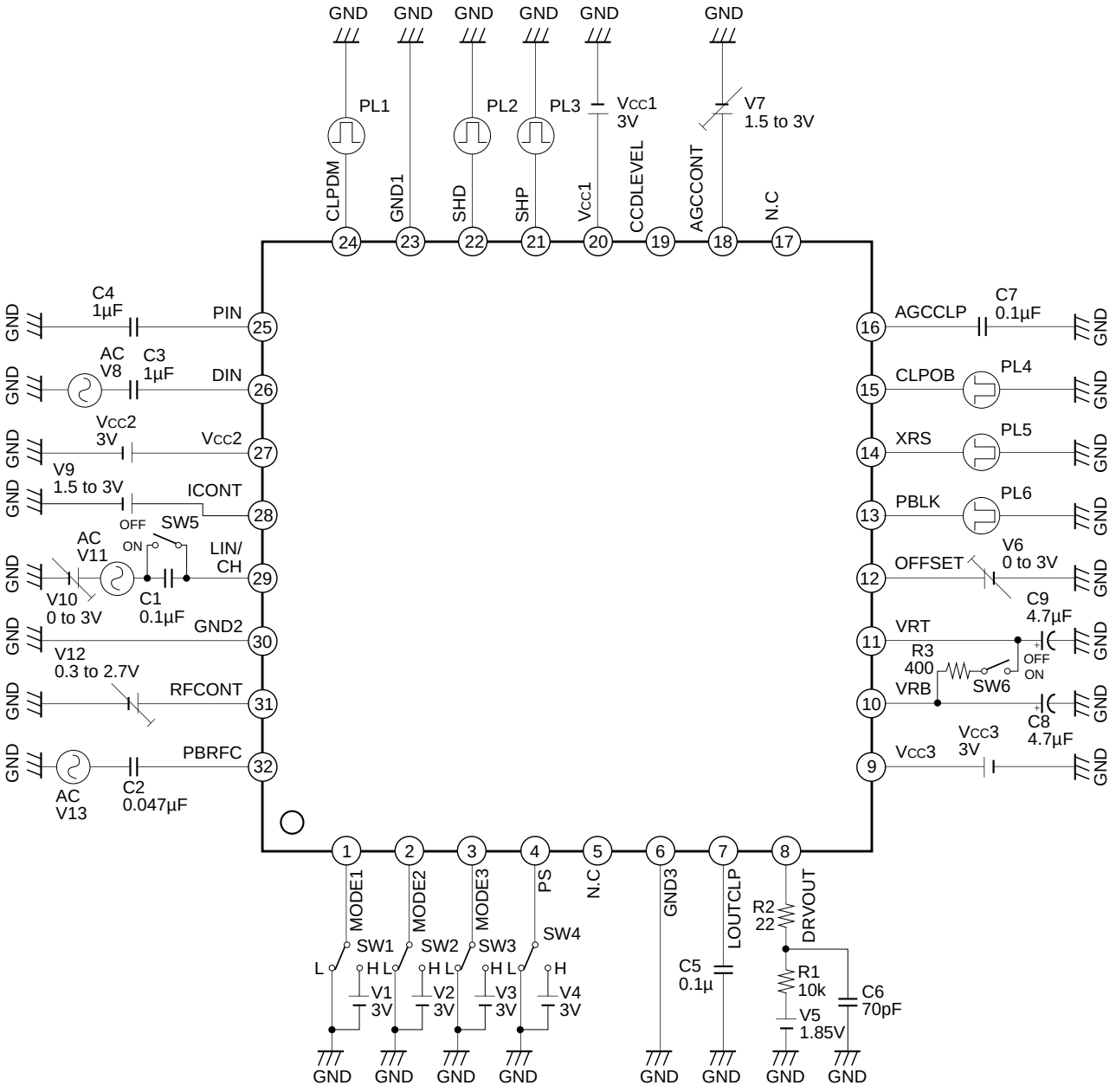
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
24	CLPDM	VTH = 1.5V  Active: Low		Clamp pulse used to clamp the dummy pixel portion of the input CCD signal.
25 26	PIN DIN	Black level: approx. 2.1V		CCD signal input.
28	ICONT	1.5 to 3V		DRVOUT output waveform rise time control. When 1.5V: Maximum rise time When 3V: Minimum rise time
29	LIN/CH	Clamp potential during LIN mode: approx. 1.46V During CH mode: approx. 1.85V		Common input for the composite video signal (LIN) and high-band chroma signal (CH).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
31	RFCONT	0.3 to 2.7V		Gain control for the low-band chroma signal (CL). When 0.3V: –4dB (Minimum gain) When 2.7V: +12.5dB (Maximum gain)
32	PBRFC	Approx. 1.9V		Low-band chroma signal (CL) input.

Electrical Characteristics (Ta=25°C, V_{CC}1, 2, 3 = 3V)

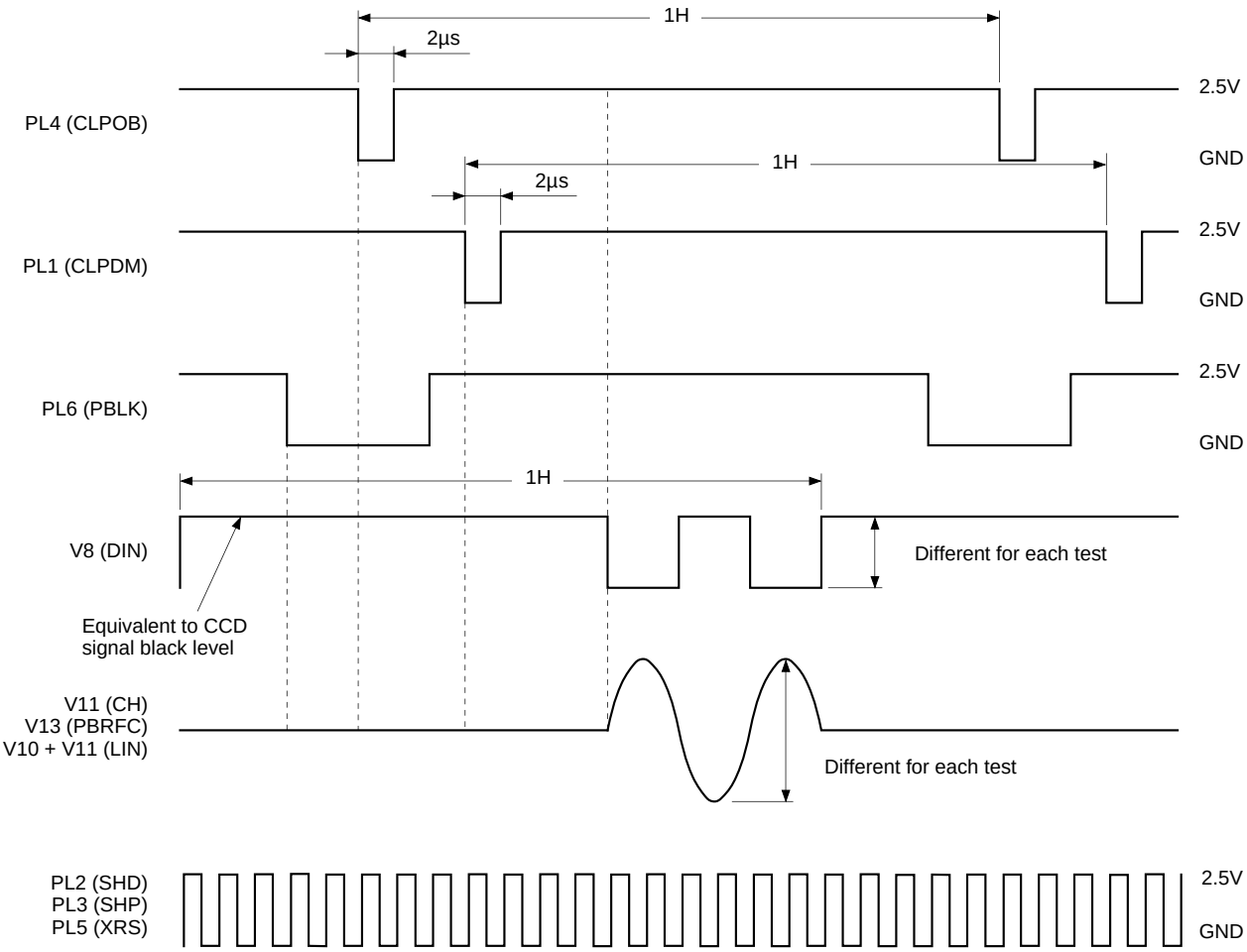
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	Camera mode	I_{DC}	AGCCONT = 1.5V, open between V_{RT} and V_{RB} MODE1 = 3V, MODE2 = 0V MODE3 = 0V, PS = 3V, I_{CONT} = 3V	30	41.0	53	mA
	LINE mode	I_{DL}	Open between V_{RT} and V_{RB} MODE1 = 0V, MODE2 = 0V, MODE3 = 0V, PS = 3V	10	13.9	19	
	CH mode	I_{DCH}	Open between V_{RT} and V_{RB} MODE1 = 0V, MODE2 = 3V, MODE3 = 3V, PS = 3V	9	12.2	17	
	CL mode	I_{PCL}	RFCONT = 0.3V, open between V_{RT} and V_{RB} MODE1 = 0V, MODE2 = 3V, MODE3 = 0V, PS = 3V	9	12.2	17	
	PS mode	I_{DP}	PS = 0V	2	3.4	6	
AGC	Maximum gain	A CONT max.	DIN = 1µs, 20mVp-p pulse AGCCONT = 3V, I_{CONT} = 3V	28.5	31.3	—	dB
	Minimum gain	A CONT min.	DIN = 1µs, 500mVp-p pulse AGCCONT = 1.5V, I_{CONT} = 3V	—	–0.8	1.4	
	Range of gain variance	AGC G	A CON max. – A CON min.	27.1	32.1	—	
	Dynamic range maximum	AGCmax. D	AGCCONT = 3V DRVOUT output signal at saturation level	800	895	—	mV
	Dynamic range typical	$AGC_{TYP.}$ D	AGCCONT = 2V DRVOUT output signal at saturation level	900	955	—	
DRV	Offset high	CAOF high	Camera mode OFFSET = 1.5V	80	98	—	mV
	Offset low	CAOF low	Camera mode OFFSET = 3.0V	—	2	5	
	Offset preset	CAOF pre	Camera mode OFFSET = 0V	25	34	40	
REF	V_{RT} DC level	VRTO	With a 400Ω load	2300	2342	2400	mV
	V_{RB} DC level	VRBO	With a 400Ω load	1300	1359	1400	
	$V_{RT} – V_{RB}$	ΔVR	With a 400Ω load	950	983	1050	
BLK	Offset	BLKOF	BLKOF (PBLK = 3V) – BLKOF (PBLK = 0V)	—10	9	23	mV
AMP	LIN mode gain	LIN G	LIN/CH = 15kHz, 500mVp-p, Sine wave + offset voltage	2.5	3.43	4.5	dB
	CH mode gain	CH G	LIN/CH = 3MHz, 500mVp-p, sine wave	2.5	3.18	4.5	
GCA	CL mode maximum gain	RF CONmax.	RFCONT = 2.7V 15kHz 80mVp-p sine wave	9.5	12.7	—	
	CL mode minimum gain	RF CONmin.	RFCONT = 0.3V 15kHz 500mVp-p sine wave	—	–4.0	–2.5	
SH3	Dynamic range	SH3 D	DIN = 1µs, 1Vp-p pulse	600	815	—	mV

Electrical Characteristics Measurement Circuit

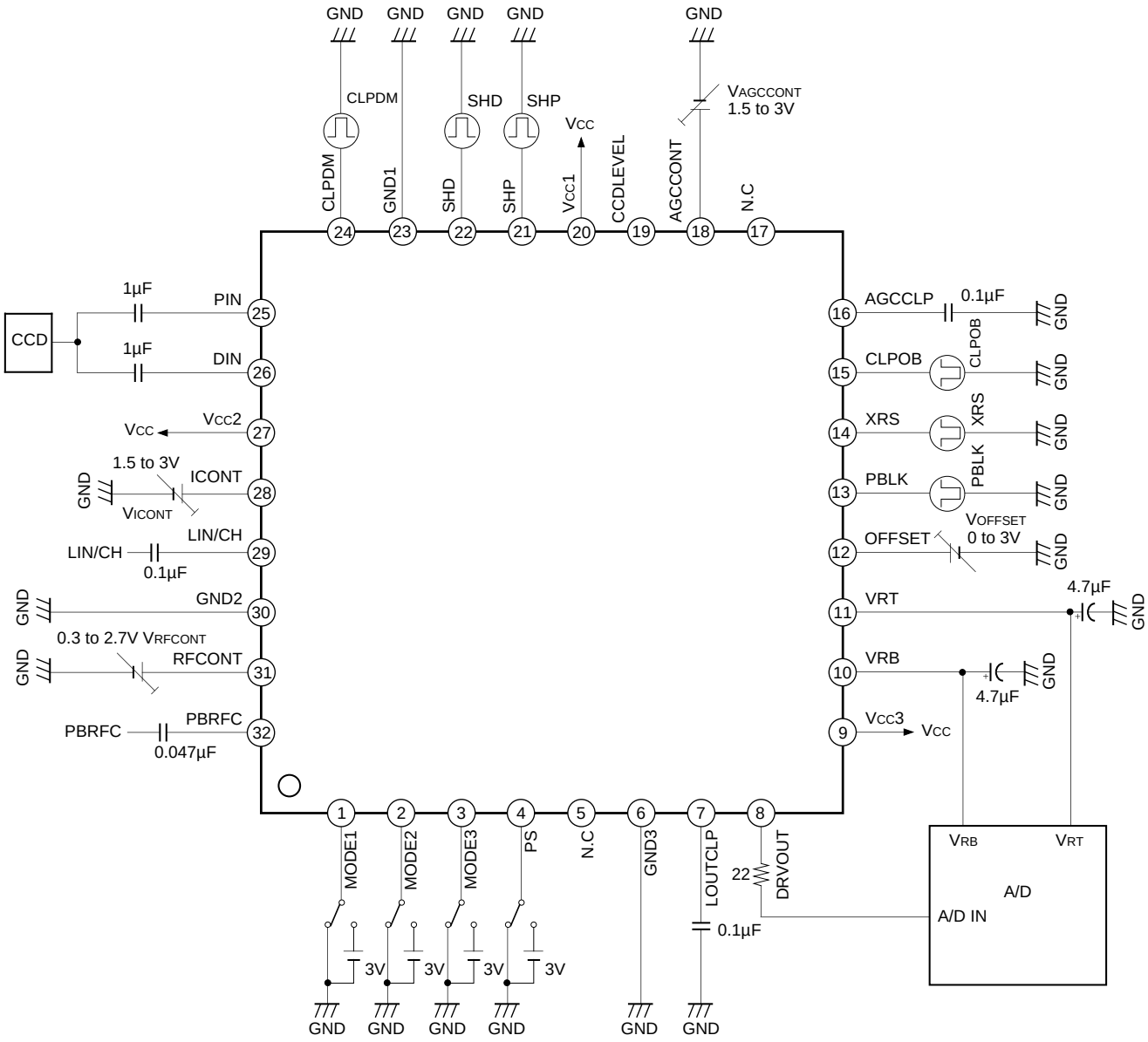


SW1	SW2	SW3	SW5	SW4	MODE
L	L	H	OFF	H	CAM
H	L	L			
H	L	H	ON		LIN
L	L	L			
H	H	L	OFF		CL
L	H	L			
L	H	H			CH
				L	POWER SAVE

Measurement Timing Chart



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

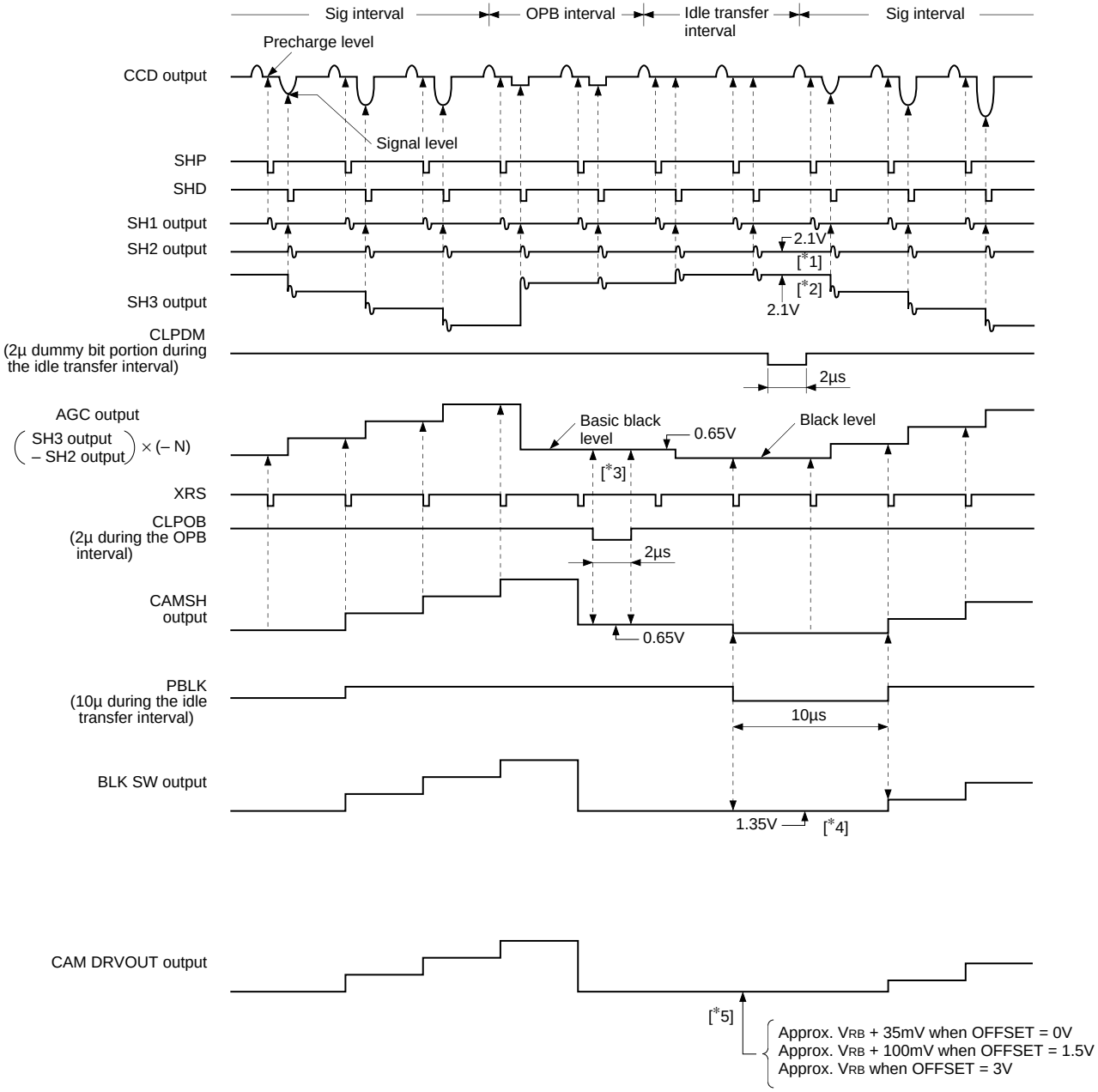
Refer to the Block Diagram.

1. Camera signal processing system

Operating conditions

The camera signal processing system operates when PS is High, MODE1 is Low, MODE2 is Low and MODE3 is High, or when PS is High, MODE1 is High, MODE2 is Low and MODE3 is Low.

Camera signal processing system timing chart (when V_{CC} = 3V)



CDS (SH1, SH2, SH3):
The CCD signal from the CCD image sensor is input to PIN and DIN where correlated double sampling (CDS) is performed by SH1, SH2 and SH3. The precharge level of the CCD output signal is sampled, held and output by the SH2 output, and the signal level is sampled, held and output by the SH3 output. SH1 and SH2 are the sample-and-hold circuits for the pre-charge level; SH3 is the sample-and-hold circuit for the signal level.

CDSCLP 1, 2:
CDSCLP1 and 2 stabilize the input signal DC level, clamp (CLPDM) the input signal during the idle transfer interval for the purpose of eliminating the AGC input offset, and adjust the DC level ([*1], [*2]) of SH2 and SH3 in line with V_{REF}. CDSCLP1 is the clamp circuit for the precharge level, and CDSCLP2 is the clamp circuit for the signal level.

AGC:
AGC is the gain control amplifier for the camera signal.
The gain can be varied from –1 to +31dB by adjusting the AGCCONT voltage control $V_{AGCCONT}$ from 1.5 to 3.0V.

CAM SH:
CAM SH is the sample-and-hold circuit for the camera signal processing system; it synchronizes the data read-in timing for the external A/D.
Sampling is possible according to the approximately 10ns sampling pulse width input to XRS.

AGCCLP:
The basic black level is set ([*3]) by clamping the AGC output waveform with the CLPOB clock during the OPB interval. When PBLK is High and CLPOB is Low, the clamping circuit operates, adjusting the AGCCLP current so that the DRVOUT potential equals the OFFSET potential (which is determined by the voltage applied to the OFFSET pin), thus setting the AGCCLP potential. The AGCCLP capacitance is connected to the AGCCLP pin.

DC SHIFT:
This circuit functions when AGCCLP operates, following the AGCCLP potential and forcing a DC shift of the AGC output waveform OPB interval to the basic black level. When AGCCLP is not operating, the basic black level is maintained at its previous setting.

BLK SW:
The black level is calibrated by blanking the black level signal of the AGC output waveform so that it does not fall below the basic black level and replacing the DC potential with V_{RB}. ([*4])
The signal is blanked when PBLK is low.

CVSW:
When the MODE1, 2, 3 and PS pin voltages are set so that the camera signal processing system operates, CVSW conducts the CAMDRV output (camera signal) into the DRVOUT. In addition, when these voltages are set so that the video signal processing system operates, CVSW conducts the VIDEODRV output (video signal) into the DRVOUT.

OFFSET:
OFFSET controls the CAMDRV output waveform black level offset.
In the camera signal processing system camera mode, the OFFSET pin is enabled, permitting adjustment of the offset for the [OFFSET] and DRVOUT camera signals. ([*5]) The voltage controlled by OFFSET is output as the CAMDRV output DC offset via AGCLP, DCSHIFT, CAMSH, and BLKSW.
When the OFFSET voltage is 1.5 to 3.0V, DRVOUT DC can vary in a linear fashion from V_{RB} + 100mV to V_{RB}.
In addition, when the OFFSET voltage is 0V, DRVOUT DC is preset to V_{RB} + 35mV.

CAMDRV:
CAMDRV operates in the camera signal processing system mode, driving the external A/D. The current that flows to the last-stage amplifier in CAMDRV is controlled by applying voltage to the ICONT pin, making it possible to adjust the rise time of the output waveform, which affects the external A/D load capacitance. The variable range is 1.5 to 3V, with 1.5V yielding the maximum and 3V yielding the minimum. The optimum rise time for the external A/D input capacitance can be selected.

V_{RT} DRV, V_{RB} DRV:
These are the external A/D reference voltage drivers. These circuits are connected to A/D V_{RT} and V_{RB}, supplying 2.35V and 1.35V, respectively, when V_{CC} is 3V. The IC's internal primary voltage is also generated on the basis of the V_{RT} and V_{RB} voltages. (V_{RB}, V_B, and V_{CENT})

MODE CONTROL & POWER SAVE CONTROL:
This block selects the mode governing the operation of the camera signal system and the video signal system through the selection of High and Low potential for the MODE1, 2, 3, and PS pins. The PS pin is the POWER SAVE pin; the power saving function operates when this pin is Low.

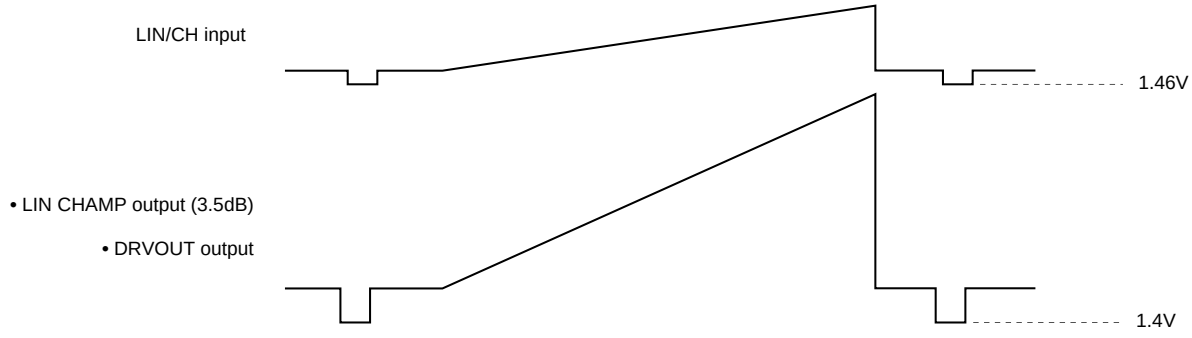
2. Video signal processing system

Operating conditions

The video signal processing system has three modes: LIN signal mode, CH signal mode and CL signal mode.
The video signal processing system operates in LIN signal mode when PS is High, MODE1 is High, MODE2 is Low and MODE3 is High, or when PS is High, MODE1 is Low, MODE 2 is Low and MODE3 is Low.
The video signal processing system operates in CH signal mode when PS is High, MODE1 is Low, MODE2 is High and MODE3 is High.
The video signal processing system operates in CL signal mode when PS is High, MODE1 is Low, MODE2 is High and MODE3 is Low, or when PS is High, MODE1 is Low, MODE2 is High and MODE3 is High.

Video signal processing system timing chart (when V_{CC} = 3V)

LIN mode



LIN signal mode

In LIN signal mode, LINSW and LOSW close, VISW is set to “1” and the video signal passes through CVSW. In addition, LINCHAMP, LINCLP, LOUTCLP, VIDC SHIFT, and VIDEO DRV all operate.

LINCLP:

LINCLP is an input clamp circuit that clamps the video composite signal sync level.

The video composite signal is input to LIN/CH pin. LINCLP expands the input dynamic range, and sync tip clamps the input signal at V_B (= 1.4V) to allow full input. The input level and frequency are respectively 571mVp-p (Max.) and DC is up to 7MHz.

LINCHAMP:

LINCHAMP amplifies the LIN signal and the CH (high-band chroma) signal; the gain is fixed at 3.5dB.

VISW:

VISW switches the LIN signal, the CH (high-band chroma) signal, and the CL (low-band chroma) signal. The signals are switched according to the mode selection.

LOUTCLP:

LOUTCLP is an output clamp circuit that clamps the sync level of the video composite signal that is output from VIDEO DRV.

Because the VIDEO DRV output signal is fully input to the external A/D, the clamp level is set to V_B (= 1.4V).

If the sync level of the signal output from VIDEO DRV drops below V_B, LOUTCLP operates: the LOUTCLP current flows so that the sync level equals V_B, and the LOUTCLP potential is set. A clamping capacitor is connected to the LOUTCLP pin.

VIDC SHIFT:

VIDC SHIFT functions when LOUTCLP operates, following the LOUTCLP potential and forcing a DC shift of the VIDEO output signal sync level to V_B.

VIDEO DRV:

VIDEO DRV outputs the video signal (LIN, CH, CL) to the external A/D in video signal processing mode.

CH (high-band chroma) signal mode

In CH mode, CHSW closes, VISW is set to “2” and the video signal passes through CVSW. In addition, LINCHAMP and VIDEO DRV operate.

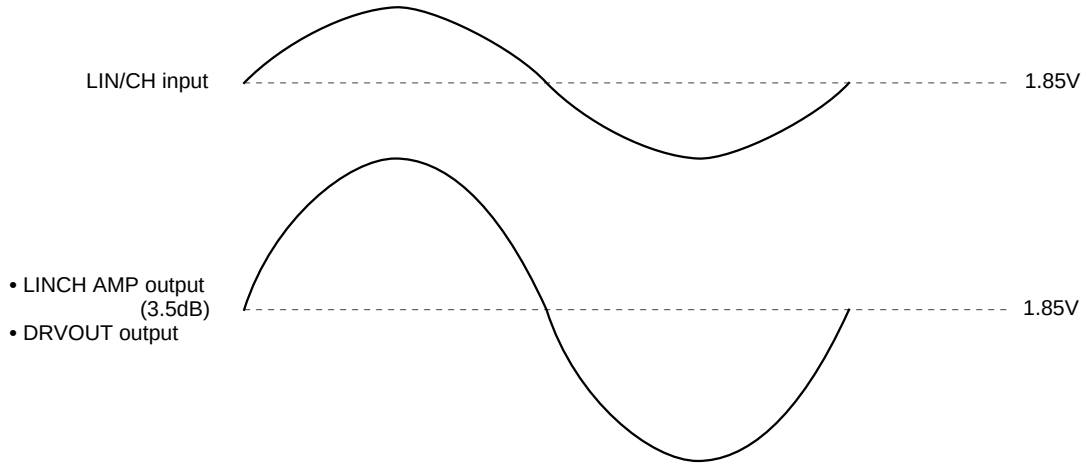
V_{S1}:

The video high-band chroma signal is input to the LIN/CH pin. V_{S1} expands the input dynamic range and sets a center DC bias so that the center potential of the SIN signal is 1.85V to allow full input. The input level and frequency of the CH signal are respectively 470mVp-p (Max.) and from 1 to 7MHz.

V_{CENT}:

V_{CENT} is a DC bias circuit that operates when the CH signal is output to VIDEO DRV. The DC bias potential is generated from V_{RT} and V_{RB}, and is set to 1.85V.

CH mode



CL (low-band chroma) signal mode

In CL mode, VISW is set to “3” and the video signal passes through CVSW. In addition, CLGCA and VIDEO DRV operate.

V_{S2}:

The video low-band chroma signal is input to the PBRFC pin. V_{S2} expands the input dynamic range and sets a center DC bias so that the center potential of the SIN signal is 1.9V to allow full input. The input level and frequency of the CH signal are respectively 1490mVp-p (Max.) and DC is up to 1.5MHz.

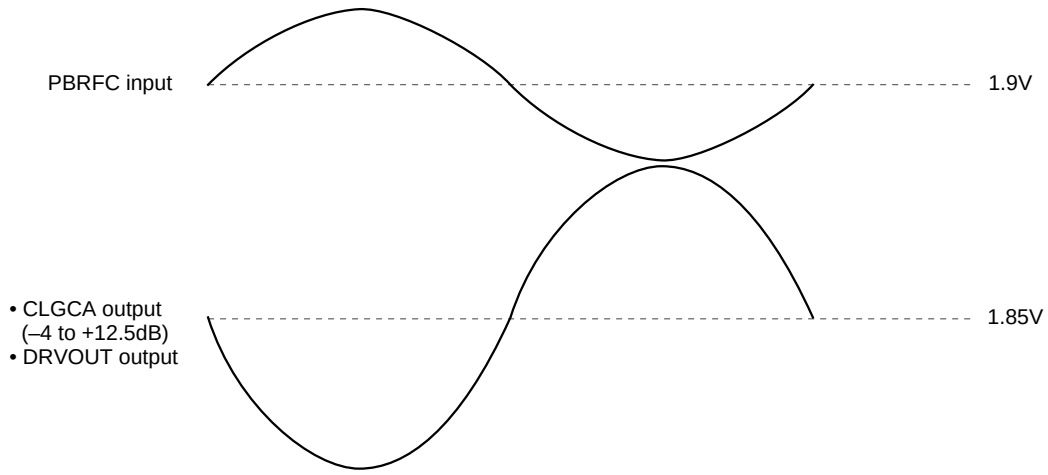
CLGCA:

The CLGCA amplifier controls the gain of the CL signal input to the PBRFC pin. The gain can be varied from –4 to +12.5dB by adjusting the RFCONT voltage from 0.3 to 2.7V. The phase of the CLGCA output waveform is reversed in DRVOUT.

V_{CENT}:

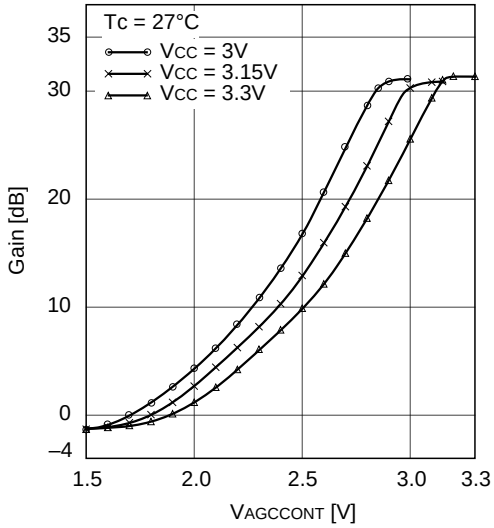
V_{CENT} is a DC bias circuit that operates when the CL signal is output to VIDEO DRV. The DC bias potential is generated from V_{RT} and V_{RB}, and is set to 1.85V.

CL mode

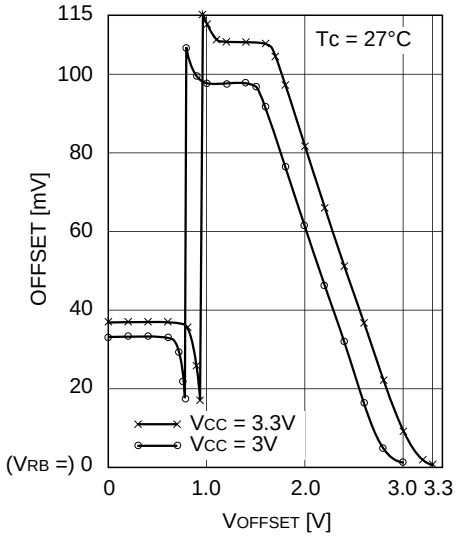


Example of Representative Characteristics

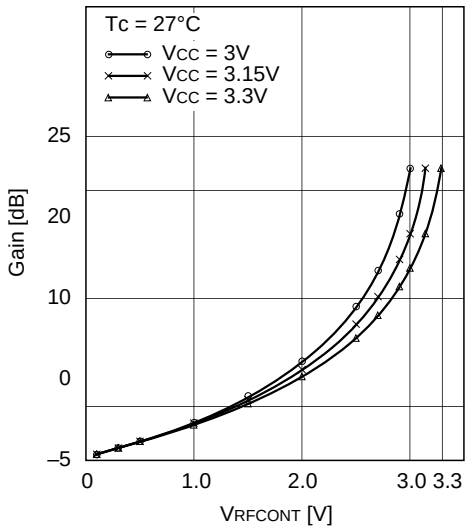
CAM mode AGCCONT control supply voltage characteristics
$V_{AGCCONT}$ vs. Gain



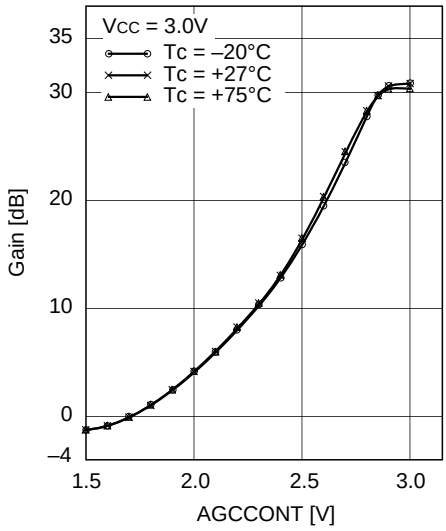
CAM mode OFFSET control supply voltage characteristics
V_{OFFSET} vs. OFFSET



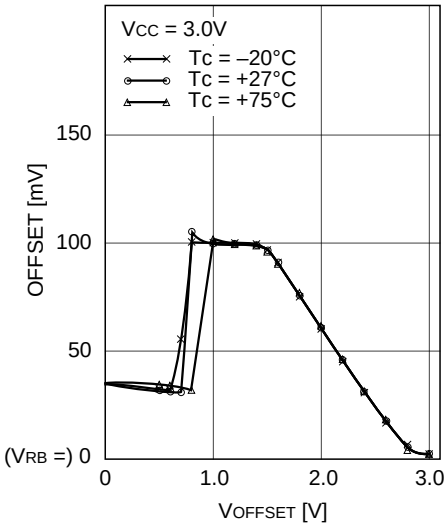
CL mode RFGCA gain control supply voltage characteristics
V_{RFCONT} vs. Gain



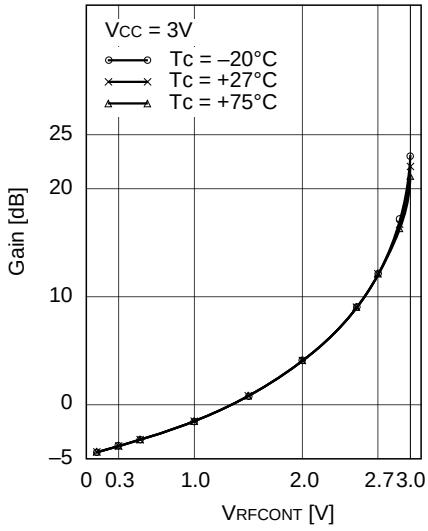
CAM mode AGCCONT control temperature characteristics
AGCCONT vs. Gain



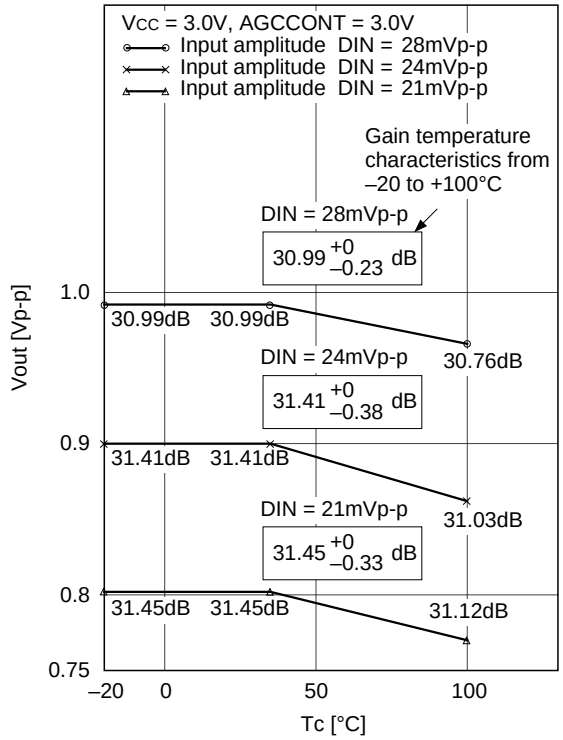
CAM mode OFFSET control temperature characteristics
VOFFSET vs. OFFSET



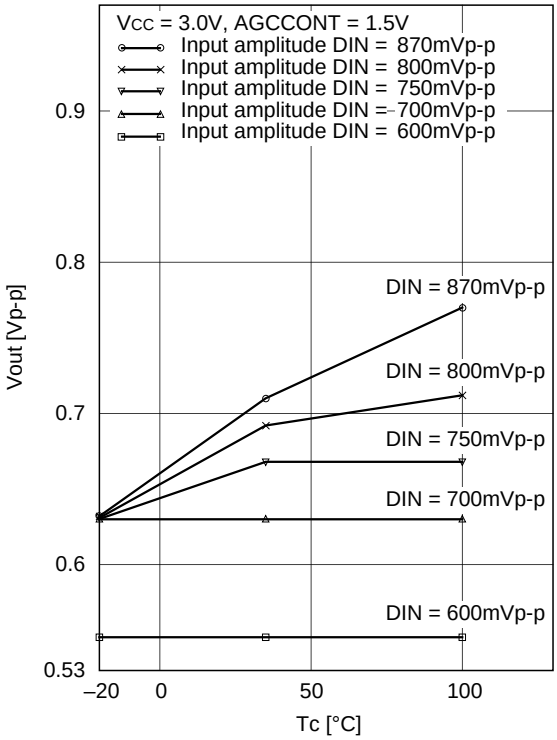
CL mode RFGCA gain control temperature characteristics
VRFCONT vs. Gain



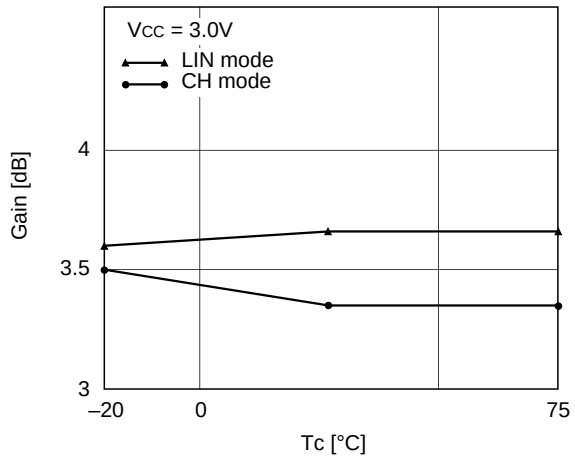
CAM mode maximum signal amplitude temperature characteristics (Max. gain) Tc vs. Vout



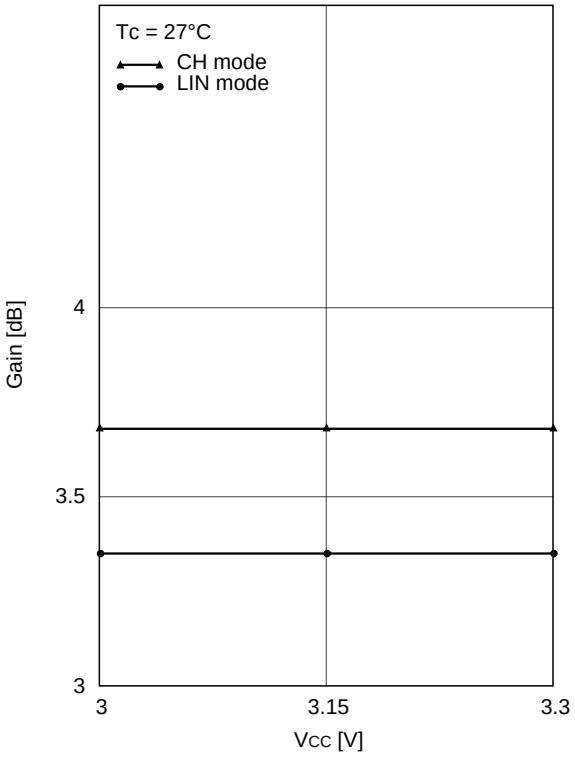
CAM mode maximum signal amplitude temperature characteristics (Min. gain) Tc vs. Vout



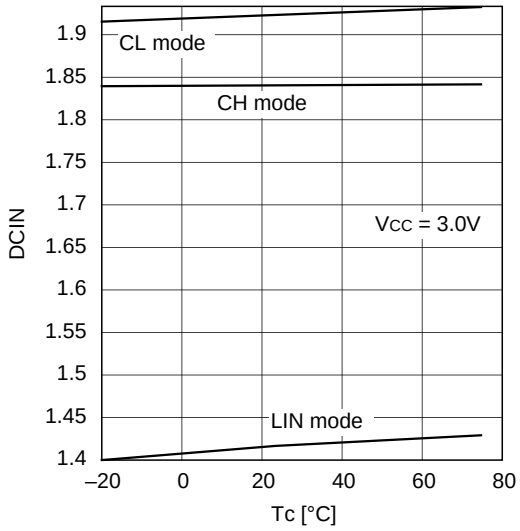
LIN, CH mode LINCHAMP gain temperature characteristics Tc vs. Gain



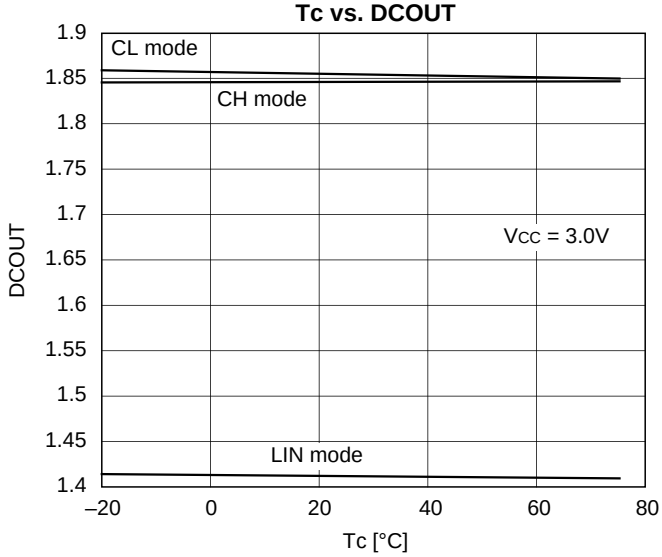
LIN, CH mode LINCHAMP gain supply voltage characteristics Vcc vs. Gain



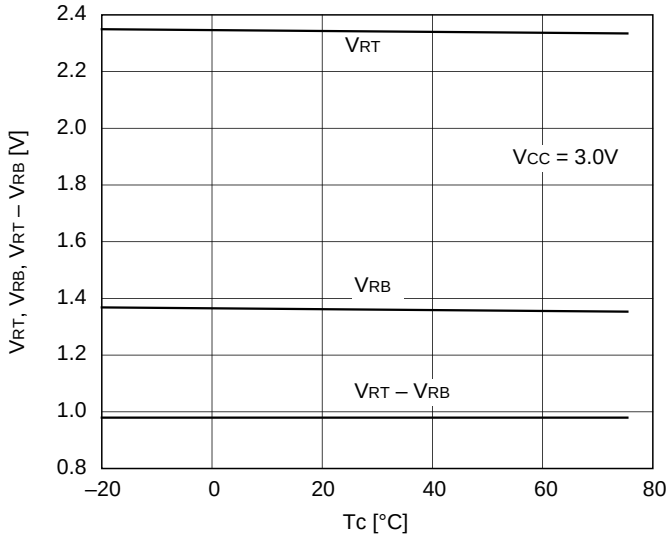
CH, LIN, CL mode input pin DC voltage temperature characteristics
Tc vs. DCIN



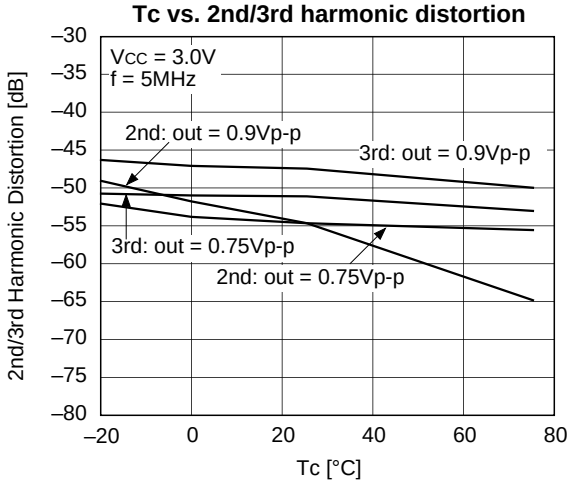
CH, LIN, CL mode DRVOUT output DC voltage temperature characteristics
Tc vs. DCOUT



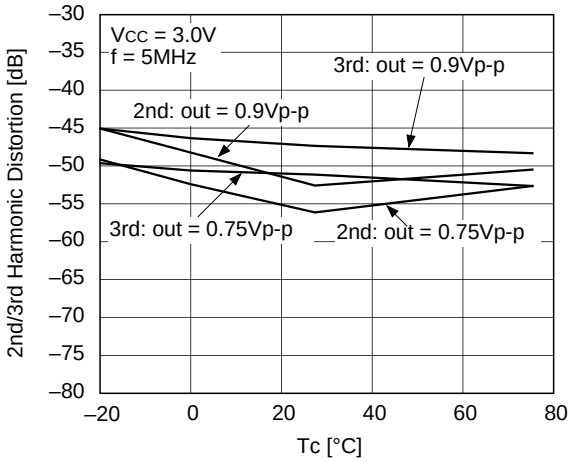
VRT, VRB, VRT – VRB temperature characteristics
Tc vs. VRT, VRB, VRT – VRB



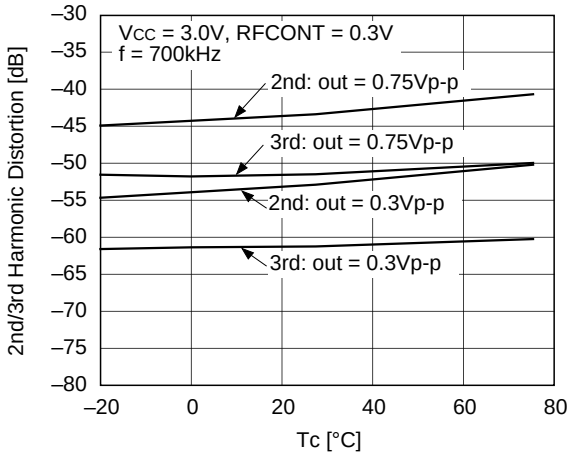
LIN mode 2nd/3rd harmonic distortion temperature characteristics
Tc vs. 2nd/3rd harmonic distortion



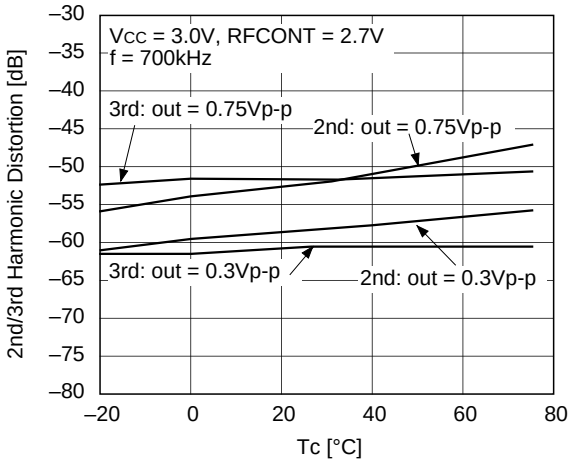
CH mode 2nd/3rd harmonic distortion temperature characteristics
Tc vs. 2nd/3rd harmonic distortion



CL mode 2nd/3rd harmonic distortion temperature characteristics (Min. gain)
Tc vs. 2nd/3rd harmonic distortion

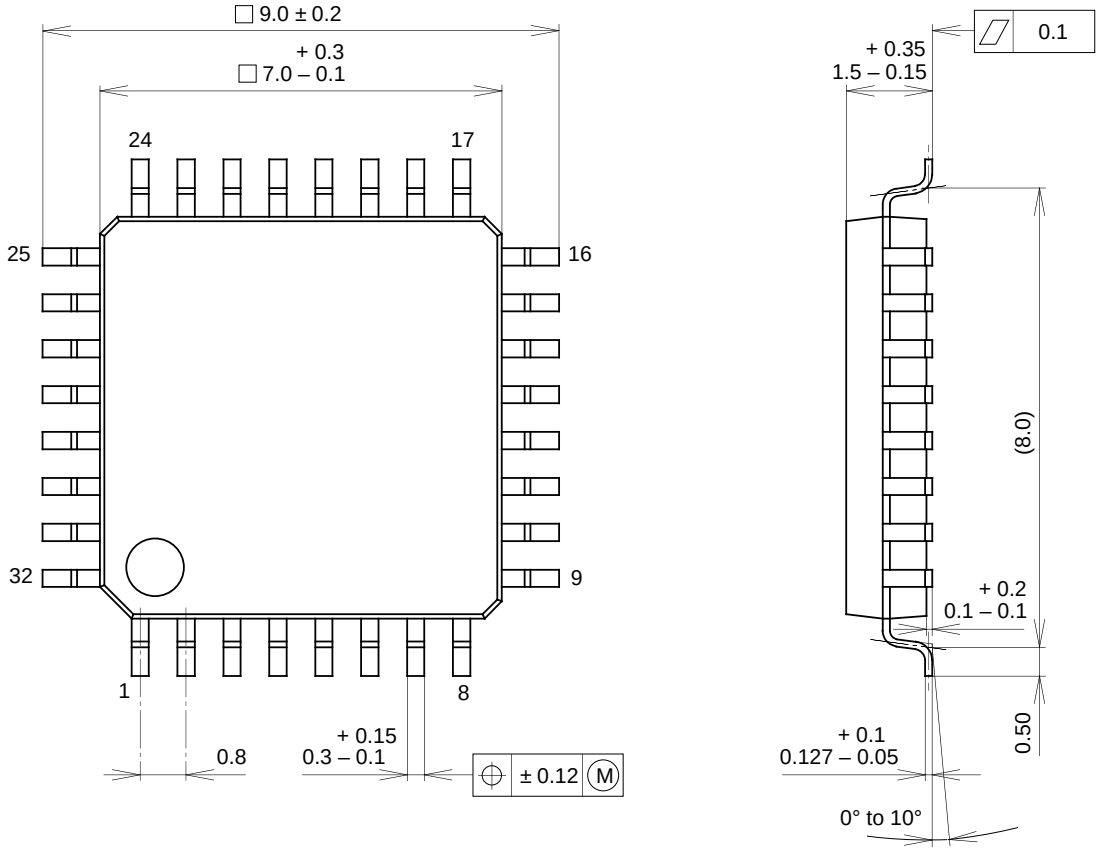


CL mode 2nd/3rd harmonic distortion temperature characteristics (Max. gain)
Tc vs. 2nd/3rd harmonic distortion



Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	∗QFP032-P-0707-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g