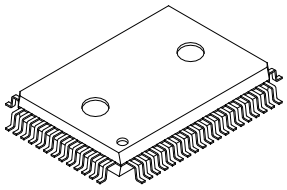
SONY

CXA2078Q

I²C Bus-Compatible Audio/Video Switch with Electronic Volume

64 pin QFP (Plastic)



Description

The CXA2078Q is an I²C programmable audio, video switch designed for set top box applications. It interfaces from digital encoder sources to TV, VCR and auxilliary scart connectors.

Features

- 3 scart independent audio/video switching (TV, VCR, AUX)
- 0 to –63dB volume control with click noise reduction
- 5 stereo audio inputs
- I²C control with two address setting
- Scart Function Switching input and output
- Scart Fast Blanking for OSD
- RF modulator output with Y/C mix option
- On-chip +12V to +9V voltage regulator
- 4 logic outputs

Applications

Audio/Video switch featuring I²C bus compatibility for set top box

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

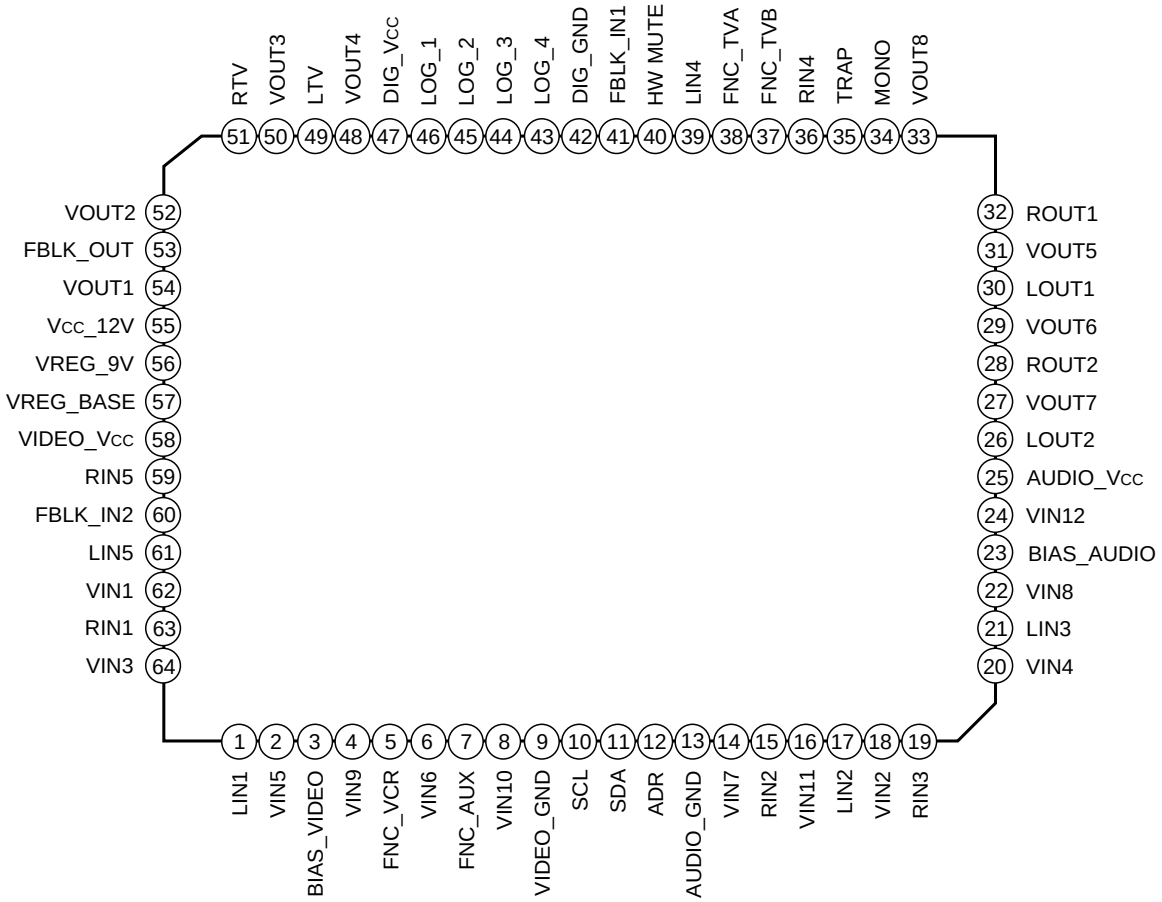
• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	500	mW

Operating Conditions

• Supply voltage	+10.7 to +12	V
• Operating voltage	9 ± 0.5	V

E97843-PS

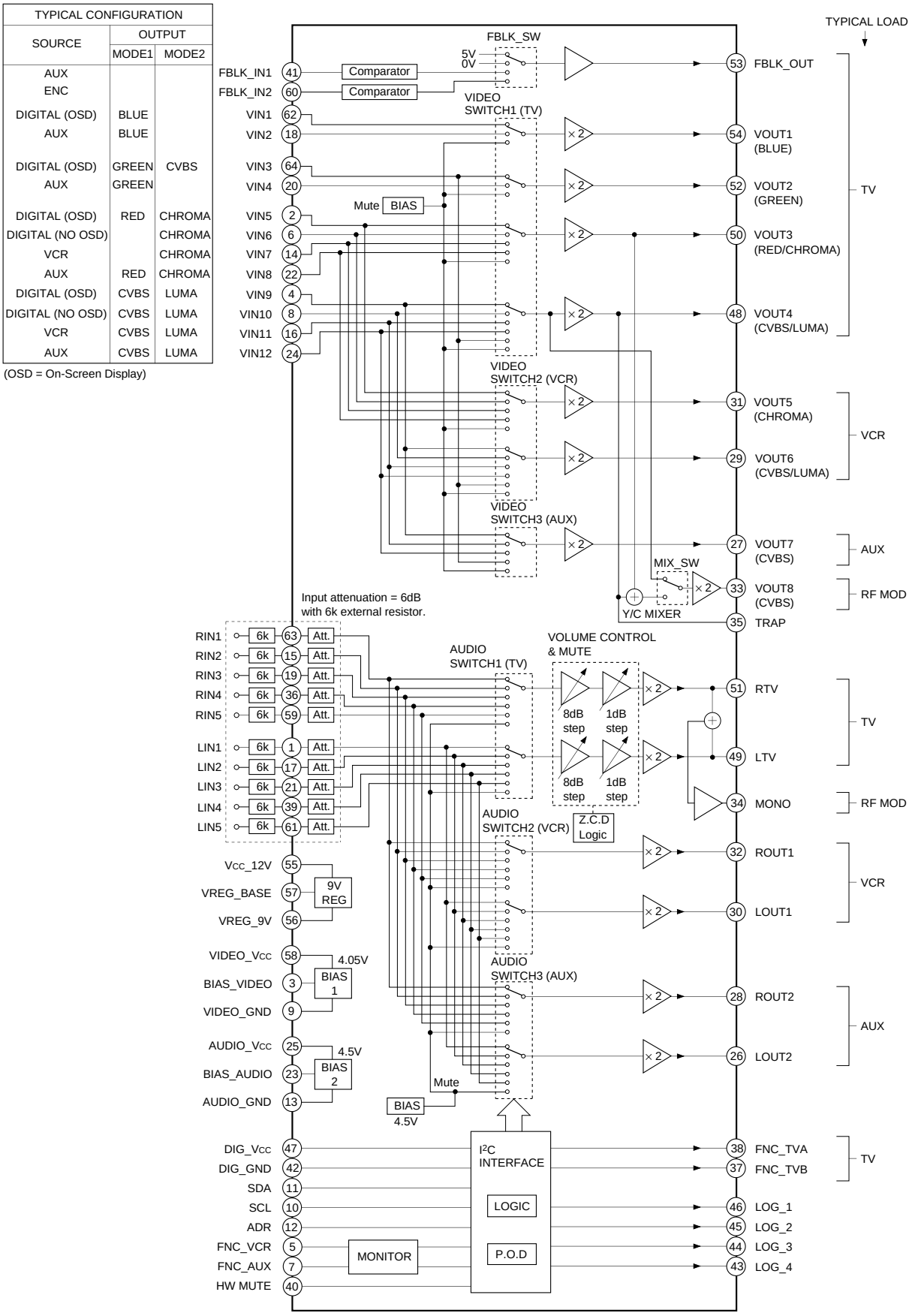
Pin Configuration



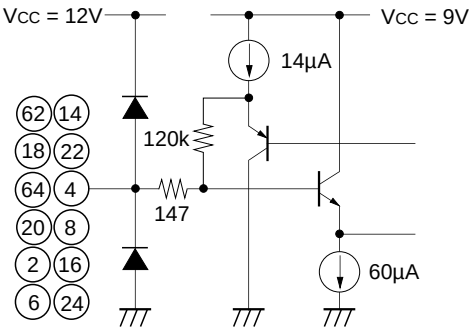
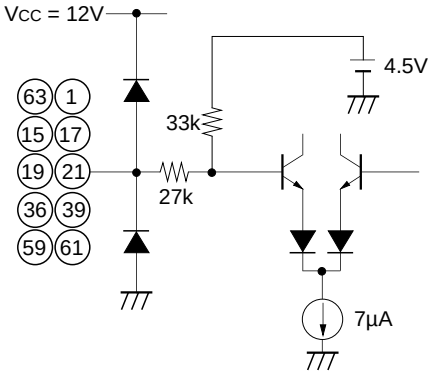
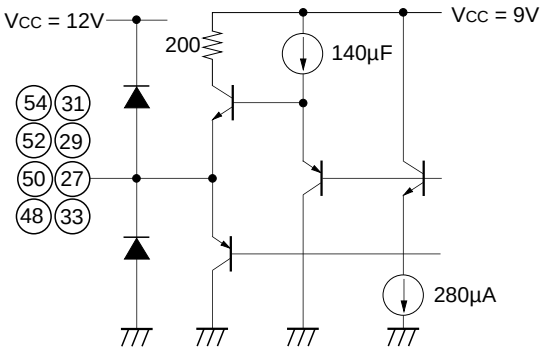
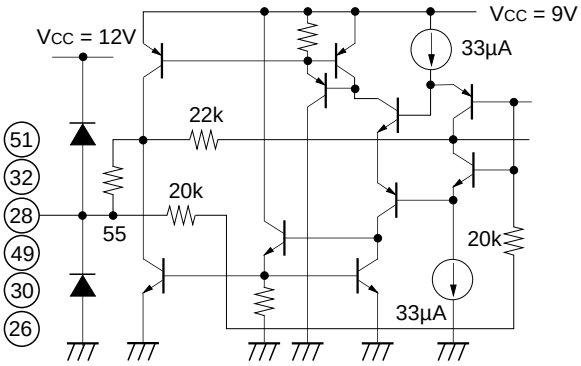
Block Diagram

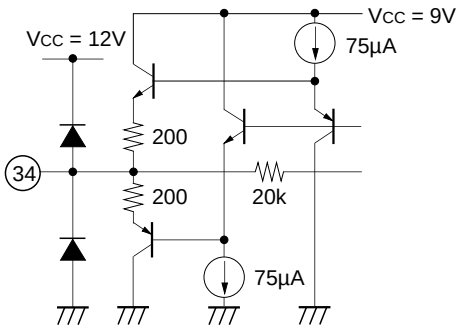
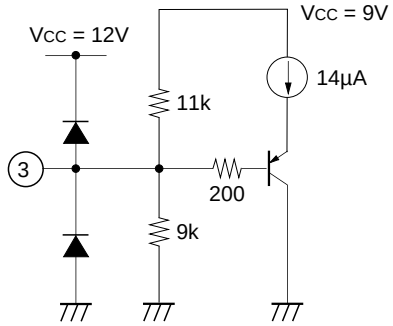
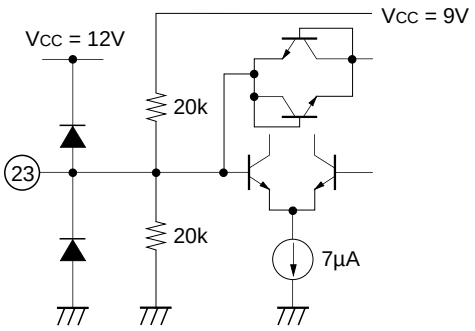
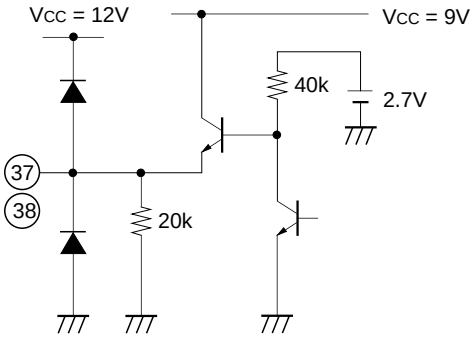
TYPICAL CONFIGURATION		
SOURCE	OUTPUT	
	MODE1	MODE2
AUX		
ENC		
DIGITAL (OSD)	BLUE	
AUX	BLUE	
DIGITAL (OSD)	GREEN	CVBS
AUX	GREEN	
DIGITAL (OSD)	RED	CHROMA
DIGITAL (NO OSD)		CHROMA
VCR		CHROMA
AUX	RED	CHROMA
DIGITAL (OSD)	CVBS	LUMA
DIGITAL (NO OSD)	CVBS	LUMA
VCR	CVBS	LUMA
AUX	CVBS	LUMA

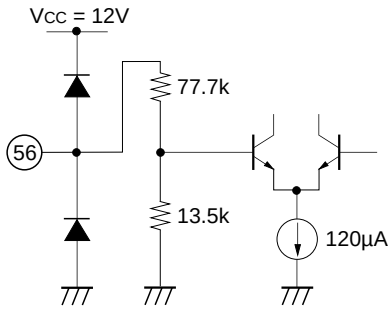
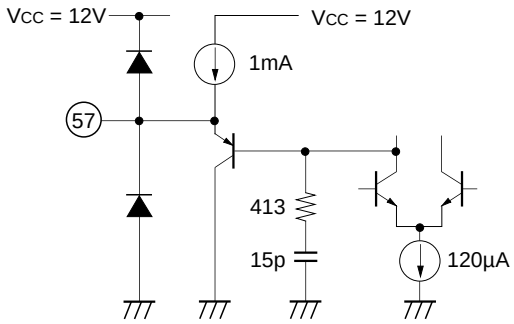
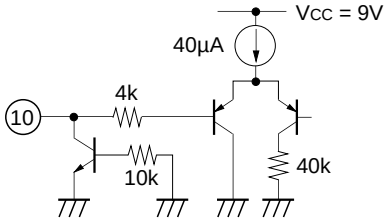
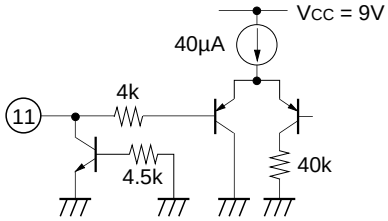
(OSD = On-Screen Display)

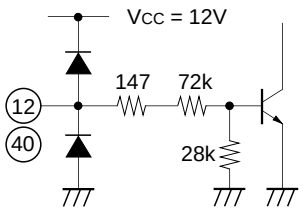
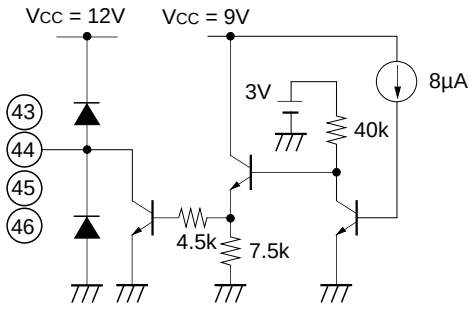
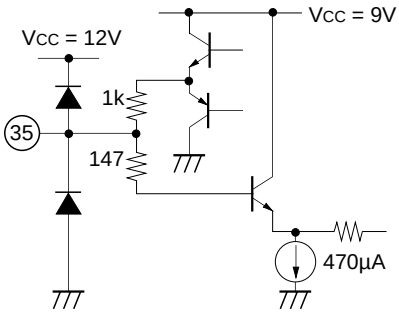
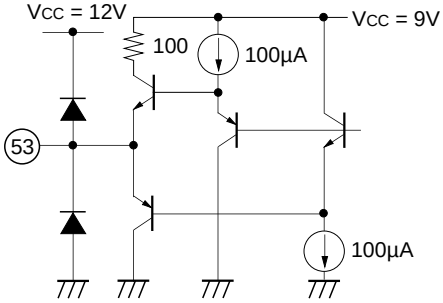


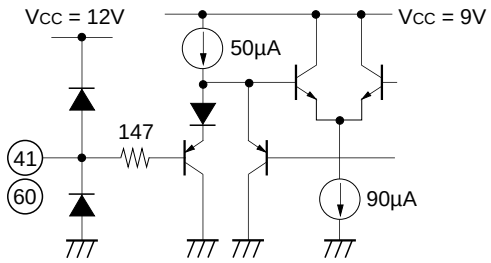
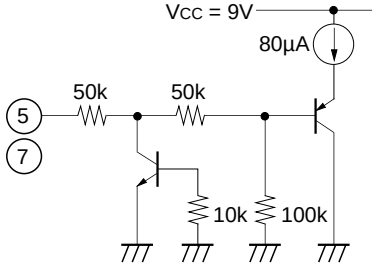
Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
62 18 64 20 2 6 14 22 4 8 16 24	VIN1 VIN2 VIN3 VIN4 VIN5 VIN6 VIN7 VIN8 VIN9 VIN10 VIN11 VIN12	4.6V		Video signal inputs. Input impedance typically 120kΩ.
63 15 19 36 59 1 17 21 39 61	RIN1 RIN2 RIN3 RIN4 RIN5 LIN1 LIN2 LIN3 LIN4 LIN5	4.5V		Audio signal inputs. Input impedance typically 60kΩ.
54 52 50 48 31 29 27 33	VOUT1 VOUT2 VOUT3 VOUT4 VOUT5 VOUT6 VOUT7 VOUT8	3.9V		Video signal outputs.
51 32 28 49 30 26	RTV ROUT1 ROUT2 LTV LOUT1 LOUT2	4.5V		Audio signal outputs.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
34	MONO	4.5V		Audio mono signal output.
3	BIAS_ VIDEO	3.9V		Reference Bias for video circuit. Connected to GND with capacitor.
23	BIAS_ AUDIO	4.5V		Reference Bias for audio circuit. Connected to GND with capacitor.
37 38	FNC_TVB FNC_TVA	—		I^2C controlled output giving 0/2V. Maximum load current = 800µA

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
56	VREG_9V	9V		Pin connected to emitter of external regulator transistor.
57	VREG_ BASE	9.7V		Connection to base of external regulator transistor.
10	SCL	—		I^2C Clock Input. V_{IL} = 1.5V (max) V_{IH} = 3.0V (min)
11	SDA	—		I^2C Data input/output. V_{IL} = 1.5V (max) V_{IH} = 3.0V (min) V_{OL} = 0.4V (max)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
12 40	ADR HW MUTE	—		HW MUTE: This pin is active high > 2.5V. When high, audio outputs RTV, LTV and MONO are muted. ADR: Selects the I²C address for the IC. < 1.5V = Low Add = 90H > 2.5V = High Add = 92H
43 44 45 46	LOG_4 LOG_3 LOG_2 LOG_1	—		Open collector logic Pins. Maximum current sink = 1mA
35	TRAP	3.9V		Connection to external trap circuit. Trap components should be kept as close as possible to this pin.
53	FBLK_ OUT	—		Fast Blank output set by I²C, FBLK_IN1 or FBLK_IN2. High = 5.1V Low = 1.2V Connected to external emitter follower. Maximum load current = 800µA

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
41 60	FBLK_IN1 FBLK_IN2	—		Fast Blank inputs. Low = < 0.4V High = > 1.0, < 3.0
5 7	FNC_VCR FNC_AUX	—		Function switching input (Scart pin 8). Typical levels = 0V/6V/12V

Electrical Characteristics

Absolute Maximum Ratings

Supply Voltage	Vcc_12V	12	V

Operating Conditions

• Supply Voltage	Vcc_12V	12 to 10.7	V	
• Voltage Regulation	Vreg_9V	9 ± 0.45	V	(from 12V supply)
• Operating Voltage	Video_Vcc, Dig_Vcc,	9 ± 0.5	V	
	Audio_Vcc	9 ± 0.5	V	

FNC_TVA (pin 38) and FNC_TVB (pin 39) are static sensitive.
Precaution should be taken (note 8 in "Notes on Operation").

Operation of the CXA2078Q using a 9V supply connected directly to the V_{CC}_12V, Video_V_{CC}, AUDIO_V_{CC} and Dig_V_{CC} pins is possible but not recommended. (The unused on-chip voltage regulator is then forced to have pins Vreg_base and Vreg_9V floating.)

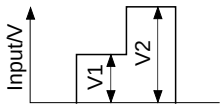
Electrical Characteristics

Nominal conditions (Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current Consumption	I_{CC}	V_{CC}_12V = 12V, No signal, no load	30	50	70	mA

Video system

Nominal conditions (Ta = 25°C, Vcc_12V = 12V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin voltage		V_{VPin}	No signal, no load (Fig.1)	4.3	4.6	4.9	V
Output pin voltage	Vout1 – 8	V_{VPout}	No signal,no load,Y/C mix inactive (Fig.1)	3.6	3.9	4.2	V
	Vout8 (mix)	V_{VPoutm}	No signal, no load, Y/C mix active (Fig.1)	3.5	3.8	4.2	V
Gain (except Y/C mixer)		GVv	f = 200kHz, 0.3Vp-p input (Fig.2)	5.5	6.0	6.5	dB
Gain of Y/C mixer		GV_{YC}	f = 200kHz, 0.3Vp-p input (Fig.2)	5.4	6.0	6.4	dB
Bandwidth (except Y/C mixer)		f_{V3dB}	0.3Vp-p input, frequency where output level is –3dB with 200kHz serving as 0dB (Fig. 2)	15	20		MHz
Bandwidth of Y/C Mixer		f_{YC3dB}	0.3Vp-p input, frequency where output level is –3dB with 200kHz serving as 0dB. No trap connected. (See note below) (Fig.2)	7	15	—	MHz
Input dynamic range		V_{DRVI}	200kHz input (Fig.2)	2.5	—	—	Vp-p
Output dynamic range		V_{DRVO}	200kHz, 2.5Vp-p input (Fig.2)	5.0	—	—	Vp-p
Cross talk		Vctv	f = 4.43MHz, 1Vp-p input (Fig.2)	—	—	–50	dB
S/N ratio		S/N_V	Ratio of 0.7Vp-p white video signal to black line noise. Weighted using CCIR 567. HPF @ 5kHz, LPF @ 5MHz. (Fig.2)	—	72	—	dB
Input Impedance		Zin_V	1Vrms 1kHz input through 56kΩ. Attenuation measured to calculate Zin_V (Fig.3)	94	120		kΩ
Non-linearity		Lin	 (Fig.4) V1 = Pin Voltage +0.5V V2 = Pin Voltage +1V At output, non-linearity = $\left(\frac{V2}{V1 \times 2} - 1\right) \times 100$	–3	–0.4	+3	%
Differential Gain		DG	1.7Vp-p 5-step modulated staircase. (Chroma and Burst are 150mVp-p 4.43MHz) (Fig.2)		1.5		%
Differential Phase		DP	as above. (Fig.2)		1		Deg
Sync crush		SC	Percentage reduction in sync pulse (0.4Vp-p), with tip at –1.2V input offset. (Fig.4)		0.2	3	%
Delay of Luma over Chroma through mixer		tcld	0.4Vp-p square wave input. Input to output edge delay measured. No trap. (Fig.2)		15	40	ns

Note) Input output path from Vin9 – 12 to Vout 8 through mixer has BW reduced by external stray capacitance on TRAP pin.

Electrical Characteristics

Audio system

Unless otherwise stated: input coupling capacitor 1µF in series with 6kΩ resistor; output coupling capacitor of 10µF; load of 10kΩ. Nominal conditions (Ta = 25°C, Vcc_12V = 12V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin voltage		V_{APIN}	No signal, no load (Fig. 5)	4.2	4.5	4.8	V
Gain	R/LOUT1, 2	GV_A	f = 1kHz, 1Vrms input. (Fig. 6)	–0.5	0	+0.5	dB
	RTV, LTV	GV_{ATV}	f = 1kHz, 1Vrms input. (Fig. 6)	–0.65	0	+0.35	dB
	MONO	GV_{AM}	f = 1kHz, 1Vrms "stereo" input. (Fig. 6)	–0.65	0	+0.45	dB
Audio frequency response		F_{AF}	0.3Vp-p input. Output level at 30kHz with 1kHz serving as 0dB. 6kΩ removed. (Fig. 7)	–0.3	0	+0.3	dB
Frequency B/W		F_{BWA1}	0.3Vp-p input; frequency where output level is –3dB with 1kHz serving as 0dB. 6kΩ removed. No load (Fig. 7)	—	1	—	MHz
Distortion		THD	f = 1kHz, 0.5Vrms, unweighted response; LPF @400Hz, HPF @ 80KHz. (Fig. 6)	—	0.004	0.2	%
Input Dynamic Range		V_{dA}	f = 1kHz (Fig. 6)	2	—	—	Vrms
Cross talk (Channel separation)		V_{ctA}	f = 1kHz, 1Vrms input on one input, measure on any other audio output. (Fig.6)	—	–88	–76	dB
Ripple rejection	R/LOUT1, 2	RR_A	f = 100Hz, 0.3Vp-p applied to Vcc_aud (Fig. 8)	—	–62	—	dB
	RTV, LTV	RR_{ATV}	f = 100Hz, 0.3Vp-p applied to Vcc_aud (Fig. 8)	—	–75	—	dB
	MONO	RR_{AM}	f = 100Hz, 0.3Vp-p applied to Vcc_aud (Fig. 8)	—	–44	—	dB
DC Offset -R/Lout1, 2		Voff	Offset voltage between any audio input and R/Lout1, 2 (Fig. 5)	–30	+2	+30	mV
Input impedance		Zin	(excluding series external 6kΩ)	48	60	72	kΩ
Output Impedance		Zout	(excluding any external series resistor)	—	10	—	Ω
Phase Difference		Vpda	f = 1kHz, 1Vrms input to two channels. Phase difference of stereo output measured	—	0.05	—	Deg
S/N ratio		S/N_A	f = 1kHz, 1Vrms input (at maximum volume). HPF @ 20Hz, LPF @ 20kHz. (Fig. 6)	72	95	—	dB
Electronic Volume Control							
Fine volume attenuation step		A_{EVC}	f = 1kHz, 0.5Vrms input. Set by I^2C (Fig.6)	0.6	1	1.4	dB
Coarse volume attenuation step		A_{EVF}	f = 1kHz, 0.5Vrms input. Set by I^2C (Fig.6)	7.5	8	8.5	dB
Mute		Amute	f = 1kHz, 1Vrms input. (Fig.6)		>80		dB
DC Offset -RTV, LTV		VoffTV	Offset voltage between any audio input and RTV, LTV outputs (Fig.5)	–30	+2	+30	mV

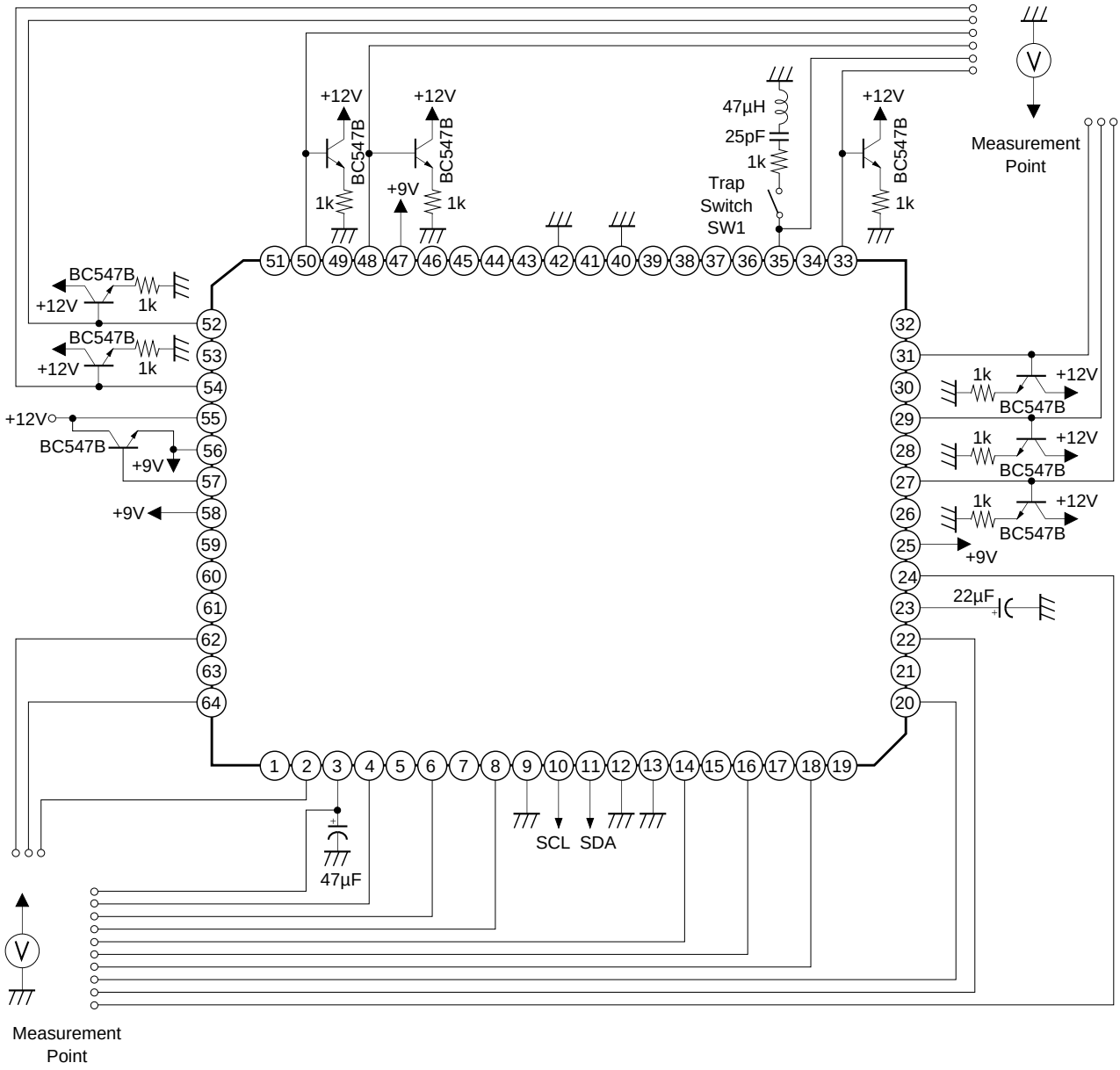


Fig. 1. Video system (d.c.test)

Notes) 1. All +9V supplies de-coupled close to supply pins, 25, 47, 58 with 10nF ceramic capacitor.
2. All video outputs are loaded with emitter follower during tests.
3. Voltage measurements carried out with a high input impedance DVM. Typically 10GΩ.

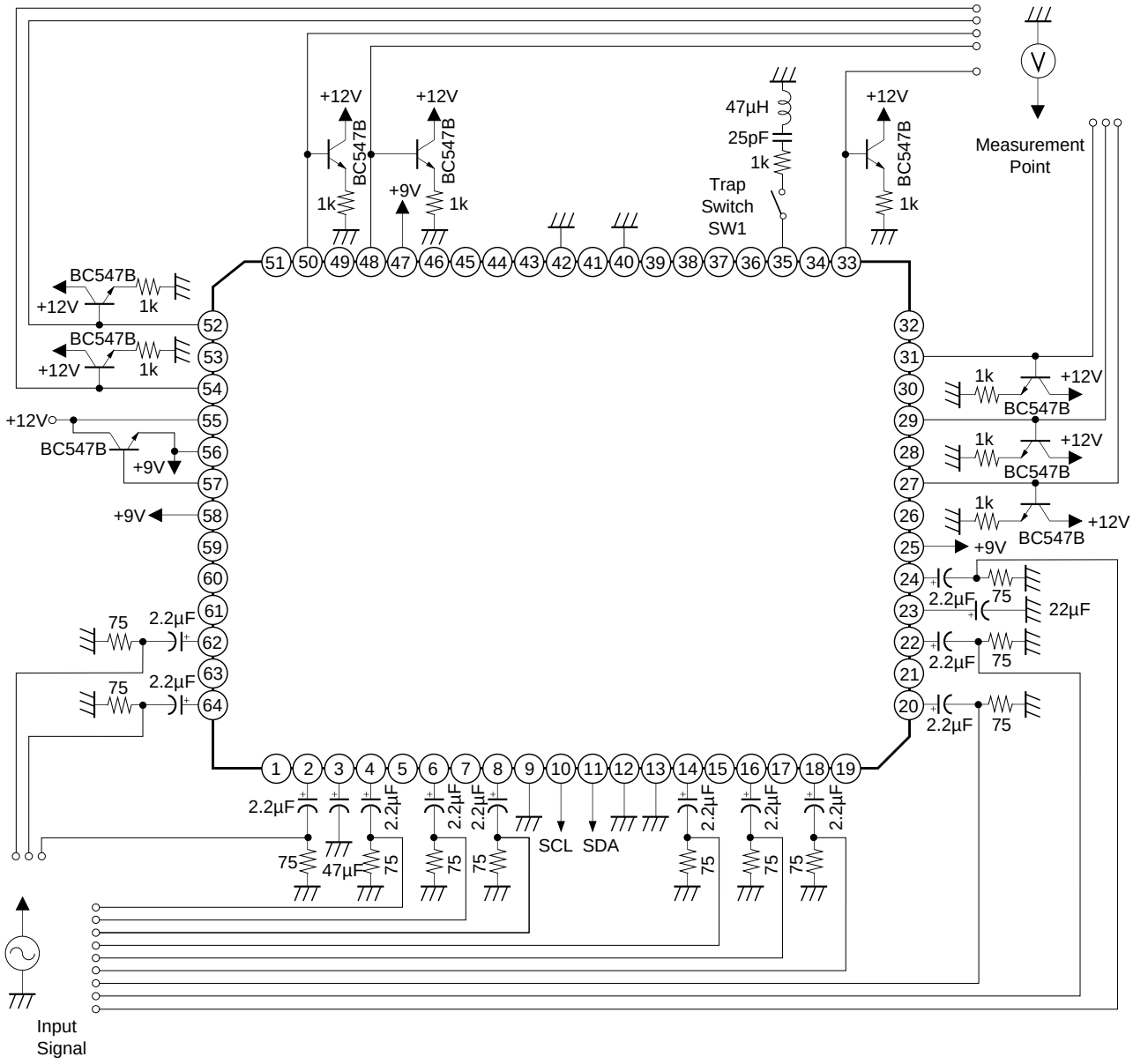


Fig. 2. Video system (gain, dynamic range, bandwidth, differential gain, differential phase, crosstalk, signal to noise, Luma-Chroma delay)

Signal applied to Pins 2, 4, 6, 8, 14, 16, 18, 20, 22, 24, 62, 64
Output Signal Measured from pins 27, 29, 31, 33, 48, 50, 52, 54

Notes)
1. All +9V supplies de-coupled close to supply pins, 25, 47, 58 with 10nF ceramic capacitor.
2. For tests requiring video measuring equipment with 75Ω input impedance, an external video line driver or buffer is used.
3. For bandwidth tests through Y/C mixer, the trap circuit is switched out using SW1.
4. All video outputs are loaded with emitter follower during tests.
5. For Luma and Chroma input to output delay, measure signal at the I.C. pins.

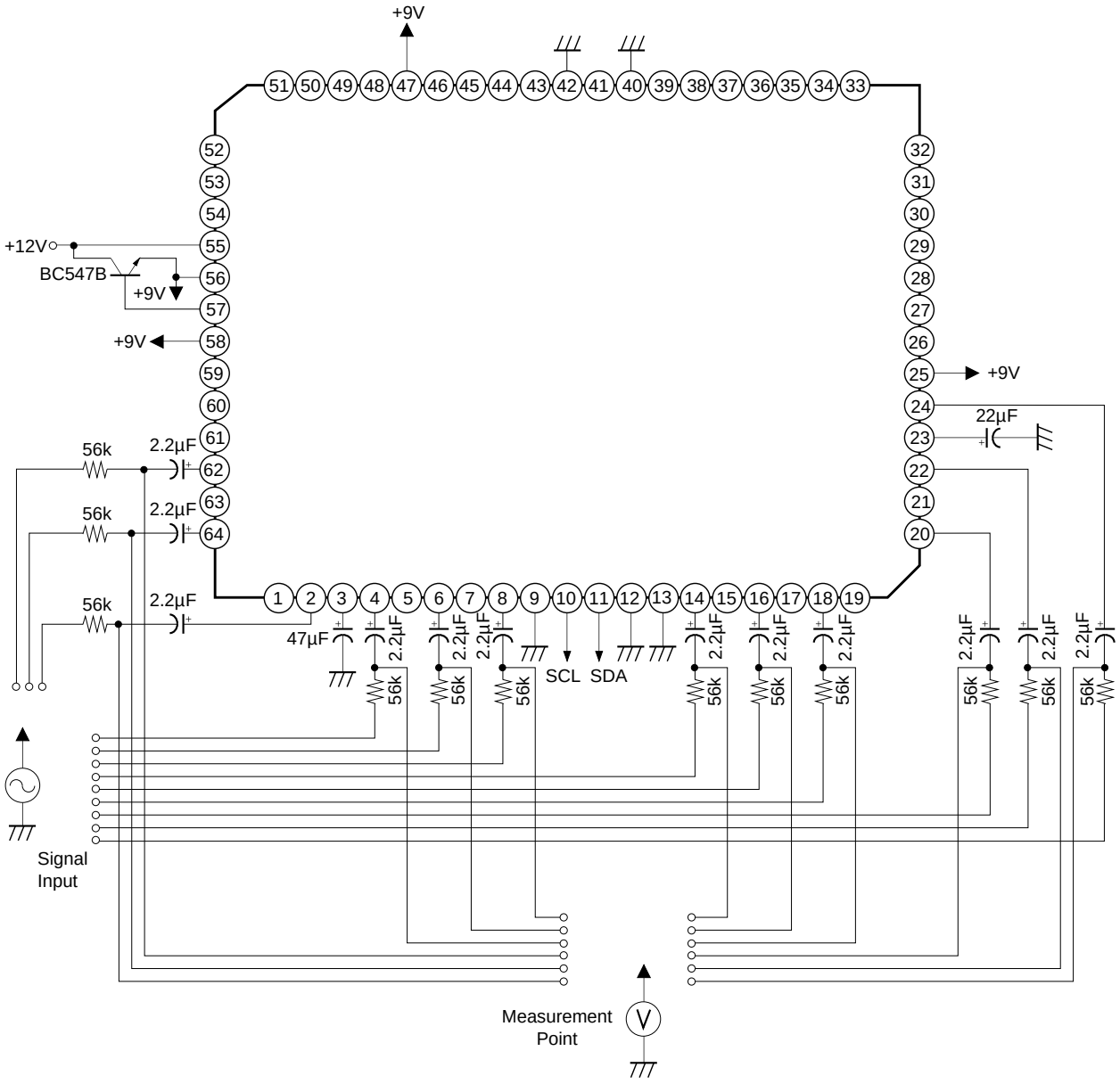


Fig. 3. Video system (input impedance)

Signal applied and measured from pins, 2, 4, 6, 8, 14, 16, 18, 20, 22, 24, 62, 64

Notes) 1. All +9V supplies de-coupled close to supply pins, 25, 47, 58 with 10nF ceramic capacitor.
2. Voltage measurements carried out with a high input impedance DVM. Typically 10GΩ.

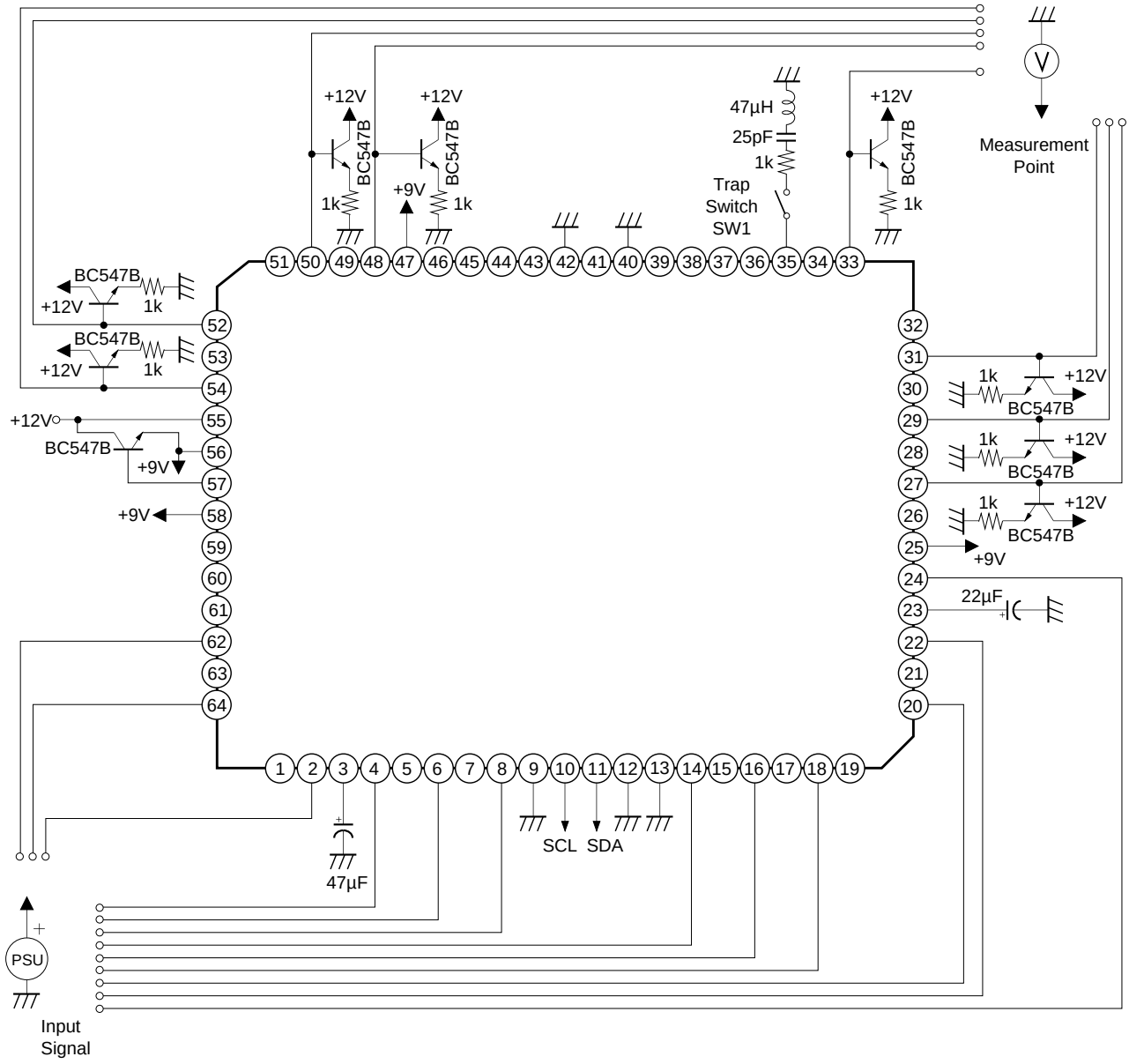


Fig. 4. Video system (linearity, sync crush)

Signal applied to Pins, 2, 4, 6, 8, 14, 16, 18, 20, 22, 24, 62, 64
Output Signal Measured from pins 27, 29, 31, 33, 48, 50, 52, 54

Notes) 1. All +9V supplies de-coupled close to supply pins, 25, 47, 58 with 10nF ceramic capacitor.
2. All video outputs are loaded with emitter follower during tests.

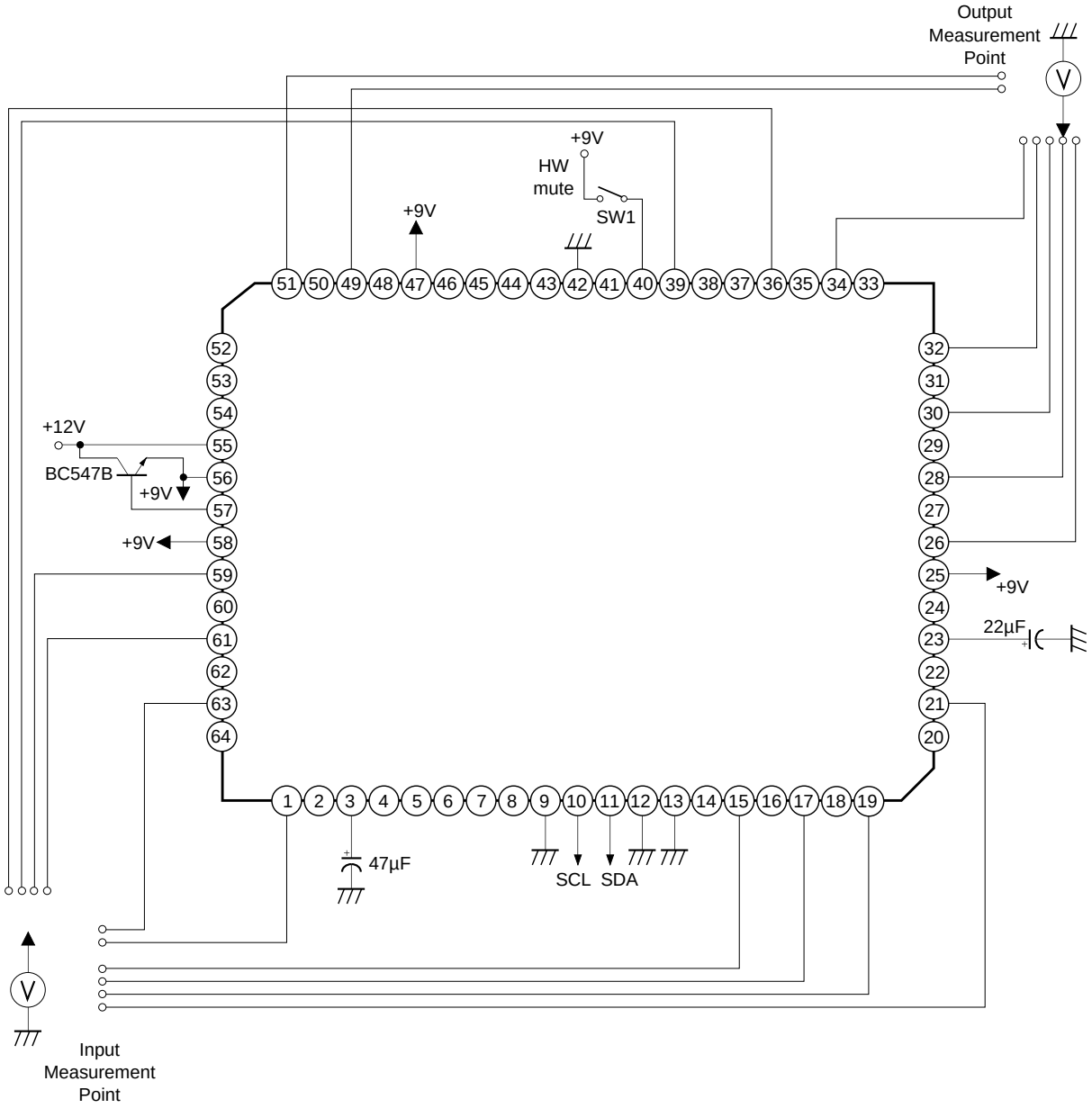


Fig. 5. Audio system (d.c. tests)

Notes) 1. All +9V supplies de-coupled close to supply pins, 25, 47, 58 with 10nF ceramic capacitor.
2. Voltage measurements carried out with a high input impedance DVM. Typically 10GΩ.

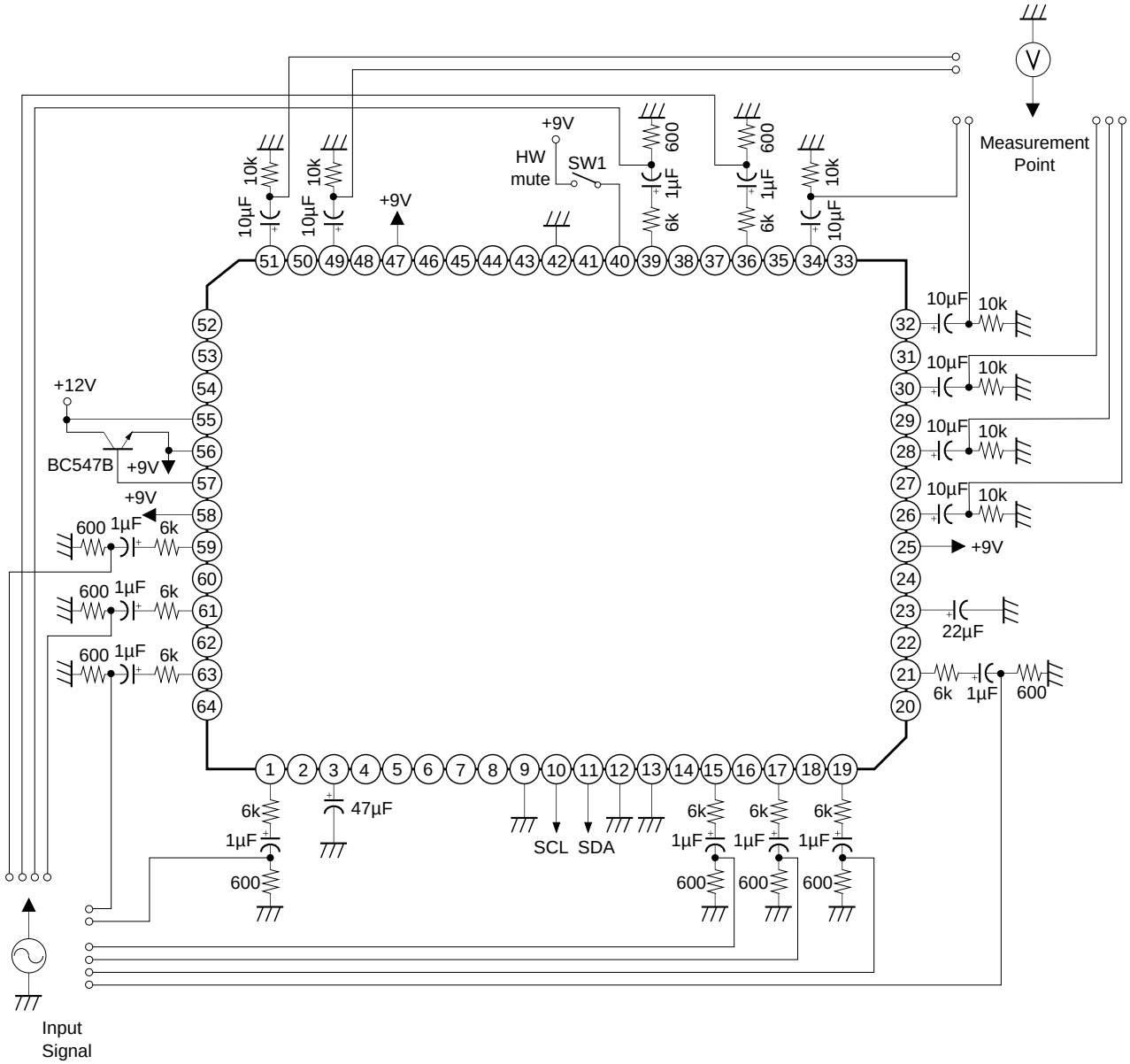


Fig. 6. Audio system (gain, dynamic range, Signal to noise, Crosstalk, Distortion, Volume control)

Signal applied to Pins, 63, 1, 59, 61, 15, 17, 19, 21, 36, 39
Output Signal Measured from pins 26, 28, 30, 32, 34, 49, 51

Notes) 1. All +9V supplies de-coupled close to supply pins, 25, 47, 58 with 10nF ceramic capacitor.
2. When muting audio using Hardware mute, SW1 is closed.

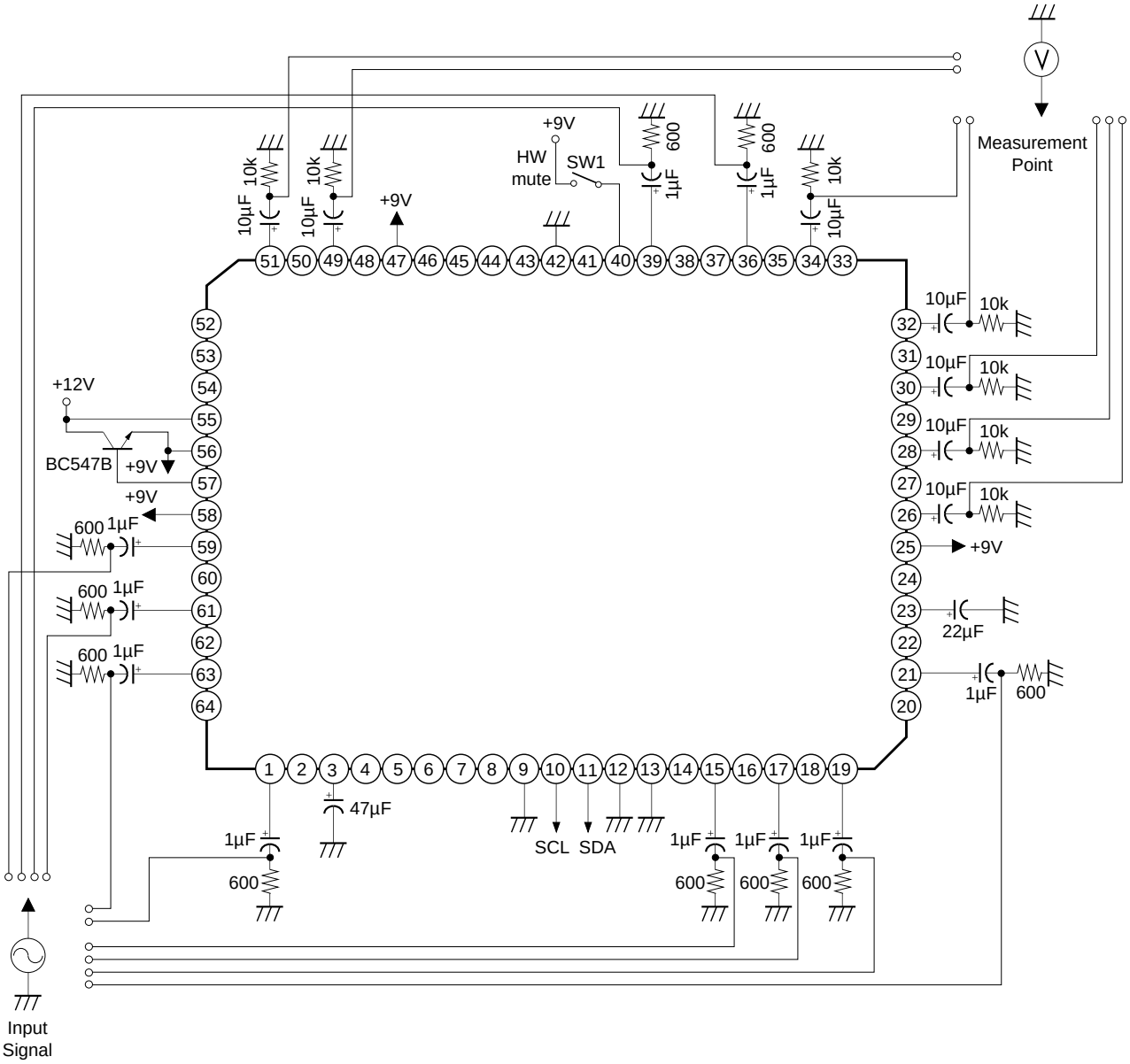


Fig. 7. Audio system (Bandwidth)

Signal applied to Pins, 63, 1, 59, 61, 15, 17, 19, 21, 36, 39
Output Signal Measured from pins 26, 28, 30, 32, 34, 49, 51

Note) All +9V supplies de-coupled close to supply pins, 25, 47, 58 with 10nF ceramic capacitor.

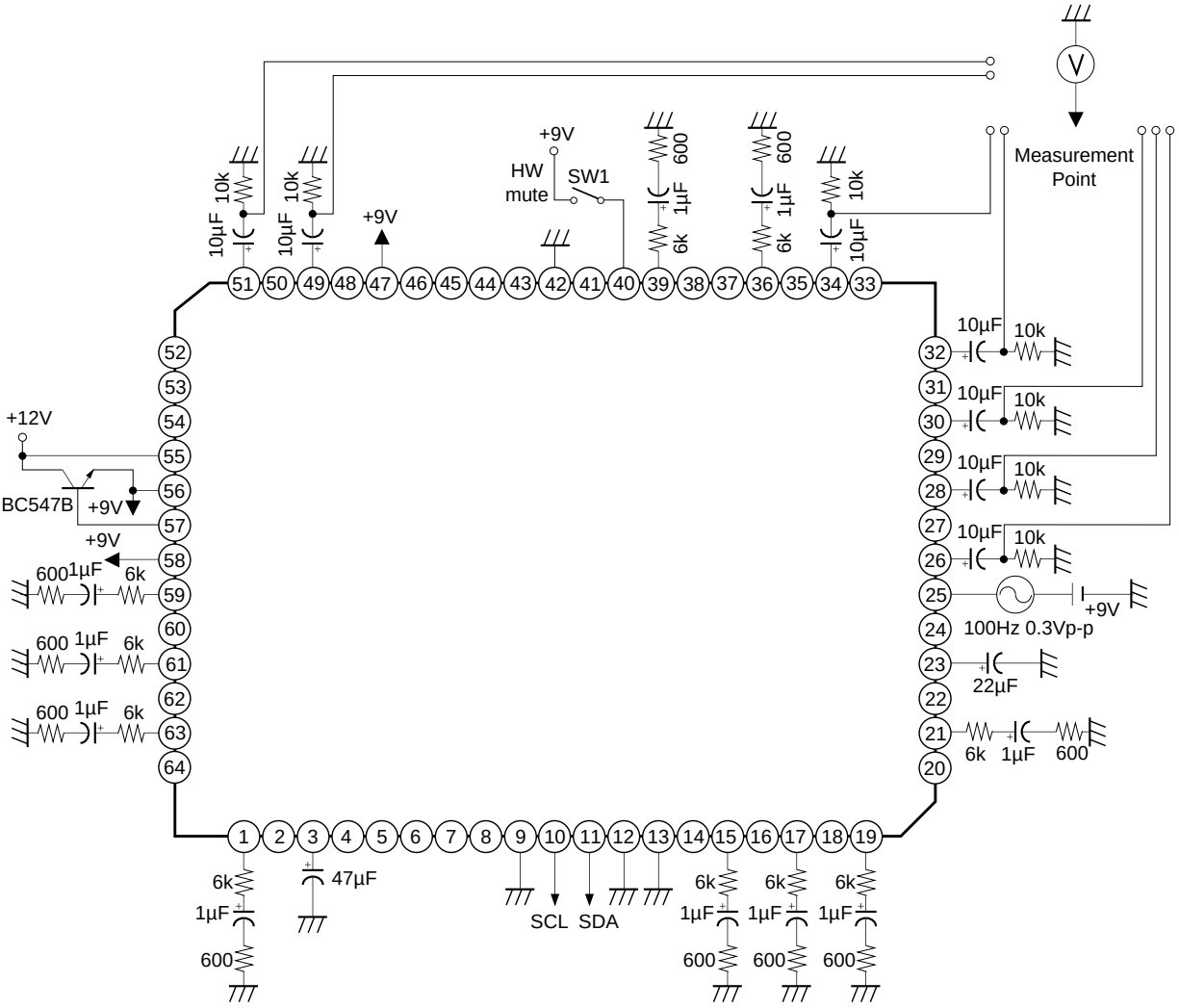
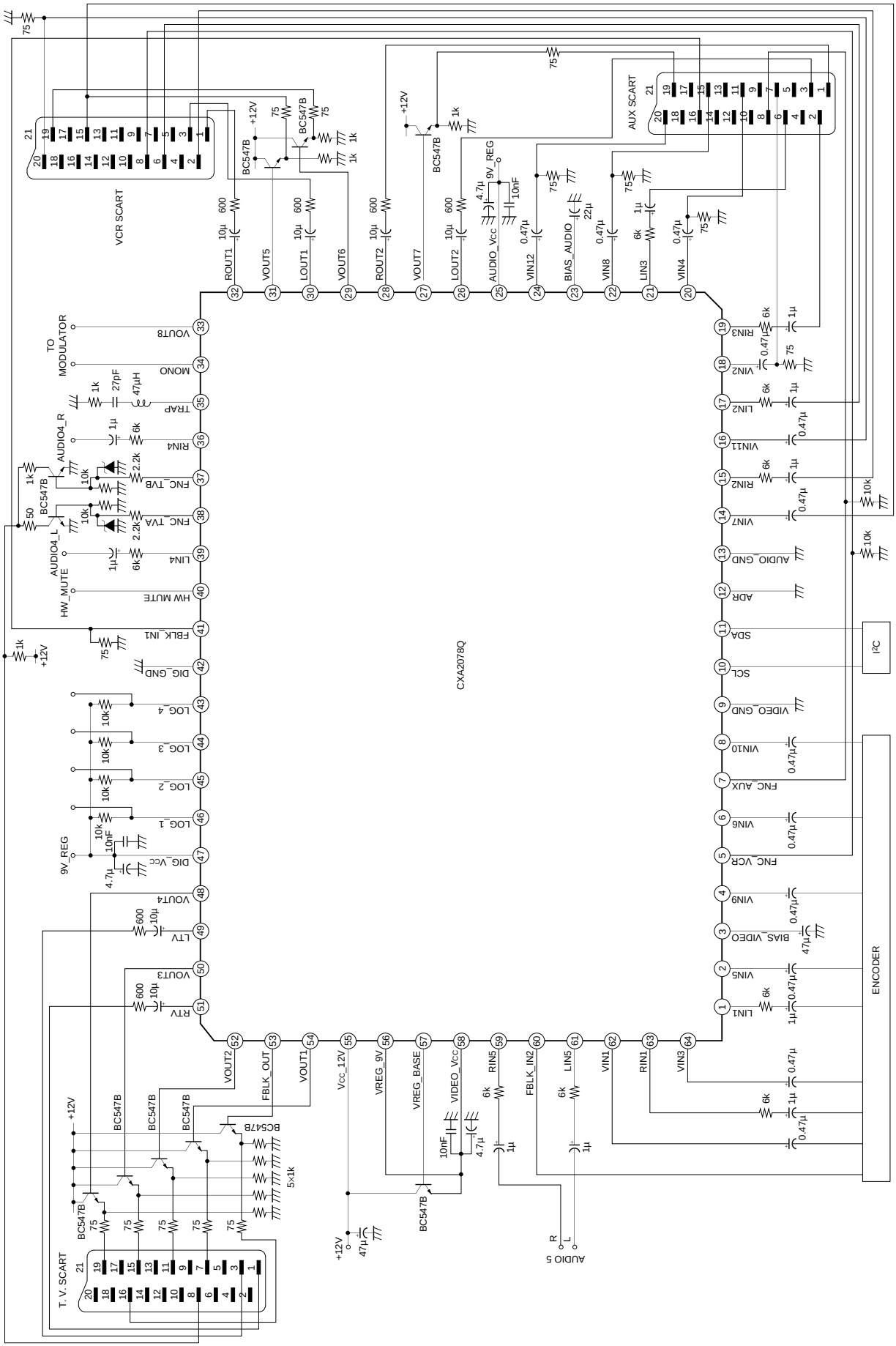


Fig. 8. Audio system (Ripple Rejection)

Output Signal Measured from pins 26, 28, 30, 32, 34, 49, 51

Note) All +9V supplies de-coupled close to supply pins, 25, 47, 58 with 10nF ceramic capacitor.

Typical Application Circuit



Description of operation

1. Explanation of Video Section

The video section comprises of 12 high impedance (120kΩ) inputs switched through to 8 video outputs. A +6dB internal amplifier is connected to each output. The amplifier is required to compensate for the 6dB attenuation which occurs at the external emitter follower stage used for driving video loads. The typical external configuration is shown in Fig. 1-1.

A Y/C mixer can be used for mixing Luma and Chroma signals for use with an external RF modulator connected to Vout8. The Y/C mixer is controllable via the I^2C data bus. The circuit is shown in Fig. 1-2 with a trap circuit used to give 3dB attenuation at 4.43MHz of the Luma signal.

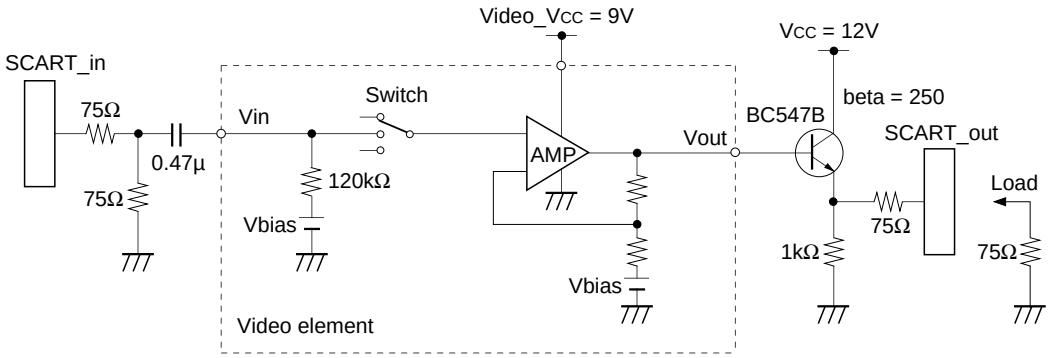


Fig. 1-1. Video circuit element: 6dB gain amplifier with external emitter follower

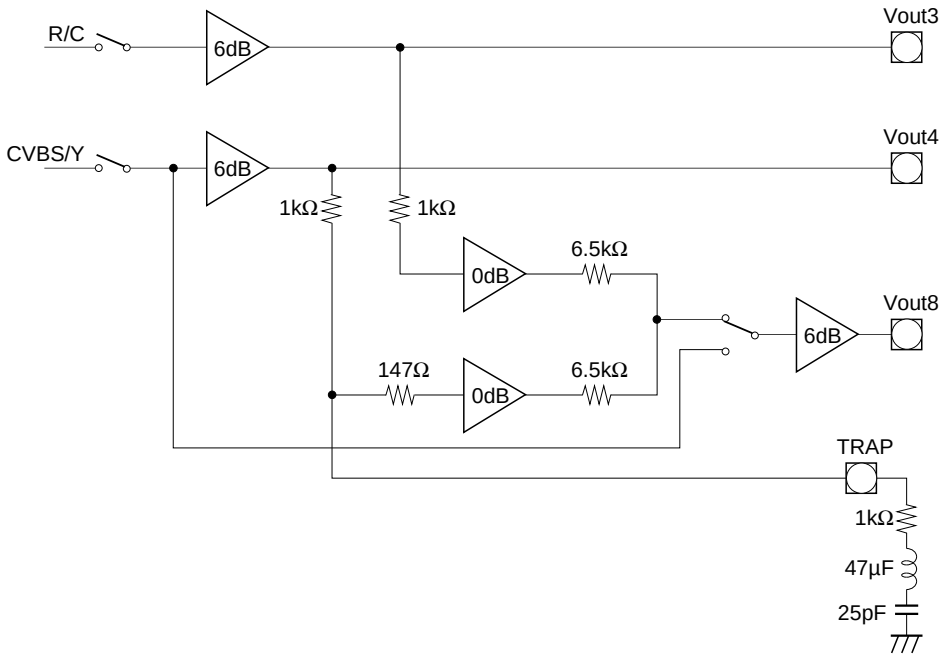


Fig. 1-2. Y/C MIXER Circuit

2. Explanation of Audio System.

Audio Switch and Amplifier

The audio system consists of 5 stereo inputs, 3 stereo outputs and a mono output. Each output can be independently connected to any one of five inputs, Lin1 to Lin5 for the left stereo audio channel, and Rin1 to Rin5 for the right hand audio channel. In all cases, the input to the switch and amplifier is composed of a potential divider consisting of a 27kΩ series resistor and a 33kΩ connected to a voltage source (4.5V). When used in conjunction with an external 6kΩ series input resistor, the input configuration forms a –6dB attenuator (Fig. 2-1). The net gain of the audio system is zero as there is an internal +6dB amplifier on each output. The output impedance of the audio amplifier is near zero, and is used to drive the external SCART circuit. The output is capacitively coupled through a 10µF capacitor, and an optional 600Ω series compliance resistor. Depending on the length and type of cable used in the scart cable connector, the load seen at the scart terminal will consist of a parallel capacitor, (100pF to 400pF) and mandatory 10kΩ resistor connected to ground (Fig. 2-2). The customer may chose to place an alternative audio output filter at the AV switch output.

TV audio output

The TV audio section is composed of an audio switch and 0dB amplifier followed by two variable gain stages, corresponding to the course and fine electronic volume control amplifiers, EVC and EVF. The EVC amplifier attenuates the input signal in steps of 8dB. A range of attenuation from 0dB to 56dB can be programmed by means of the I^2C interface. Similarly, the fine volume control (EVF) can be programmed to provide a range of attenuations between 0dB and 7dB. The attenuated signal is passed through to the output buffer stage which provides the necessary +6dB gain, and is used to drive the SCART connector. The final output buffer can also act as a –80dB (mute) amplifier (Fig. 2-4).

Zero Cross Detector (ZCD)

The zero cross detector reduces the effect of "click noise" when implementing a volume change or an audio mute. The change volume or mute instruction sent by I^2C will only be implemented when a minimal (ie zero cross) signal amplitude is detected.

The zero cross detection circuit can be turned off by setting the "ZCD" bit low in the I^2C write mode.

The status of the zero cross detector can be checked in the I^2C read mode (Z.C status). When this bit is high, a zero cross condition has been detected subsequent to the issue of an I^2C volume change or mute instruction. This may be useful if the input waveform is very low frequency, whereupon the microprocessor can re-issue the same instruction, with the zero cross detector circuit switched off.

I^2C Mute

The mute instruction in the I^2C format refers to the TV audio circuit. Audio mute can be implemented after a audio zero cross detection, or immediately depending on whether ZCD = 1 or 0.

It can be seen from the I^2C write format that the same mute bit occurs in DATA1 and DATA5. This allows the software to action an immediate mute, make any suitable changes to the audio source or electronic volume control and after a minimum period of $4 \times 90\mu s$ (360µs) un-mute the output buffer. Such a period provides ample time to allow any transient ac voltages to settle during an audio source change.

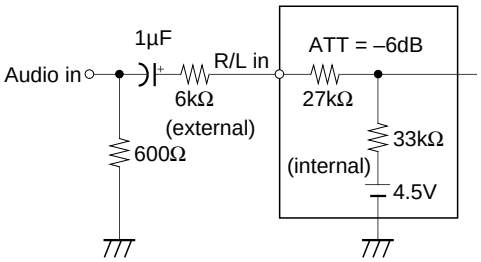


Fig. 2-1. Audio input configuration

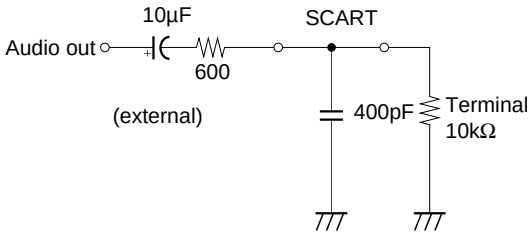


Fig. 2-2. Audio output configuration

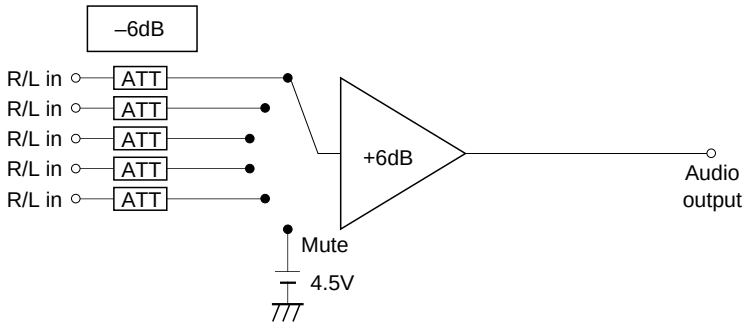


Fig. 2-3. VCR and AUX audio configuration

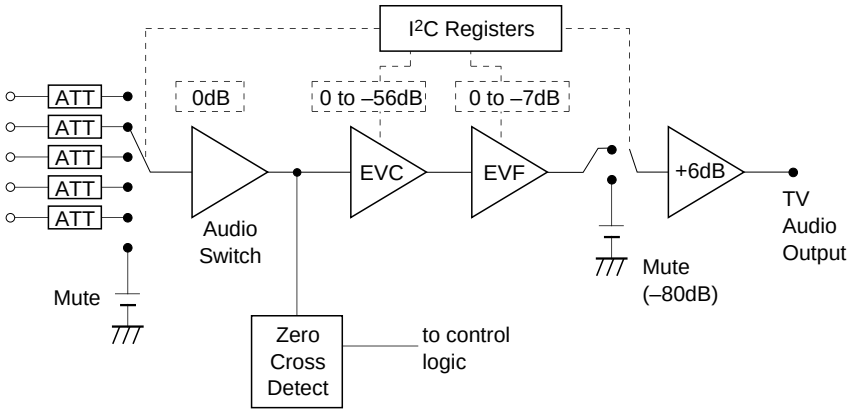


Fig. 2-4. T.V. audio section and Electronic Volume Control

I²C Interface Data Format

IC Control Data Format

S	Slave address	A	DATA1	A	DATA2	A	DATA3	A	DATA4	A	DATA5	A	P

S: Start condition A: Acknowledge P: Stop condition

There are two possible addresses depending on external address pin (12) tied high or low.
Pin 12 = high, Address = 92 Hex Ao = 1
Pin 12 = low, Address = 90 Hex Ao = 0

General I²C data structure (write mode)

	b7	b6	b5	b4	b3	b2	b1	b0
Address	1	0	0	1	0	0	Ao	(W) 0
Data1	EVC			EVF			TVMute	Z.C.D
Data2	F_{BLK}		Vid_Sw1 (TV)			Aud_Sw1 (TV)		
Data3	FNC		Vid_Sw2 (VCR)			Aud_Sw2 (VCR)		
Data4	Y/C Mix	x	Vid_Sw3 (AUX)			Aud_Sw3 (AUX)		
Data5	TVMute	x	x	x	LOG4	LOG3	LOG2	LOG1

Key
EVC: Electronic Volume Course (8dB steps)
EVF: Electronic Volume Fine (1dB steps)
TVMute: TV Audio mute. Controls the TV audio output buffer. (Same bit appears in data 1 & 5)
Z.C.D: Zero cross detector active. When ZCD = 1 volume and mute change at zero cross.
Vid_Sw1: Selects the input video sources for Vout1, Vout2, Vout3, Vout4
Vid_Sw2: Selects the input video sources for Vout5, Vout6
Vid_Sw3: Selects the input video sources for Vout7
Aud_Sw1: Selects one of 5 stereo inputs for RTV, LTV
Aud_Sw2: Selects one of 5 stereo inputs for Rout1, Lout1
Aud_Sw3: Selects one of 5 stereo inputs for Rout2, Lout2
FNC: Video function switch control
FBLK: Video Fast Blanking control
Y/C Mix: When Y/C Mix = 1 converts Y/C input to CVBS for output through Vout8
LOG1-LOG4: Logic outputs (open collector). 0 = high impedance. 1 = current sink mode.

General I²C data structure (read mode)

S	Slave address	A	DATA6	NA	P

NA: No Acknowledge

DATA STRUCTURE

	b7	b6	b5	b4	b3	b2	b1	b0
Slave Address	1	0	0	1	0	0	X	(R) 1
Data6	x	x	ZC STATUS	P.O.D.	FUNC_AUX		FUNC_VCR	

FUNC_VCR: At pin 5 AV switch monitors the voltage of pin 8 from VCR scart, and records status.

FUNC_AUX: At pin 7 AV switch monitors the voltage of pin 8 from AUX scart, and records status.

ZC Status: ZC Status = 1 indicates that zero cross condition has been achieved after a volume or mute instruction issued.

P.O.D.: Power On Detect. P.O.D. = 1 when DIG_V_{CC} voltage rises above a threshold level of approximately 5V.

3. Video Input I²C Control

3-1. Video Switch 1 (Vid_Sw1) – TV Output

			Vout1	Vout2	Vout3	Vout4	Comment
			B	G/CVBS/Y	R/C	CVBS/Y	
d2_b5	d2_b4	d2_b3					
0	0	0	Vin1	Vin3	Vin5	Vin9	Digital encoder
0	0	1	Vbias	Vbias	Vin6	Vin10	Digital encoder
0	1	0	Vbias	Vbias	Vin7	Vin11	VCR
0	1	1	Vin2	Vin4	Vin8	Vin12	Aux
1	0	0	Vbias	Vbias	Vin5	Vin3	Digital encoder
1	0	1	Vin1	Vin3	Vin5	Vin10	Digital encoder
1	1	0	Vin1	Vin3	Vin5	Vin11	Digital encoder
1	1	1	Vbias	Vbias	Vbias	Vbias	Video Mute

Table 3-1. showing which video input pins connect to the four TV output pins

3-2. Video Switch 2 (Vid_Sw2) – VCR Output

			Vout5	Vout6	Comment
			Chroma (C)	CVBS/Y	
d3_b5	d3_b4	d3_b3			
0	0	0	Vin5	Vin9	Digital encoder
0	0	1	Vin6	Vin10	Digital encoder
0	1	0	Vin7	Vin11	VCR
0	1	1	Vin8	Vin12	Aux
1	0	0	Vin5	Vin3	Digital encoder
1	0	1	Vbias	Vbias	Video Mute
1	1	0	Vbias	Vbias	Video Mute
1	1	1	Vbias	Vbias	Video Mute

Table 3-2. showing which video input pins connect to the two VCR output pins

3-3. Video Switch 3 (Vid_Sw3) – AUX Output

			Vout7	Comment
			CVBS	
d4_b5	d4_b4	d4_b3		
0	0	0	Vin9	Digital encoder
0	0	1	Vbias	Video Mute
0	1	0	Vin11	VCR
0	1	1	Vin12	Aux
1	0	0	Vin3	Digital encoder
1	0	1	Vbias	Video Mute
1	1	0	Vbias	Video Mute
1	1	1	Vbias	Video Mute

Table 3-3. showing which video input pins connect to the single AUX output pin

4. Fast Blanking operation (Pin 16 on SCART), FBLK

The fast blanking signal instructs the TV to select either the external CVBS information or the external RGB information. This is used to impose an on screen display (OSD) presentation (normally RGB) upon a CVBS background. Fast blanking information has the same nominal phase as the RGB and CVBS signal, and is defined as follows,

Fast blanking output at scart,

1. CVBS mode Scart pin voltage = 0 to 0.4V
2. RGB mode Scart pin voltage = 1 to 3.0V

Threshold voltage is approximately 0.75V DC voltage at scart input.

The blanking information is usually generated by the same source as that producing the RGB signal.

I²C Control

In the CXA2078Q, there are two fast blanking inputs, one associated with the auxiliary RGB/CVBS inputs and another associated with Digital Encoder input. These can be selected by I²C. In addition to the two blanking inputs, the fast blank pin output can be set to a constant 0V or 5V by means of the I²C control. Hence there are four possible states. These are controlled according to the following table.

FBLK		
d2_b7	d2_b6	FBLK_OUT (pin 53)
0	0	0V*1
0	1	5V
1	0	same state as FBLK_IN1 (0/5V)
1	1	same state as FBLK_IN2 (0/5V)

*1 Default = 0V at power up

5. Function switch, FNC.

The function switch facility is designed to read the status of the SCART function pin 8 from the VCR and AUX inputs (IC pin 5, 7). The output function pins FNC_TVA and FNC_TVB are controlled from the IC using a write instruction. A suitable interface circuit (fig 5-2) will allow FNC_TVA and FNC_TVB to instruct the TV to switch between display modes.

Read Mode DATA STRUCTURE

	b7	b6	b5	b4	b3	b2	b1	b0
Slave Address	1	0	0	1	0	0	X	(R) 1
Data6			Z.C STATUS	P.O.D.	FUNC_AUX		FUNC_VCR	

Read mode

Status of I^2C registers as a function of the voltage on FNC_AUX (pin 7) and FNC_VCR (pin 5)

Input Pin Voltage		read data6	
FNC_AUX or FNC_VCR	Level (SCART Defn)	b3/b1	b2/b0
0V to +2V (default)	(Internal TV)	0	0
+4.5 to +7V	(16:9 External)	0	1
+9.5 to +12V	(4:3 External)	1	1

Write mode TV Function switch, Interface table

d3_b7	d3_b6	FNC_TVA Pin voltage	FNC_TVB Pin voltage	Comment
0	0	2V	2V	Internal TV (default)
0	1	0V	2V	External 16:9
1	0	0V	0V	External 4:3
1	1	0V	0V	External 4:3

Default is Internal TV (0, 0) at power up

The two function output pins are controlled via logic to swing from 0 to +2V.

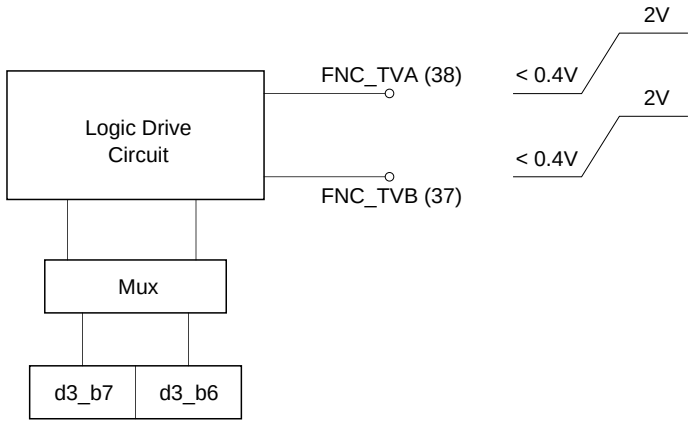


Fig. 5-1. TV Function switch output

Some external circuitry is required to interface from the IC pins to the SCART pin 8. A typical interface circuit is shown in Fig. 5-2.

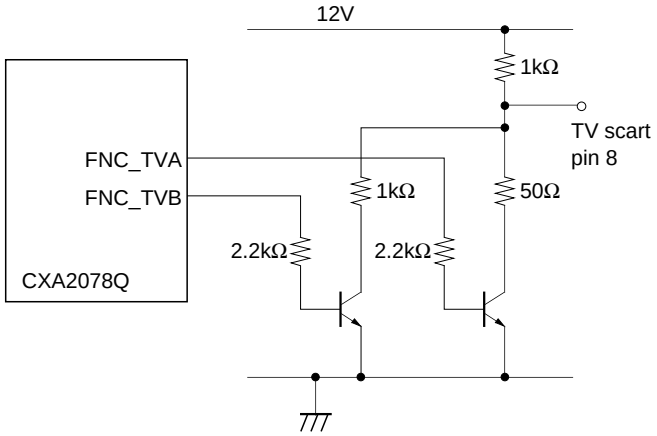


Fig. 5-2. External circuit for function switch

6. Logic outputs

I²C control of logic outputs achieved using bits LOG1 – 4.

Specification

I²C bit 0 = open collector/high output impedance on logic pin

I²C bit 1 = current sink mode resulting in 0.2V saturation voltage on logic pin

Vmax at logic pin = 12V

Imax during current sink = 1mA

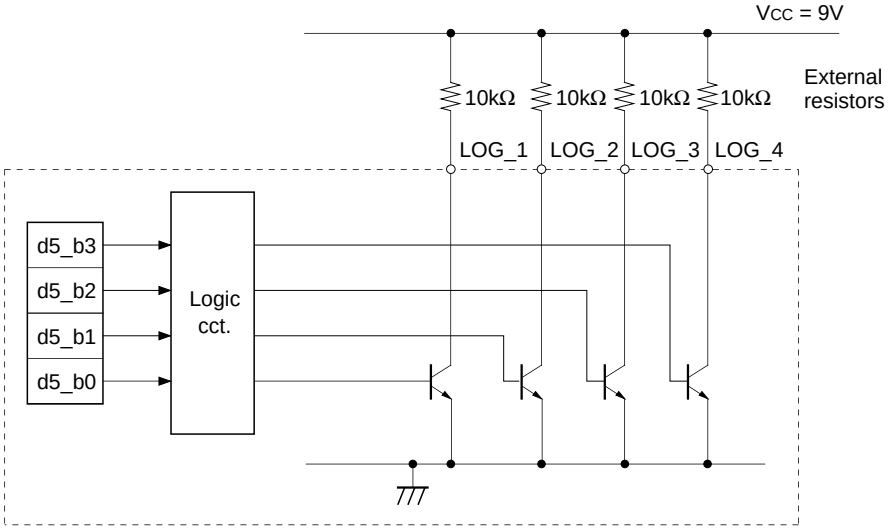


Fig. 6-1. Open collector logic outputs

7. I²C Audio Signal Control

I²C Audio input select using Aud_Sw1 (TV), Aud_Sw2 (VCR), Aud_Sw3 (AUX)

b2	b1	b0	RTV, ROUT1, ROUT2	LTV, LOUT1, LOUT2
0	0	0	Rin1	Lin1
0	0	1	Rin2	Lin2
0	1	0	Rin3	Lin3
0	1	1	Rin4	Lin4
1	0	0	Rin5	Lin5
1	0	1	Audio mute	Audio mute
1	1	0	Audio mute	Audio mute
1	1	1	Audio mute	Audio mute

I²C Electronic Volume control (coarse) DATA 1, EVC

b7	b6	b5	Gain (dB)
0	0	0	0
0	0	1	–8
0	1	0	–16
0	1	1	–24
1	0	0	–32
1	0	1	–40
1	1	0	–48
1	1	1	–56

I²C Electronic Volume control (fine) DATA 1, EVF

b4	b3	b2	Gain (dB)
0	0	0	0
0	0	1	–1
0	1	0	–2
0	1	1	–3
1	0	0	–4
1	0	1	–5
1	1	0	–6
1	1	1	–7

I²C Mute function

TV Mute DATA1 b1 DATA5 b7	Z.C.D DATA1 b0	RTV, LTV, MONO output
0	0	Un-mute immediately
0	1	Un-mute on next zero cross
1	0	Mute immediately
1	1	Mute on the next zero cross

Notes on operation

1) Supply de-coupling capacitors, 10nF and 4.7µF in parallel should be inserted as close to the supply pins, 25, 47, 58 as possible.

2) To minimise crosstalk, attention should be given to the routing of audio and video to the IC inputs. PCB track lengths should be kept as short as possible and preferably, audio placed on a separate layer to the video.

3) The trap components on pin 35 should be kept as close to the IC as possible to minimise parasitic capacitance to ground.

4) Attention should be given to the electrolytic capacitors on the input and output signal pins. As the pin's voltage is between 3.7V and 4.7V dc the positive terminal on the capacitor should be orientated towards the pin.

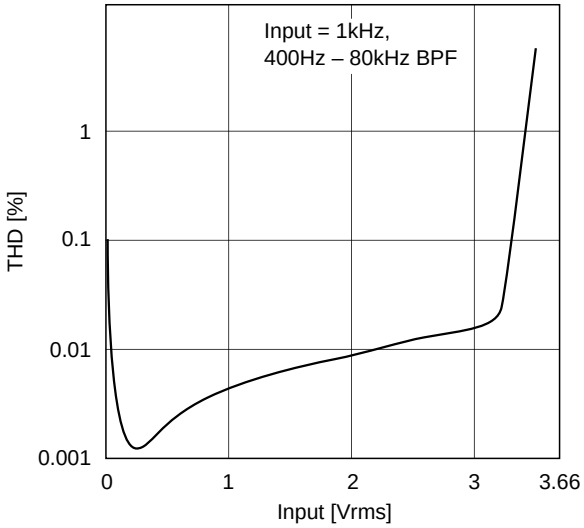
5) The audio outputs may be muted at any time after power up by connecting the HW MUTE pin (40) to a voltage > 2.5V and < 9V.

6) The I²C address of the IC can be changed using the ADR pin (12). By connecting this pin to >5V and <9V the Address changes from 90H to 92H.

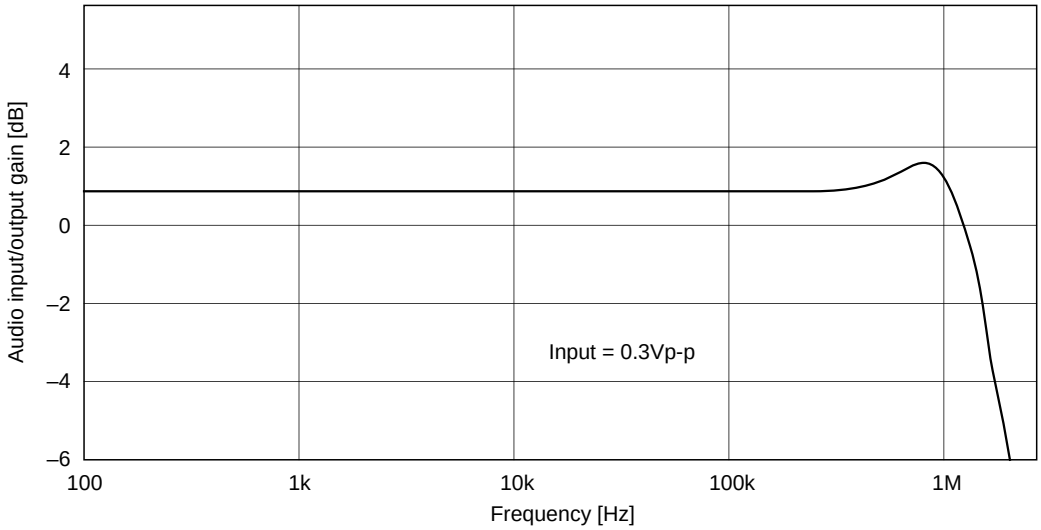
7) When driving video loads with impedance = 75Ω an emitter follower or video line driver is required to be connected at the video outputs.
   Stray capacitance on pins Vout1-8 must be kept to a minimum by placing loads as close to the pins as possible.

8) As shown on the application schematic, static protection for pins 38 and 37 may typically be achieved using Zener diodes. Diodes with a Zener voltage > 5V are suitable.

Typical audio output distortion

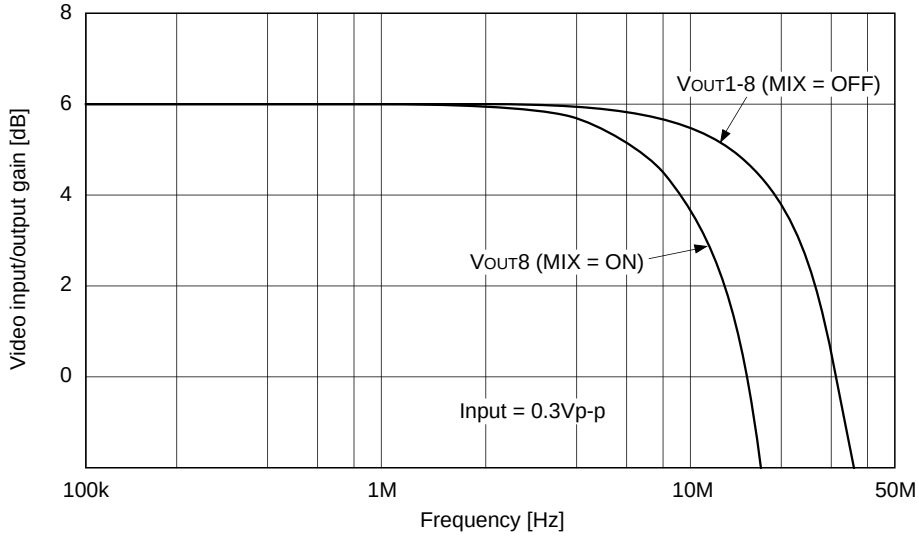


Audio frequency characteristics



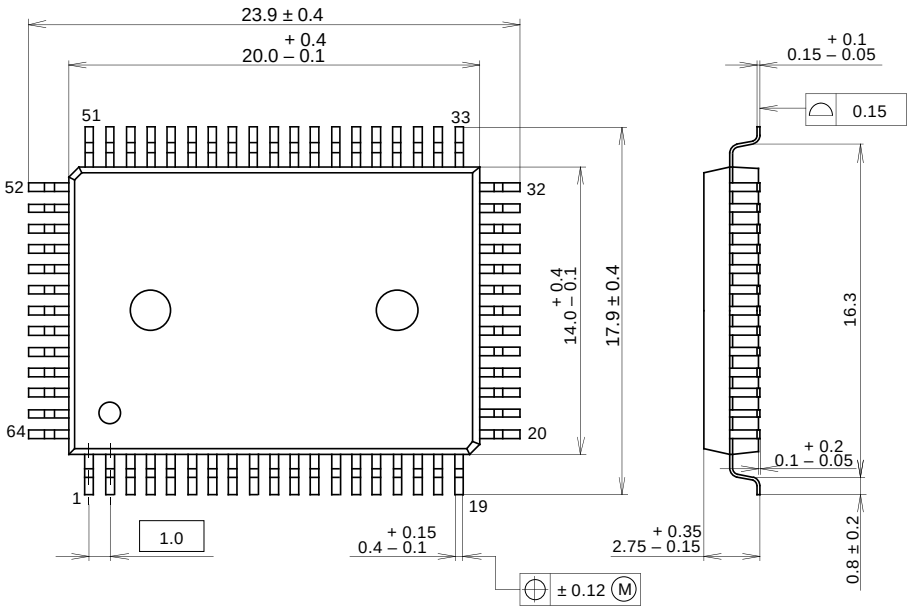
NOTE: Audio input 6kΩ resistor removed for this test.

Video frequency characteristics



Package Outline Unit: mm

64PIN QFP(PLASTIC)



SONY CODE	QFP–64P–L01
EIAJ CODE	QFP064–P–1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g