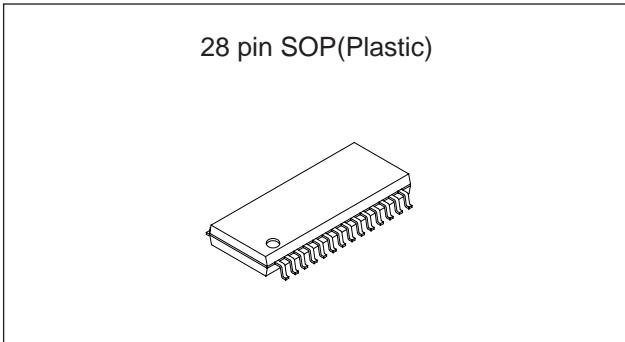


# Y color difference I/F

## Description

The CXA2119M is a video switch IC developed for Y color difference I/F used in televisions.



## Features

- Two YCbCr input systems, one RGB input system, one YCbCr output system
  - Three inputs, one output for composite video signal
  - On-chip matrix circuit for RGB signal → YCbCr signal
  - On-chip 6dB amplifier
  - Has YM function relative to YCbCr input

### Applications

TV

## Structure

## Bipolar silicon monolithic IC

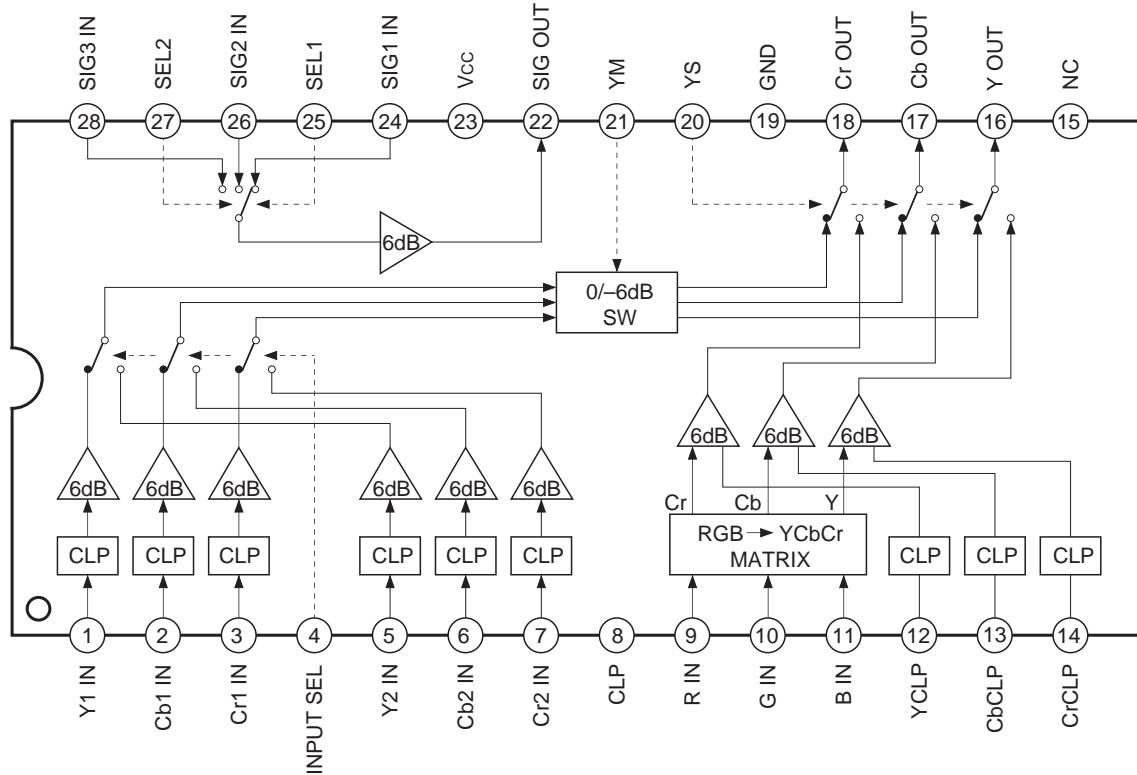
### Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

- Supply voltage V<sub>CC</sub> 12 V
  - Operating temperature T<sub>OPR</sub> -20 to +75 °C
  - Storage temperature T<sub>STG</sub> -65 to +150 °C
  - Allowable power dissipation P<sub>D</sub> 1 W
  - Pin voltage -0.3 to V<sub>CC</sub> + 0.3 V

## Operating Conditions

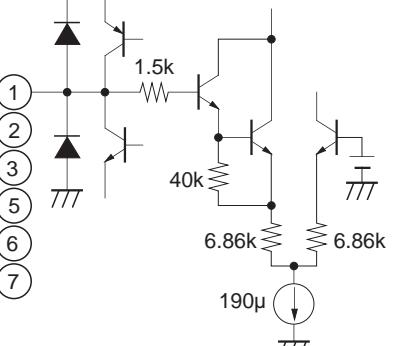
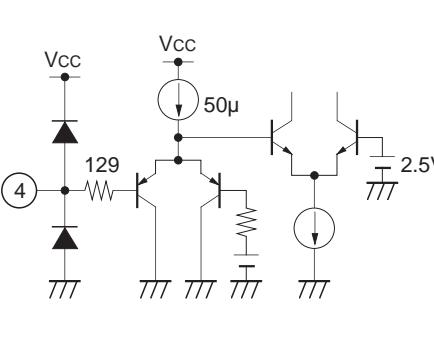
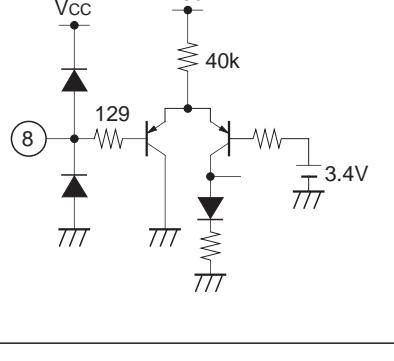
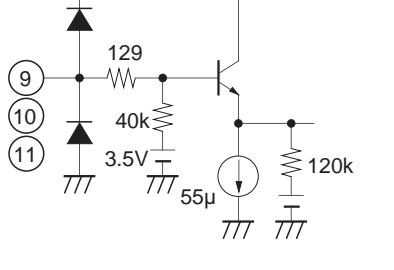
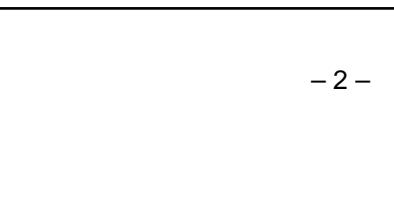
Supply voltage Vcc  $9.0 \pm 0.5$  V

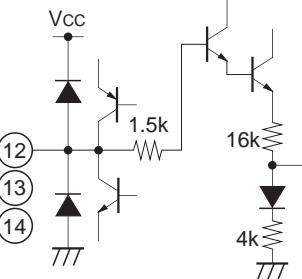
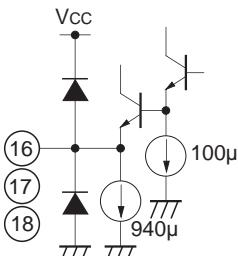
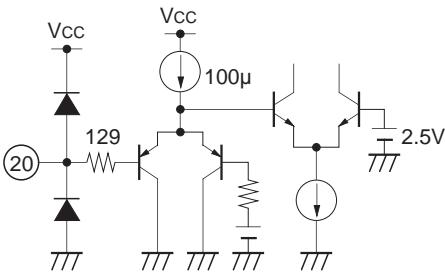
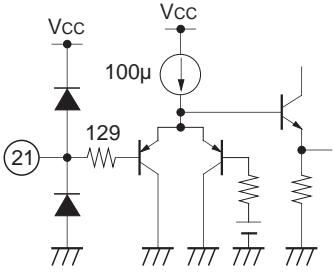
## Block Diagram



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## Pin Description

Pin No.	Symbol	Equivalent circuit	Description
1	Y1 IN		YCbCr signal input pins. Input a YCbCr standard (100% color bar, 0.7Vp-p) signal. The input signal pedestal level is clamped to 4V.
2	Cb1 IN		
3	Cr1 IN		
5	Y2 IN		
6	Cb2 IN		
7	Cr2 IN		
4	INPUT SEL		Control pin for two YCbCr inputs selection switch. High: Y1, Cb1, Cr1 inputs selected Low: Y2, Cb2, Cr2 inputs selected VILMAX = 1V VIHMIN = 3V
8	CLP		Clamp pulse input pin. High: CLP ON Low: CLP OFF VILMAX = 2.5V VIHMIN = 4V
9	R IN		
10	G IN		RGB signal input pins. Input 100 IRE, 0.7Vp-p signals via capacitors.
11	B IN		

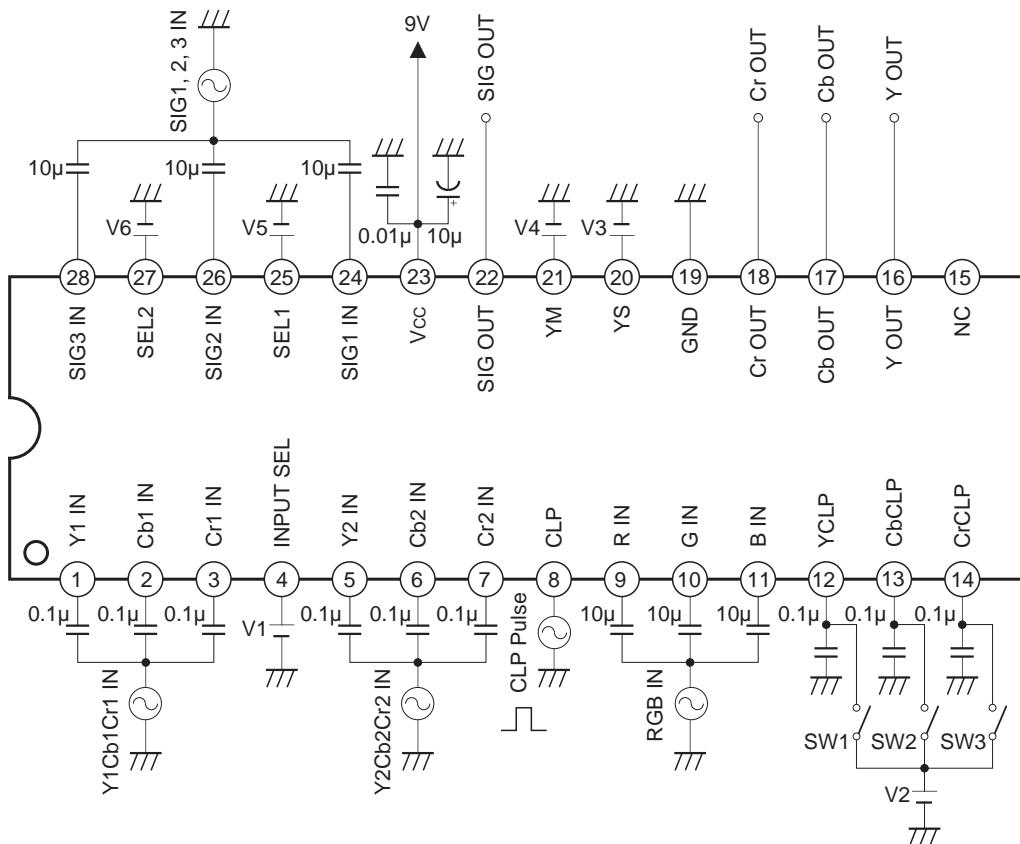
Pin No.	Symbol	Equivalent circuit	Description
12	YCLP		
13	CbCLP		Capacitor connection pins for clamping the YCbCr signal made from the RGB signal.
14	CrCLP		
15	NC		NC pin.
16	Y OUT		
17	Cb OUT		YCbCr signal output pins. Output pedestal level becomes 3.8V.
18	Cr OUT		
19	GND		GND pin.
20	YS		YSSW control pin. High: RGB input system selected Low: YCbCr input system selected VILMAX = 1V VIHMIN = 3V
21	YM		YMSW control pin. High: -6dB signal selected Low: 0dB signal selected VILMAX = 1V VIHMIN = 3V

Pin No.	Symbol	Equivalent circuit	Description															
22	SIG OUT		Output pin for SIG1, SIG2, and SIG3. Output input signal of 6dB. Signal APL becomes 4.4V at output.															
23	Vcc		Vcc pin.															
24	SIG1 IN																	
26	SIG2 IN		Composite video signal input pins. Inputs 1Vp-p (100% white including sync) signals via capacitors.															
28	SIG3 IN																	
25	SEL1		Control pins for 3 input composite video signal output selection switch.															
27	SEL2		<table> <tr> <td>SEL1</td> <td>SEL2</td> <td>SIG OUT</td> </tr> <tr> <td>Low</td> <td>Low</td> <td>SIG1</td> </tr> <tr> <td>High</td> <td>Low</td> <td>SIG2</td> </tr> <tr> <td>Low</td> <td>High</td> <td>SIG3</td> </tr> <tr> <td>High</td> <td>High</td> <td>Prohibited</td> </tr> </table> <p>VILMAX = 0.5V VIHMIN = 3.5V</p>	SEL1	SEL2	SIG OUT	Low	Low	SIG1	High	Low	SIG2	Low	High	SIG3	High	High	Prohibited
SEL1	SEL2	SIG OUT																
Low	Low	SIG1																
High	Low	SIG2																
Low	High	SIG3																
High	High	Prohibited																

**Electrical Characteristics****Setting Conditions ( $T_a = 25^\circ\text{C}$ ,  $V_{cc} = 9\text{V}$ ,  $\text{GND} = 0\text{V}$ )**

No.	Symbol	Item	Measurement conditions	Measurement pin	Measurement contents	Min.	Typ.	Max.	Unit
1	I <sub>cc</sub>	Current consumption	$V_{cc} = 9\text{V}$ , CLP: clamp pulse (0 to 5V) input SW1, SW2, SW3: OFF	23	Measure the pin inflow current.	13	16.9	22.5	mA
2	Gybr1	$Y_1 \text{ IN}, C_{b1} \text{ IN}, C_{r1} \text{ IN} \rightarrow Y \text{ OUT}, C_{b} \text{ OUT}, C_{r} \text{ OUT}$ Input/output gain	$Y_1 \text{ IN}, C_{b1} \text{ IN}, C_{r1} \text{ IN}: 200\text{kHz}, 0.7\text{Vp-p CW}$ (4.35V bias) input	16 17 18	Measure output amplitude $V_{out1}$ . Specified at 20 log ( $V_{out1}/0.7\text{Vp-p}$ ).	5.5	6	6.5	dB
3	Gybr2	$Y_2 \text{ IN}, C_{b2} \text{ IN}, C_{r2} \text{ IN} \rightarrow Y \text{ OUT}, C_{b} \text{ OUT}, C_{r} \text{ OUT}$ Input/output gain	$Y_2 \text{ IN}, C_{b2} \text{ IN}, C_{r2} \text{ IN}: 200\text{kHz}, 0.7\text{Vp-p CW}$ (4.35V bias) input INPUT SEL (V1): 0V	16 17 18	Measure output amplitude $V_{out2}$ . Specified at 20 log ( $V_{out2}/0.7\text{Vp-p}$ ).	5.5	6	6.5	dB
4	Grgb	For R IN, G IN, B IN input → $Y \text{ OUT}$ output gain	R IN, G IN, B IN: 200kHz, 0.7Vp-p CW input YS (V3): 5V	16	Measure output amplitude $V_y$ . Specified at 20 log ( $V_y/0.7\text{Vp-p}$ ).	5.5	6	6.5	dB
5	Gsig	SIG1 IN SIG2 IN → SIG OUT input/output gain SIG3 IN	SIG1 IN, SIG2 IN, SIG3 IN: 200 kHz, 0.7Vp-p CW input SEL1 (V5): 0V, 5V, 0V SEL2 (V6): 0V, 0V, 5V	22	Measure the respective output amplitude $V_{sig}$ when SIG1 IN, SIG2 IN and SIG3 IN are output selected. Specified at 20 log ( $V_{sig}/0.7\text{Vp-p}$ ).	5.5	6	6.5	dB
6	Gym	$Y_1 \text{ IN}, C_{b1} \text{ IN}, C_{r1} \text{ IN} \rightarrow Y \text{ OUT}, C_{b} \text{ OUT}, C_{r} \text{ OUT}$ YM gain	$Y_1 \text{ IN}, C_{b1} \text{ IN}, C_{r1} \text{ IN}: 200\text{kHz}, 0.7\text{Vp-p CW}$ (4.35V bias) input YM (V4): 5V	16 17 18	Measure output amplitude $V_{ym}$ . Specified at 20 log ( $V_{ym}/V_{out1}$ ).	-6.5	-6	-5.5	dB

### Electrical Characteristics Measurement Circuit

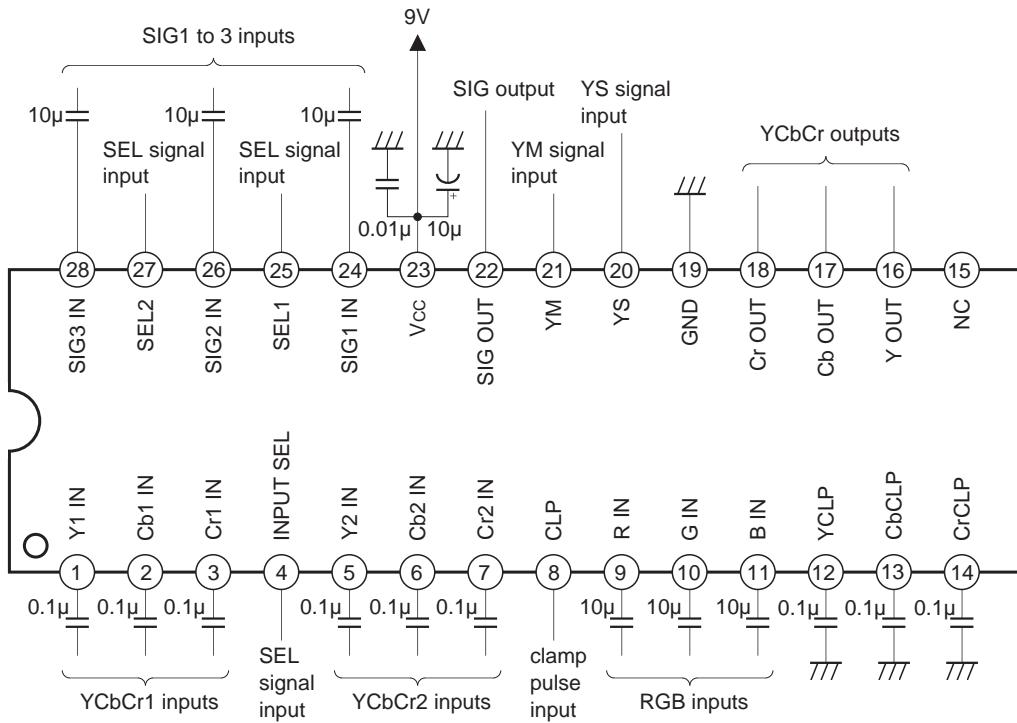


**Note:** Set as follows unless otherwise specified in the measurement conditions column of Electrical Characteristics.

V1 = 5V, V2 = 3.8V, V3 = V4 = V5 = V6 = 0V,

SW1, SW2, SW3: ON,

( are all GND.

**Application Circuit**

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

## Description of Operation

The CXA2119M has two input systems for the YCbCr signal (Y1, Cb1, Cr1 IN: Pins 1 to 3; Y2, Cb2, Cr2 IN: Pins 5 to 7). These two signals (specified input level: 100% color bar, 0.7Vp-p) are input via capacitors, and are clamped to approximately 4V at the timing of the CLP pulse input to CLP (Pin 8). After clamping, they pass the 6dB amplifier, and one system is selected by INPUT SEL (Pin 4) control. The selected YCbCr signal is controlled by YM (Pin 21) for 0/-6dB, then is input to the YS circuit.

The CXA2119M also has one RGB signal input system (R, G, B IN: Pins 9 to 11). This RGB signal (specified input level: 100 IRE, 0.7Vp-p) is input to the IC via a capacitor, and is matrix converted to a YCbCr signal from the RGB signal.

The conversion formula is:

$$Y = 0.299R + 0.587G + 0.114B$$

$$Cb = 0.564 (-0.299R - 0.587G + 0.886B)$$

$$Cr = 0.713 (0.701R - 0.587G - 0.114B)$$

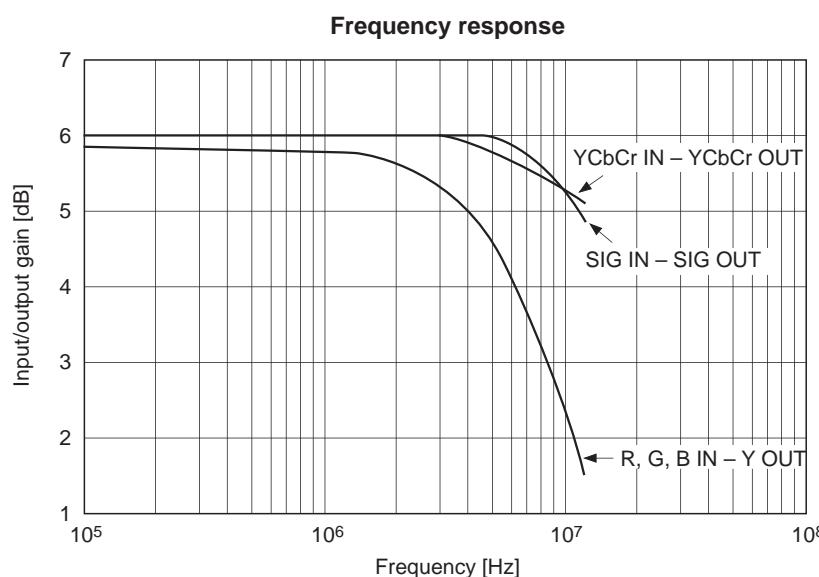
Then, the converted YCbCr signal passes the 6dB amplifier, and the capacitors connected to Y, Cb and Cr CLP (Pins 12 to 14) are used to clamp it, and it is input to the YS circuit.

The Y1Cb1Cr1/Y2Cb2Cr2 signal or the Y1Cb1Cr signal converted from RGB input is selected by YS (Pin 20) control. The selected signal is output to Y, Cb and Cr OUT (Pins 16 to 18). Signal pedestal level at output is approximately 3.8V.

The CXA2119M has three inputs for composite video signal input (SIG1, SIG2, SIG3 IN: Pins 24, 26, 28). These signals (specified input level: 1Vp-p (including sync)) are input to the IC via capacitors, and the signal selected by SEL1 (Pin 25) and SEL2 (Pin 27) control is output via the 6dB amplifier from SIG OUT (Pin 22).

(Refer to the Pin Description for the Truth Table for each switch.)

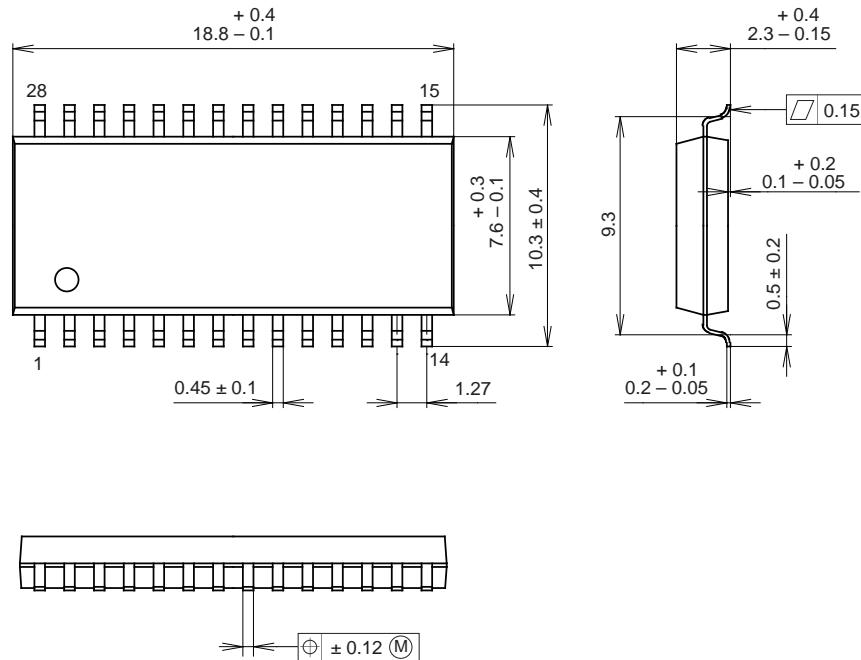
## Example of Representative Characteristics



**Package Outline**

Unit: mm

28PIN SOP (PLASTIC) 375mil



## PACKAGE STRUCTURE

SONY CODE	SOP-28P-L04
EIAJ CODE	*SOP028-P-0375-D
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.7g