SONY

SP5T SOI Antenna Switch for WCDMA Diversity

CXA2985GC

Description

The CXA2985GC is a low power SP5T antenna switch for WCDMA diversity switching applications.
The CXA2985GC has a 1.8 V CMOS compatible decoder.
The Sony Silicon On Insulator (SOI) technology is used for low insertion loss.

Features

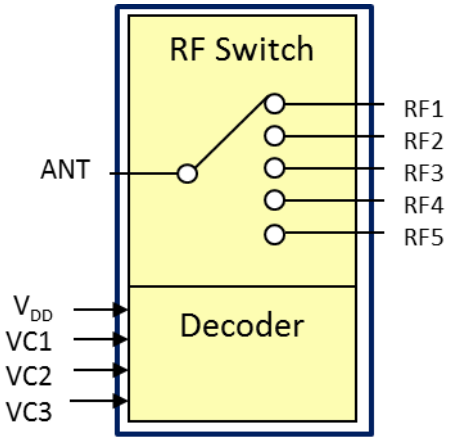
- ◆Low Insertion loss : 0.35 dB (typ.) at 800 MHz
  0.42 dB (typ.) at 2 GHz
  0.55 dB (typ.) at 2.7 GHz
- ◆No DC Blocking Capacitors (except sourcing DC bias)
- ◆Bump Pitch = 0.4 mm
- ◆Small Flip-Chip Size : 1.5 mm × 1.5 mm × 0.35 mm Typ.
- ◆Lead-Free and RoHS compliant

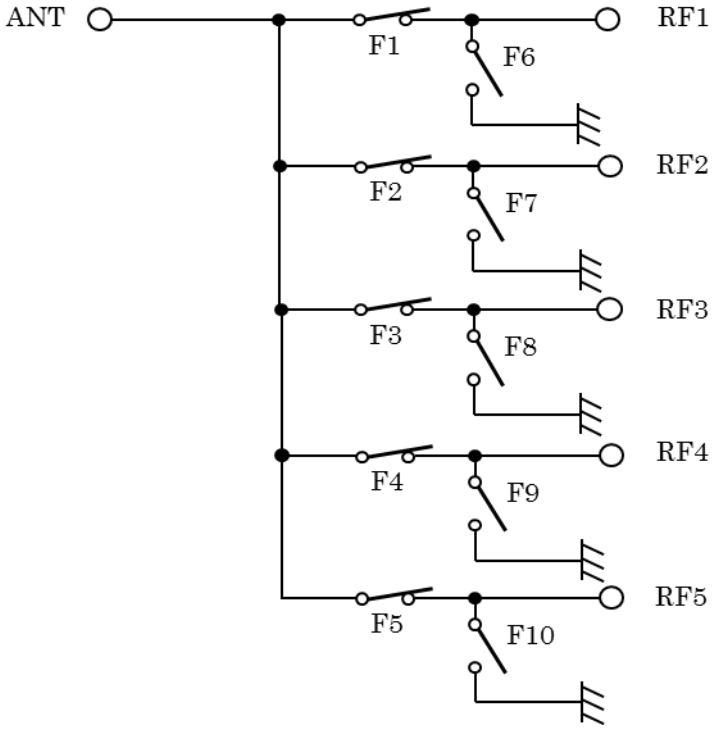
Structure

SOI CMOS MMIC

This IC is ESD sensitive device. Special handling precautions are required

Block Diagram

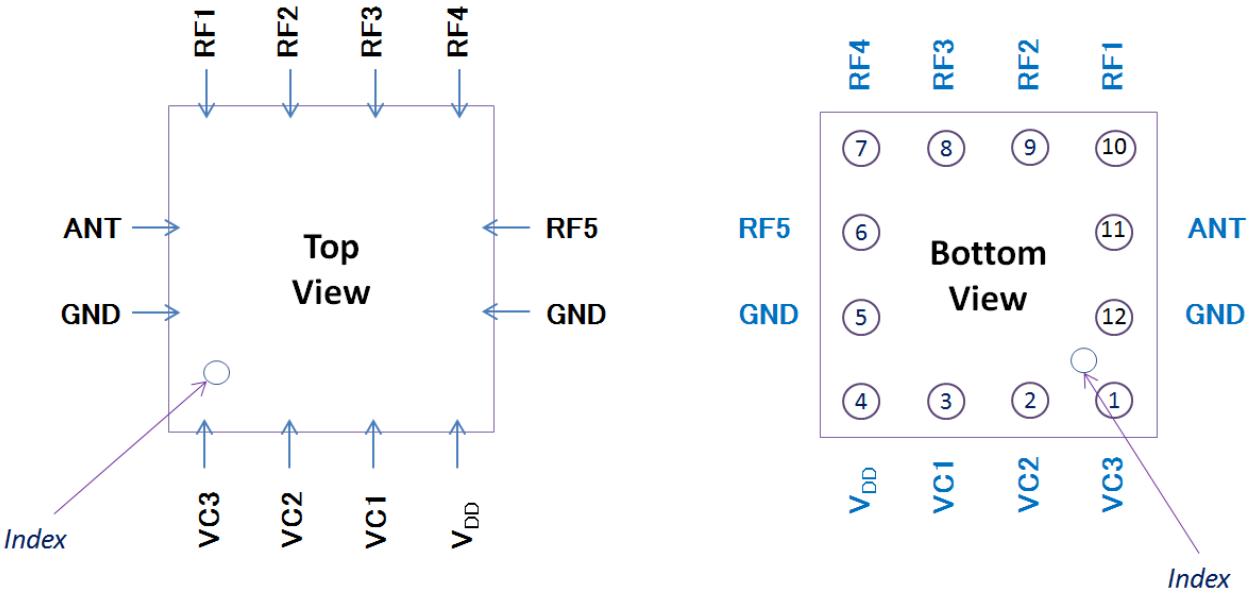




Truth Table

State	ON Path	VC1	VC2	VC3	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
1	ANT-RF1	H	L	H	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON
2	ANT-RF2	H	H	L	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON
3	ANT-RF3	H	L	L	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON
4	ANT-RF4	L	L/H	L	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON
5	ANT-RF5	L	L/H	H	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF

Pin Configuration



Absolute Maximum Ratings

◆Supply voltage	V_{DD}	4	V	(Ta = 25 °C)
◆Control voltage	VC	4	V	(Ta = 25 °C)
◆Maximum input		30	dBm	(Ta = 25 °C, V_{DD} = 2.5 to 3.3 V)
◆Operating temperature	Topr	–35 to +90	°C	
◆Storage temperature	Tstg	–65 to +150	°C	

DC Bias Condition

(Ta = 25 °C)

Parameter	Min.	Typ.	Max.	Unit
V_{DD}	2.5	2.8	3.3	V
VC(H)	1.3	1.8	3.3	V
VC(L)	0	-	0.45	V

Electrical Characteristics

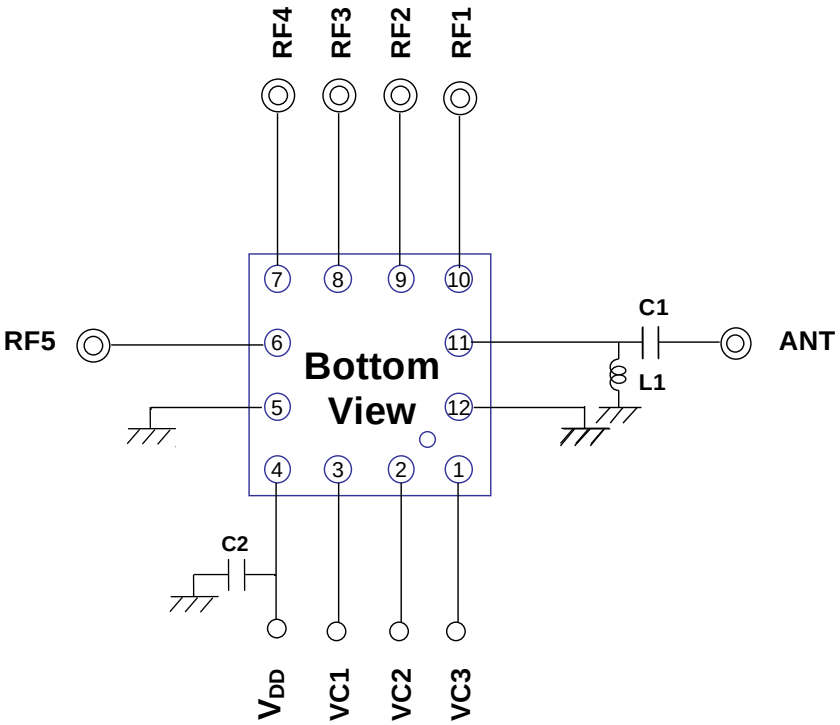
(V_{DD} = 2.5 V, Ta = 25 °C)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	ANT – RF1	*1	—	0.35	0.45	dB
			*2, *3	—	0.48	0.63	
			*4	—	0.65	0.80	
		ANT – RF2	*1	—	0.35	0.45	
			*2, *3	—	0.42	0.57	
			*4	—	0.55	0.70	
		ANT – RF3	*1	—	0.35	0.45	
			*2, *3	—	0.43	0.58	
			*4	—	0.56	0.71	
		ANT – RF4	*1	—	0.35	0.45	
			*2, *3	—	0.45	0.60	
			*4	—	0.59	0.74	
		ANT – RF5	*1	—	0.35	0.45	
			*2, *3	—	0.44	0.59	
			*4	—	0.56	0.71	
Isolation	ISO.	ANT – RF1-2	*1	25	31	—	dB
			*2, *3	19	23	—	
			*4	16	20	—	
		ANT – RF3-5	*1	30	40	—	
			*2, *3	25	30	—	
			*4	22	27	—	
VSWR	VSWR		824 to 2690 MHz	—	1.3	1.6	—
Harmonics	2fo	ANT – RF1-5	*1	—	-64	-40	dBm
	3fo			—	-64	-40	
	2fo		*2, *3	—	-64	-40	
	3fo			—	-64	-40	
	2fo		*4	—	-64	-40	
	3fo			—	-64	-40	
Inter Modulation Product Power in Rx Band	IMD2	ANT – RF1-5	*5, *13	—	—	-105	dBm
			*6-8, *13	—	—	-105	
	IMD3		*9, *13	—	—	-105	
			*10-12, *13	—	—	-105	
Control Current	Ictl		Vctl = 1.8 V per line	—	0.05	2	μ A
Supply Current	Idd		V_{DD} = 2.5 V	—	12	30	μ A
Switching Speed	Swt		50 % VC to 90 % RF	—	3	5	μ s

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

* 1 Pin = 26 dBm, freq = 704 to 915 MHz
* 2 Pin = 26 dBm, freq = 1710 to 1910 MHz
* 3 Pin = 26 dBm, freq = 1920 to 1980 MHz
* 4 Pin = 26 dBm, freq = 2500 to 2570 MHz
* 5 Pin on RF: 20 dBm, 835 MHz, Pin on ANT: -15 dBm, 45 MHz
* 6 Pin on RF: 20 dBm, 1745 MHz, Pin on ANT: -15 dBm, 95 MHz
* 7 Pin on RF: 20 dBm, 1880 MHz, Pin on ANT: -15 dBm, 80 MHz
* 8 Pin on RF: 20 dBm, 1950 MHz, Pin on ANT: -15 dBm, 190 MHz
* 9 Pin on RF: 20 dBm, 835 MHz, Pin on ANT: -15 dBm, 790 MHz
* 10 Pin on RF: 20 dBm, 1745 MHz, Pin on ANT: -15 dBm, 1650 MHz
* 11 Pin on RF: 20 dBm, 1880 MHz, Pin on ANT: -15 dBm, 1800 MHz
* 12 Pin on RF: 20 dBm, 1950 MHz, Pin on ANT: -15 dBm, 1760 MHz
* 13 Measured with the recommended circuit

Recommended Circuit



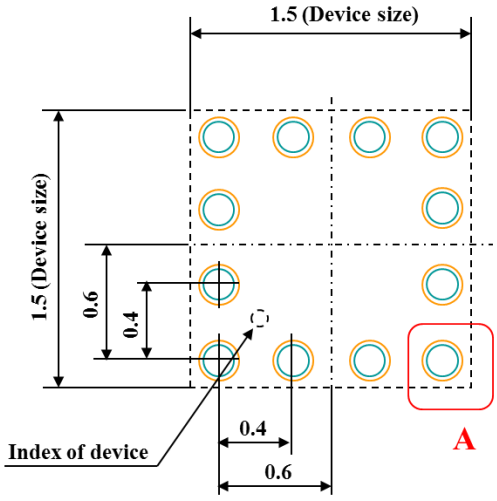
*1: No DC blocking capacitors are required on all RF ports.
*2: DC levels of all RF ports are GND.
*3: L1 (27 nH) and C1 (6.8 pF) are recommended on Ant port for ESD protection.
*4: C2(100 pF) is recommended on V_{DD} pin for Decoupling Capacitor.

Solder Bump Foot Print (Macro) Reference

Device specification

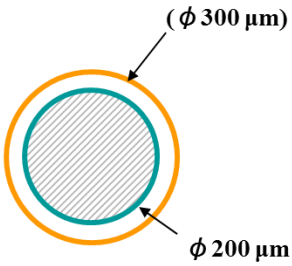
- Device size : 1.5 mm × 1.5 mm × t 0.35 mm
- Pin counts : 12 Pin
- Solder Bump height : 0.15 mm
- Solder Bump ball size : ϕ0.2 mm
- Solder Bump pitch : 0.4 mm

Unit:mm



Detail - A

- Land size (Resist Open area) : ϕ200 µm
- Cu pattern size : (ϕ300 µm)

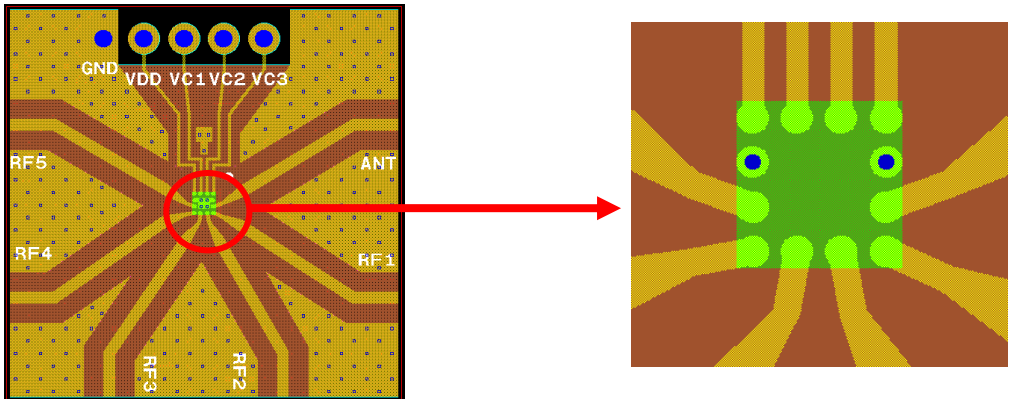


: Cu pattern

: Resist open

: Solder print area (Metal mask thickness : 110 µm)

Recommended PCB Layout



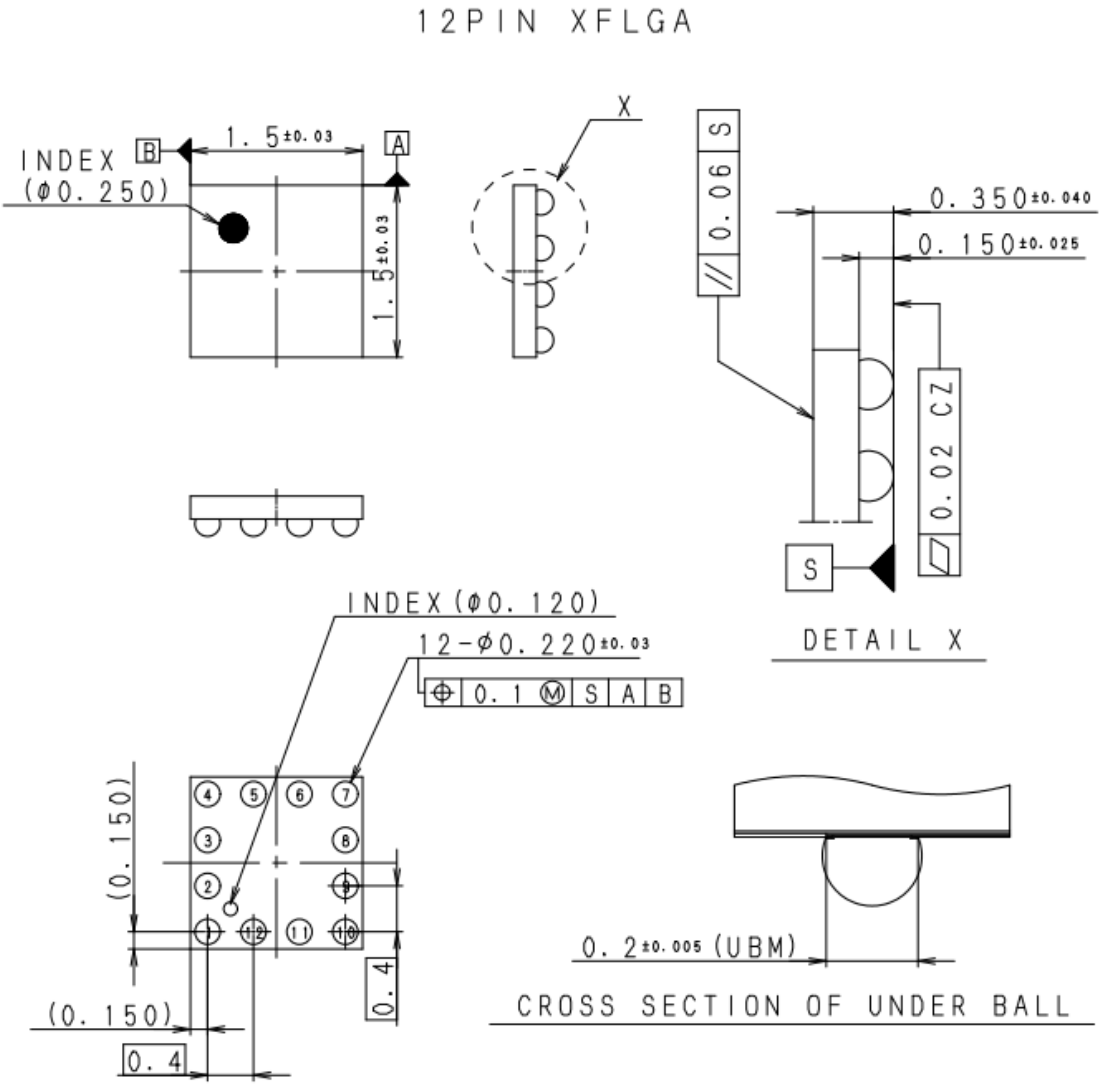
Device Area

Via

Metal Pattern

Package Outline

(Unit: mm)



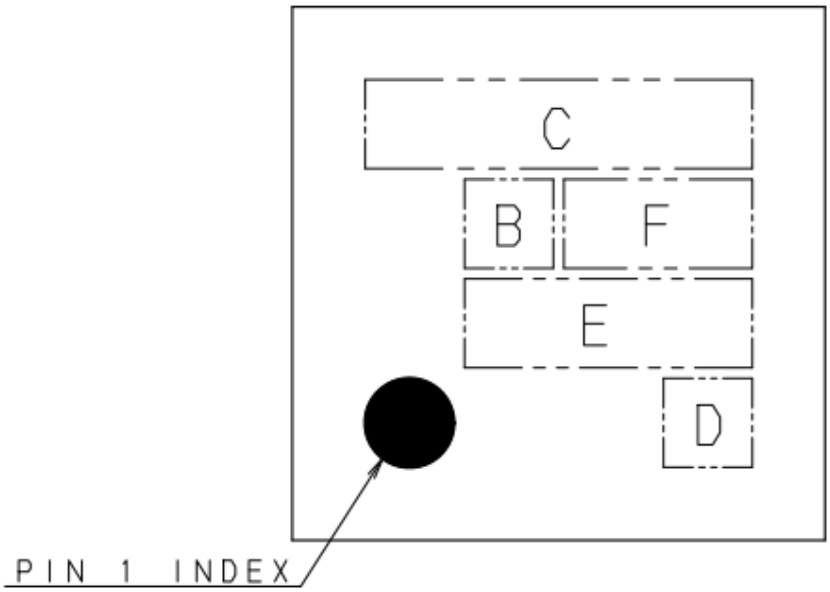
PACKAGE STRUCTURE

SONY CODE	XFLGA-12S-432
JEITA CODE	S-XFLGA12-1.5x1.5-0.4
JEDEC CODE	————

PACKAGE MATERIAL	Si SUBSTRATE
TERMINAL MATERIAL	Sn-3.0Ag-0.5Cu
PACKAGE MASS	0.0014g

PART No. AP-2000-12LGAS2	Rev. 0
ISSUED 12.06.21	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:GX-12-CAS	

Marking



MARKING C: 2985

注1） C部は製品名（Ｍａｘ４文字）を配置する。
（４文字を超える場合は製品名省略標示規定に従う。）
2） B部は製造年（１文字）を配置する。
3） D部は組立場所記号（１文字）を配置する。
4） E部は通し記号（ＭＡＸ３文字）を配置する。
5） F部は製造週（ＭＡＸ２文字）を配置する。

< INSTRUCTIONS >
1) TYPE NO. (MAX 4 CHARACTERS) IN SECTION C.
(FOR MORE THAN 4 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) MANUFACTURING YEAR (1 CHARACTER) IN SECTION B.
3) ASSEMBLY LOCATION CODE (1 CHARACTER) IN SECTION D.
4) SERIAL CODE (MAX 3 CHARACTERS) IN SECTION E.
5) MANUFACTURING WEEK (MAX 2 CHARACTERS) IN SECTION F.

Note

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits