SONY

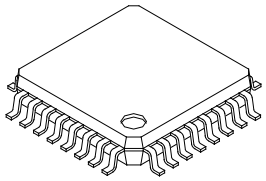
CXB1572Q

Post amplifier for Optical Fiber Communication Receiver

Description

The CXB1572Q achieves the 2R optical-fiber communication receiver functions (Reshaping and Regenerating) on a single chip. This IC is also equipped with the signal interruption alarm output function, which is used to discriminate the existence of data input.

32 pin QFP (Plastic)



Features

- Auto-offset canceler circuit
- Signal interruption alarm output
- 2-level switching function of identification maximum voltage amplitude for alarm block
- Single 3.3 V power supply

Applications

- FDDI : 125 Mb/s
- SONET/SDH : 155.52 Mb/s
- ESCON : 200 Mb/s
- Fiber channel : 265.625 Mb/s
- ATM : 155.52 Mb/s

Absolute Maximum Ratings

• Supply voltage	$V_{CC} - V_{EE}$	–0.3 to +7.0	V
• Storage temperature	Tstg	–65 to +150	°C
• Input voltage difference : $\lvert V_D - V_{\overline{D}} \rvert$	Vdif	0 to +2.5	V
• SW input voltage	Vi	V_{EE} to V_{CC}	V
• Output current (Continuous)	I_O	0 to 50	mA
(Surge current)		0 to 100	mA

Recommended Operating Conditions

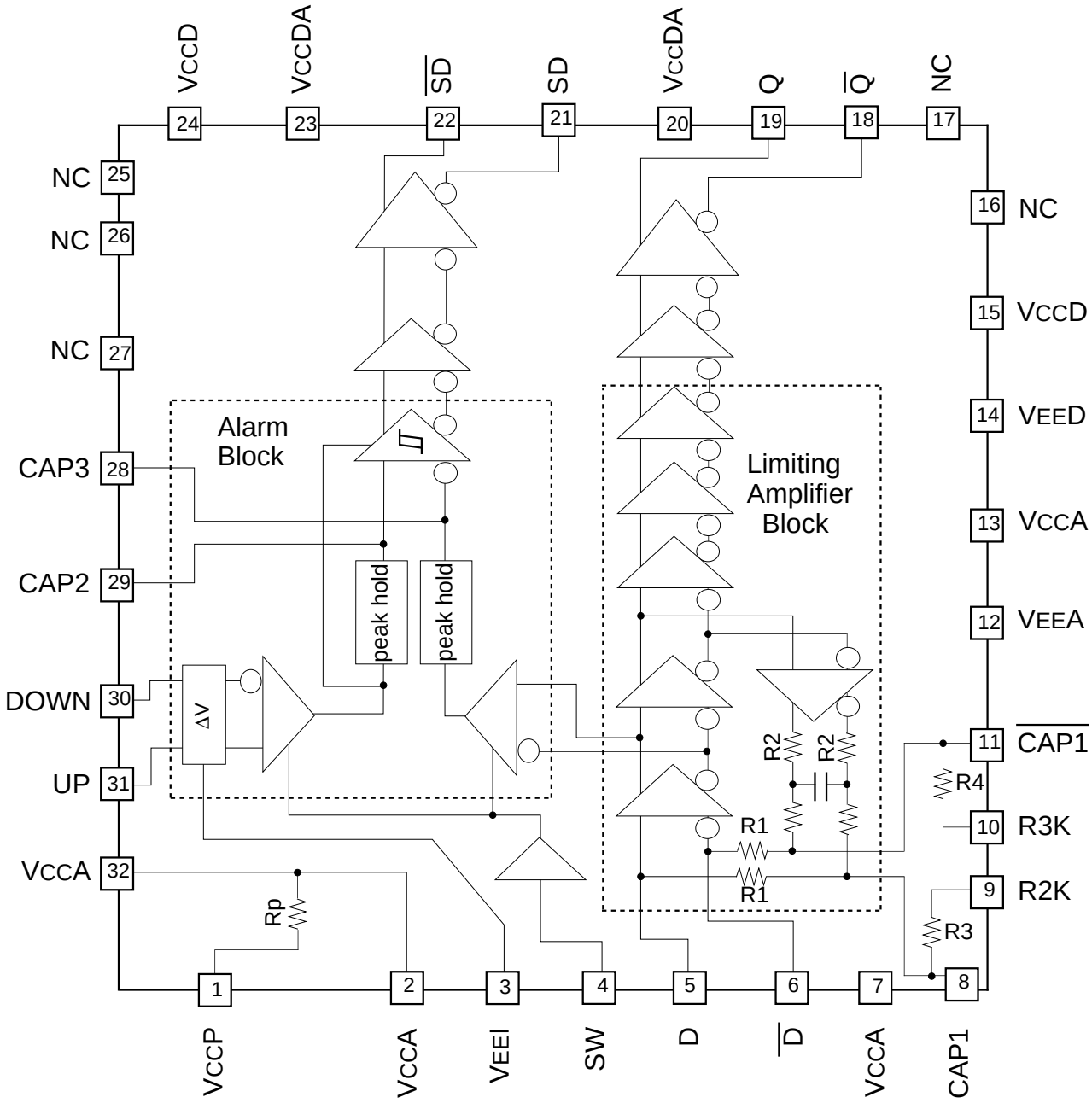
• Supply voltage	$V_{CC} - V_{EE}$	3.0 to 3.6	V
• Termination voltage (for data/alarm)	$V_{CC} - V_{T1}$	1.8 to 2.2	V
• Termination voltage (for alarm 2)	V_{T2}	V_{EE}	V
• Termination resistance (for data/alarm)	R_{T1}	46 to 56	Ω
• Termination resistance (for alarm 2)	R_{T2}	460 to 560	Ω
• Operating temperature	Ta	–40 to +85	°C

Structure

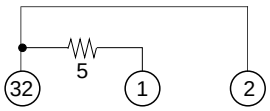
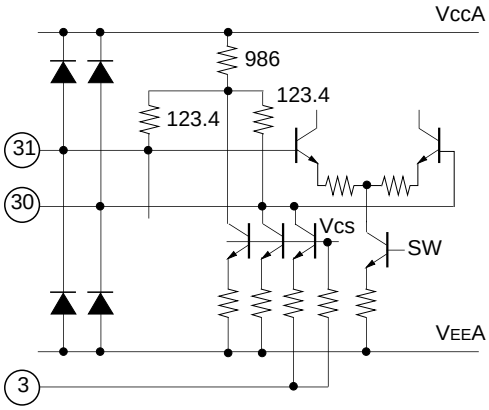
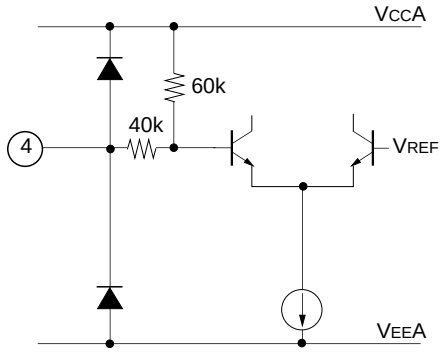
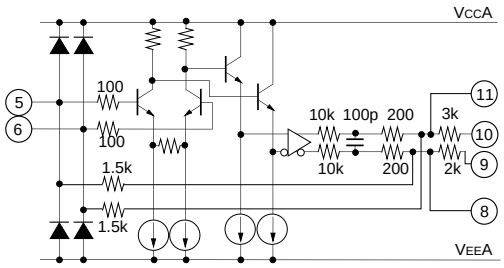
Bipolar silicon monolithic IC

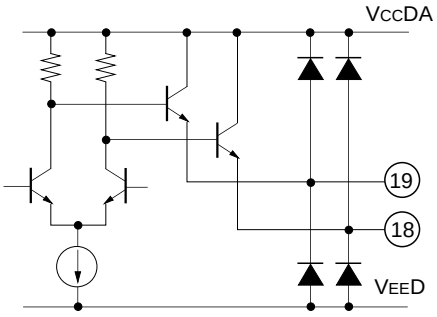
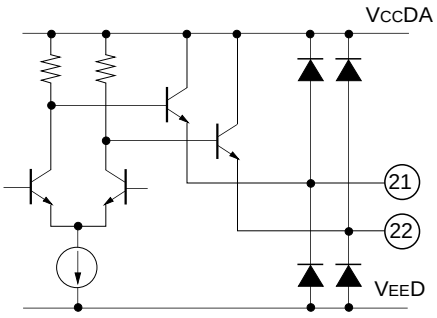
E96638-TE

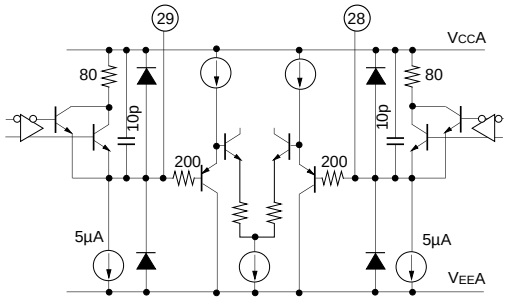
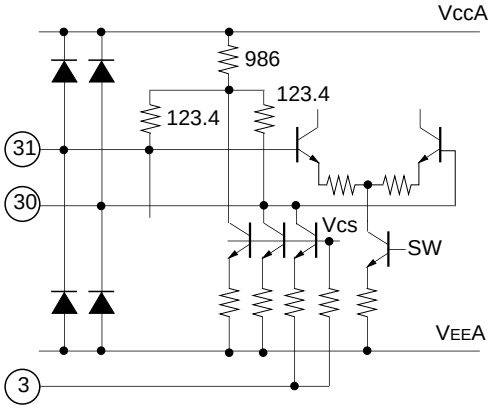
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
1	$V_{CC}P$				Positive power supply for external power supply.
2	$V_{CC}A$	0 V			
3	$V_{EE}I$	–3.3 V			Generates the default voltage between UP and DOWN. The voltage (5.3 mV for input conversion) can be generated between UP and DOWN (Pins 30 and 31) as alarm setting level 1 by this pin to Open. The voltage (12 mV for input conversion) can be generated as alarm setting level 2 by connecting this pin to $V_{EE}A$.
4	SW	0 V (OPEN) or –3.3 V			Switches the identification maximum voltage amplitude. High voltage when open; the identification maximum voltage amplitude becomes 50 mVp-p. Low voltage when connecting this pin to V_{EE}; the amplitude becomes 20 mVp-p.
5	D	–1.3 V	–0.9 V to –1.7 V		Limiting amplifier block input. Be sure to make this input with AC coupled.
6	$\overline{D}$	–1.3 V	–0.9 V to –1.7 V		
7	$V_{CC}A$	0 V			Positive power supply for analog block.
8	CAP1	–1.8 V			Pins 8 and 11 connect a capacitor which determines the cut-off frequency for feedback block, and 2 kΩ is connected between Pins 8 and 9; 3 kΩ between Pins 10 and 11. A resistor which is to be inserted in parallel with a capacitor can be selected 5 ways by external wiring, and DC feedback gain can be varied due to compensate the input duty cycle distortion.
9	R2K				
10	R3K				
11	$\overline{CAP1}$	–1.8 V			

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
12	$V_{EE}A$	–3.3 V			Negative power supply for analog block.
13	$V_{CC}A$	0 V			Positive power supply for analog block.
14	$V_{EE}D$	–3.3 V			Negative power supply for digital block.
15	$V_{CC}D$	0 V			Positive power supply for digital block.
16	NC				No connected.
17					
18	$\overline{Q}$		–0.9 V to –1.7 V		Data signal output. Terminate this pin in 50 Ω at V_{TT} = –2 V.
19	Q		–0.9 V to –1.7 V		
20	VccDA	0 V			Positive power supply for output buffer.
21	SD		–0.9 V to –1.7 V		Alarm signal output. Terminate this pin in 50 Ω at V_{TT} = –2 V.
22	$\overline{SD}$		–0.9 V to –1.7 V		
23	VccDA	0 V			Positive power supply for digital block.
24	VccD	0 V			Positive power supply for digital block.
25	NC				No connected.
26					
27					

Pin No.	Symbol	Typical pin voltage (V)		Equivalent circuit	Description
		DC	AC		
28	CAP3	–1.8 V			Connects a peak hold circuit capacitor for alarm block. 470 pF should be connected to VccA each. CAP2 pin → Peak hold capacitor connection for alarm level setting block. CAP3 pin → Peak hold capacitor connection for limiting amplifier signal.
29	CAP2	–1.8 V			
30	DOWN	–1090 mV (for VEEI = –3.3 V)			Connects a resistor for alarm level setting. Default voltage can be generated without an external resistor. (Please refer to pin description of pin No. 3.)
31	UP	–1020 mV (for VEEI = –3.3 V)			
32	VccA	0 V			Positive power supply for analog block.

Electrical Characteristics

• **DC characteristics**

(V_{CC} = GND, V_{EE} = –3.0 V to –3.6 V, Ta = –40 to +85 °C, V_{CC} = V_{CC}D, V_{CC}DA, V_{CC}A V_{EE} = V_{EE}D, V_{EE}A)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply	I_{EE}		–56	–40	–29	mA
Q/$\overline{Q}$ SD/$\overline{SD}$ High output voltage	V_{OH}	R_{T1} = 51 Ω, V_{T1} = V_{CC}–2 V termination, Ta=0 to 85 °C	–1025		–830	mV
Q/$\overline{Q}$ SD/$\overline{SD}$ Low output voltage	V_{OL}		–1810		–1550	
SD/$\overline{SD}$ High output voltage 2	V_{OHb}	R_{T2} = 510 Ω, V_{T2} =V_{EE} termination, Ta=0 to 85 °C	–1025		–700	
SD/$\overline{SD}$ Low output voltage 2	V_{OLb}		–1860		–1500	
SW High input voltage	V_{IH}		–500		0	
SW Low input voltage	V_{IL}		V_{EE}		V_{EE}+500	
SW High input current	I_{IH}				2	µA
SW Low input current	I_{IL}		–60			
D/$\overline{D}$ input resistance	Rin		1109	1479	1849	Ω
Internal resistance 1 for alarm level setting	Ra1	Refer to Fig. 3.	739	986	1233	
Internal resistance 2 for alarm level setting	Ra2A, B	Refer to Fig. 3.	93	123	154	
Resistance between V_{CC}A and V_{CC}P	RP		3.3	5	6.9	
Pare ratio of internal resistance 2 for alarm level setting	δRa2	Ra2A/Ra2B	0.97		1.03	
Resistance between CAP1 and R2K	R3		1470	1970	2470	Ω
Resistance between $\overline{CAP1}$ and R3K	R4		2210	2960	3700	

• **AC characteristics**

(V_{CC} = GND, V_{EE} = –3.0 V to –3.6 V, Ta = –40 to +85 °C, V_{CC} = V_{CC}D, V_{CC}DA, V_{CC}A V_{EE} = V_{EE}D, V_{EE}A)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum input voltage amplitude	Vmax	Single-ended input	1600			mVpp
Amplifier gain (except for output buffer)	GL		52			dB
Identification maximum voltage amplitude of alarm level	VminA1	SW pin: Low, single-ended input	20			mVpp
	VminA2	SW pin: Open High, single-ended input	50			
Hysteresis width	ΔP	Alarm level is default value	3	6	7	dB
SD response assert time	Tas	Low → High*1	0		100	µs
SD response deassert time	Tdas	High → Low*2	2.3		100	
SD response assert time for alarm level default	Tasd	Low → High*3	0		100	
SD response deassert time for alarm level default	Tdasd	High → Low*4	2.3		100	
Alarm setting level 1 for default	Vdef1	UP,DOWN,V_{EE}I pins ;Open,connect SW pin to V_{EE}	4.3	5.3	6.3	mV
Alarm setting level 2 for default	Vdef2	UP,DOWN,SW pins ;Open,connect V_{EE}I to V_{EE}	10.5	12.0	13.5	
Propagation delay time	T_{PD}	D to Q	1.2	1.7	2.6	ns
Q/$\overline{Q}$ SD/$\overline{SD}$ rise time	Tr	R_{T1} = 50 Ω, V_{T1} = V_{CC}–2 V termination, V_{EE}=–3.3 V, Ta=0 to 85 °C 20 % to 80 %	0.45	0.85	1.3	
Q/$\overline{Q}$ SD/$\overline{SD}$ fall time	Tf		0.45	0.85	1.3	

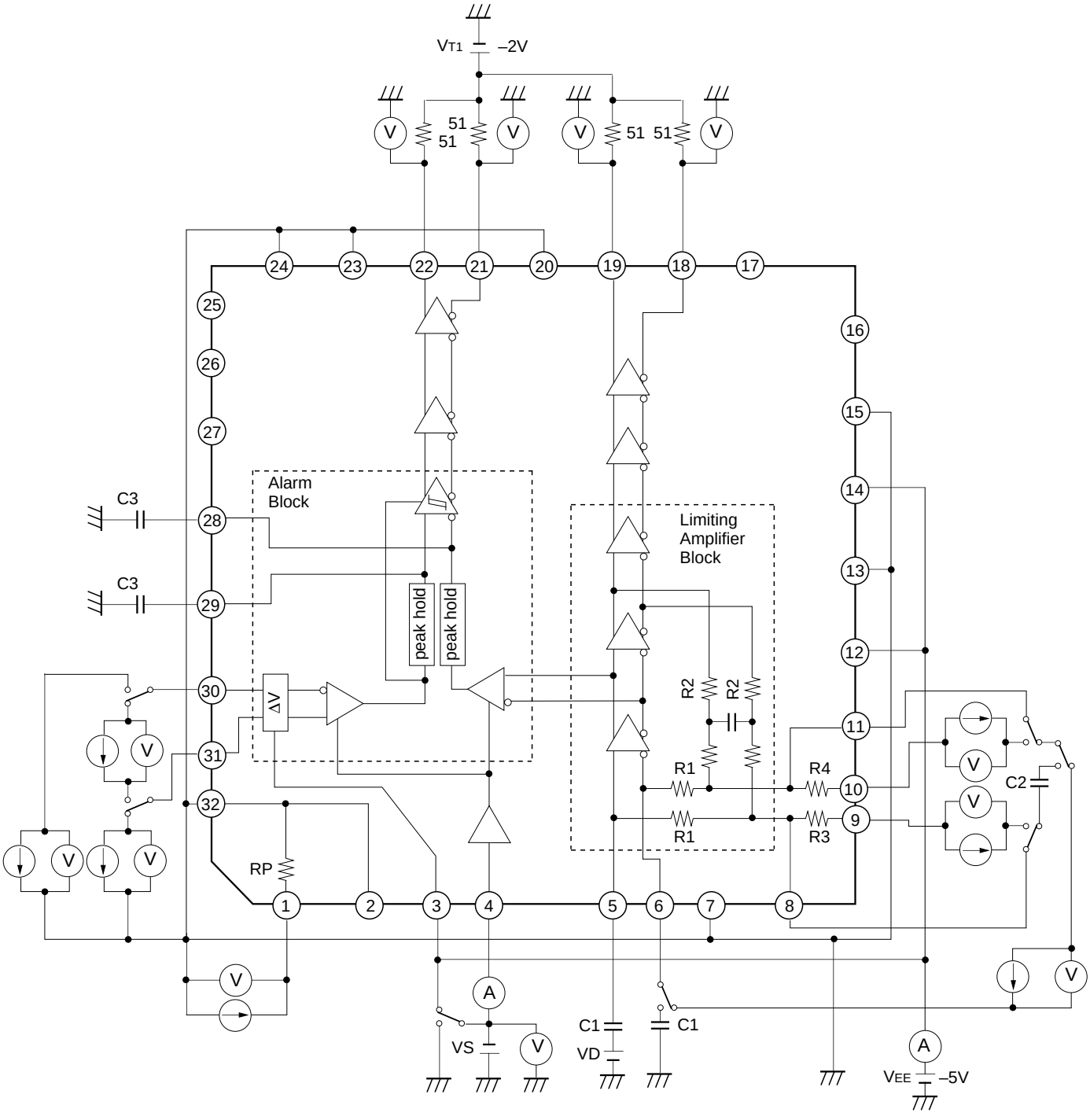
*1 V_{UP} – V_{DOWN} = 100 mV, Vin = 100 mVpp (single ended), SW pin: High
Peak hold capacitance of 470 pF; connect V_{EE}I to V_{EE}.

*2 V_{UP} – V_{DOWN} = 100 mV, Vin = 1 Vpp (single ended), SW pin: High
Peak hold capacitance of 470 pF; connect V_{EE}I to V_{EE}.

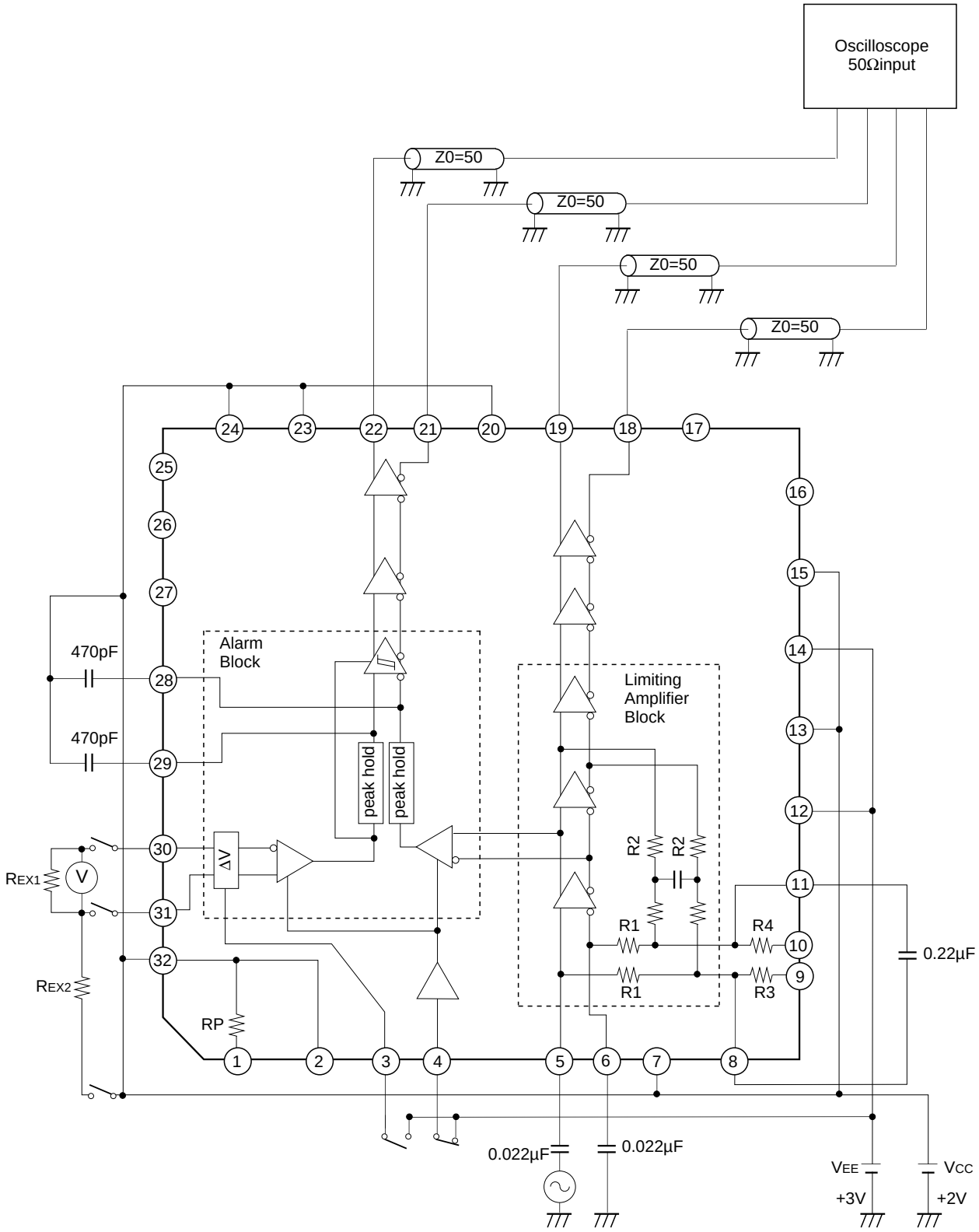
*3 Vin = 50 mVpp (single ended), SW pin: Low
Peak hold capacitance of 470 pF; connect V_{EE}I to V_{EE}.

*4 Vin = 1 Vpp (single ended), SW pin: Low
Peak hold capacitance of 470 pF; connect V_{EE}I to V_{EE}.

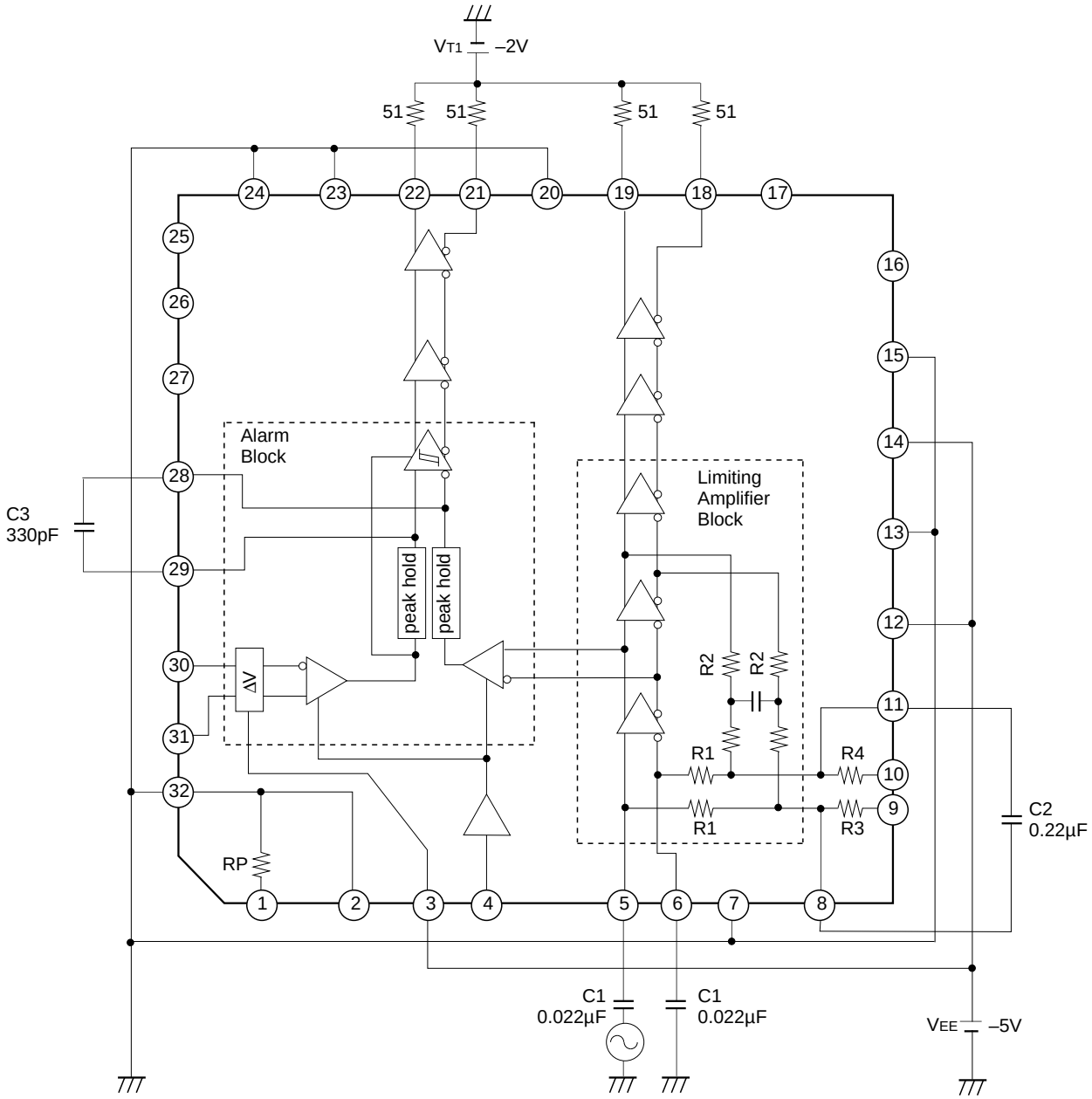
DC Electrical Characteristics Measurement Circuit



AC Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1. Limiting amplifier block

The limiting amplifier block is equipped with the auto-offset canceler circuit. When external capacitors C1 and C2 are connected as shown in Fig. 1, the DC bias is set automatically in this block. External capacitor C1 and IC internal resistor R1 determine the low input cut-off frequency f2 as shown in Fig. 2. Similarly, external capacitor C2 and IC internal resistor R2 determine the high cut-off frequency f1 for DC bias feedback. Since peaking characteristics may occur in the low frequency area of the amplifier gain characteristics depending on the f1/f2 combination, set the C1 and C2 so as to avoid the occurrence of peaking characteristics. The target values of R1 and R2 and the typical values of C1 and C2 are as indicated below. When a single-ended input is used, provide AC grounding by connecting Pin 6 to a capacitor which has the same capacitance as capacitor C1.

R1 (internal): 1.5 kΩ
C1 (external): 0.022 µF
→ f2: 4.8 kHz

R2 (internal): 10 kΩ
C2 (external): 0.22 µF
→ f1: 72 Hz

2 kΩ is incorporated between Pins 8 and 9; 3 kΩ between Pins 10 and 11. A resistance value which is to be inserted in parallel with a capacitor C2 can be selected 5 ways (∞, 5 kΩ, 3 kΩ, 2 kΩ, 2 k//3 kΩ) by external wiring, and DC feedback can be varied.

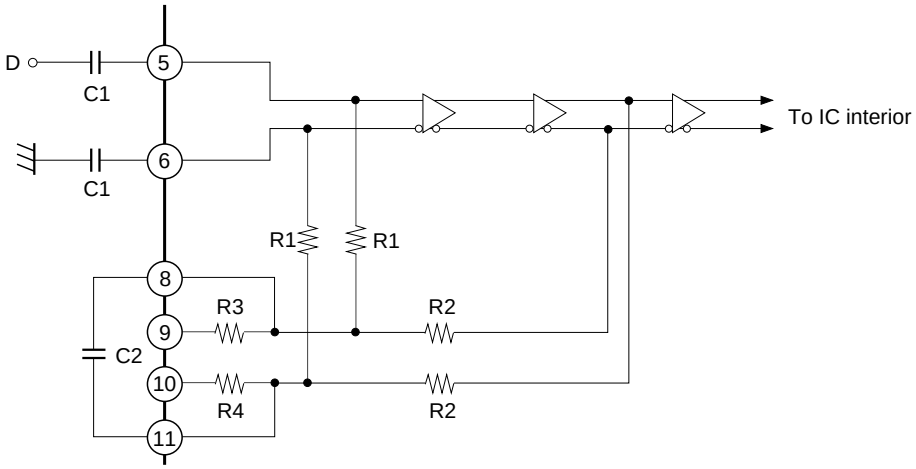


Fig. 1

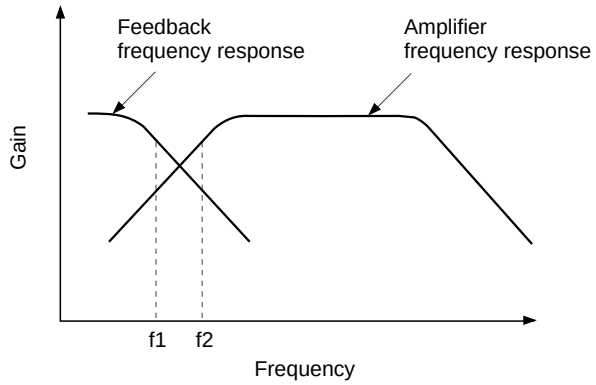


Fig. 2

2. Alarm block

In order to operate the alarm block, give the voltage difference between Pins 30 and 31 to set an alarm level and connect the peak hold capacitor C3 shown in Fig. 3.
This IC has two setting methods of alarm level; one is to leave Pins 30 and 31 open to set an alarm level default value (5.3 mV or 12 mV for input conversion). Default value of alarm level is 5.3 mV for input conversion by leaving Pin3 to open,12 mV by connecting Pin3 to V_{EE}. The other is to connect Pin 3 to V_{EE} and set a desired alarm level using the external resistors R_{EX1} and R_{EX2} and R_{EX3} shown in Fig. 3.
Connect R_{EX1} between Pins 30 and 31, or connect R_{EX3} between Pin 30 and V_{CC} when less alarm level is desired to be set than its default value; connect R_{EX2} between Pin 31 and V_{CC} potential when more alarm level is desired to be set than its default value. However, the Pin 31 voltage must be higher than that of Pin 30. Refer to Figs. 7 to 9 for this alarm level setting.
This IC also features two-level setting of identification maximum voltage amplitude for the alarm function. The amplitude is set to 50 mVp-p when Pin 4 is left open (High level) and it is set to 20 mVp-p when Pin 4 is Low level. Therefore, noise margin can be increased by setting Pin 4 to Low level when small signal is input. The relation of input voltage and peak hold output voltage is shown in Fig. 5.
In the relation between the alarm setting level and hysteresis width, the hysteresis width is designed to maintain a constant gain (design target value: 6 dB) as shown in Fig. 4. The C3 capacitance value should be set so as to obtain desired assert time and deassert time settings for the alarm signal.
The electrical characteristics for the SD response assert and deassert times are guaranteed only when the waveforms are input as shown in the timing chart of Fig. 6.
The typical values of R_{EX1}, R_{EX2}, R_{EX3} and C3 are as follows: (Approximately 10 pF capacitor is built in Pins 28 and 29 each.)

R_{EX1} : 400 Ω (when the alarm level is set to 3 mV for input conversion.Pin3; open,connect Pin4 to V_{EE})
R_{EX2} : 4k Ω (when the alarm level is set to 15 mV for input conversion.connect Pin3 to V_{EE}, Pin4; open)
R_{EX3} : 6.2 kΩ (when the alarm level is set to 3 mV for input conversion.Pin3; open,connect Pin4 to V_{EE})
C3 : 470 pF

The table below shows the alarm logic.

Optical signal input state	SD	$\overline{SD}$
Signal input	High level	Low level
Signal interruption	Low level	High level

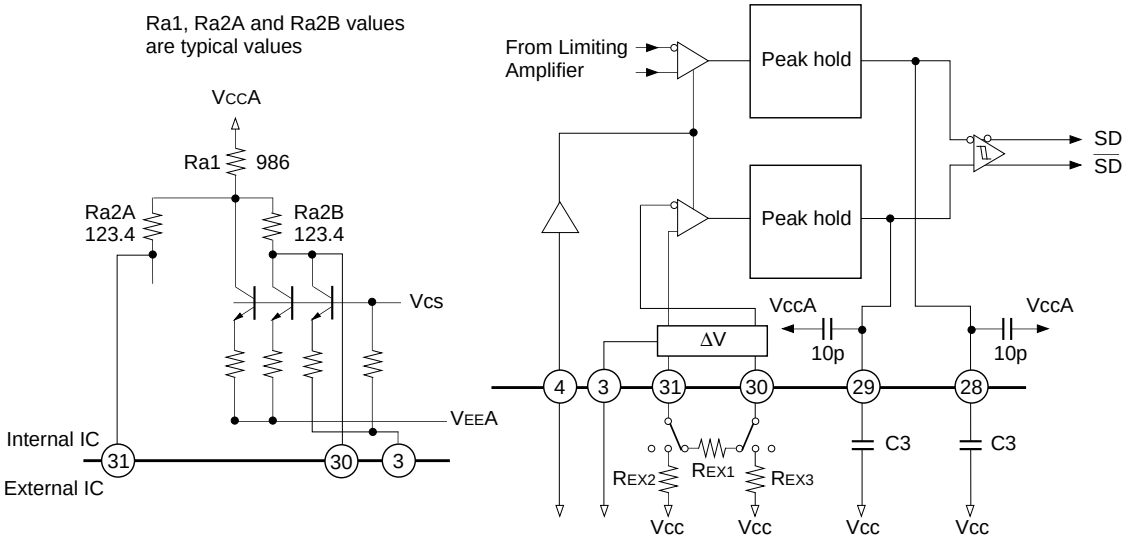


Fig. 3

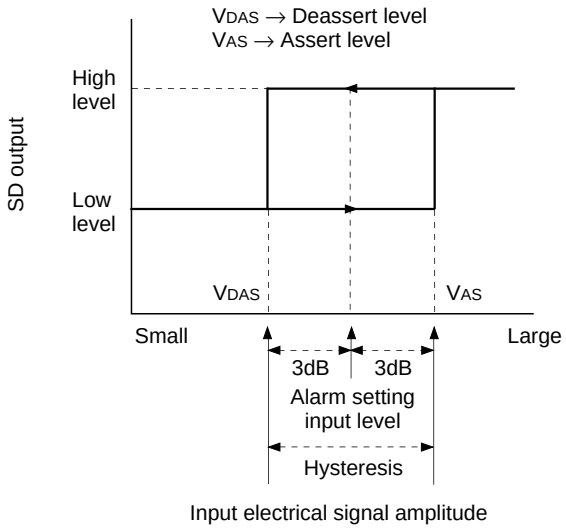


Fig. 4

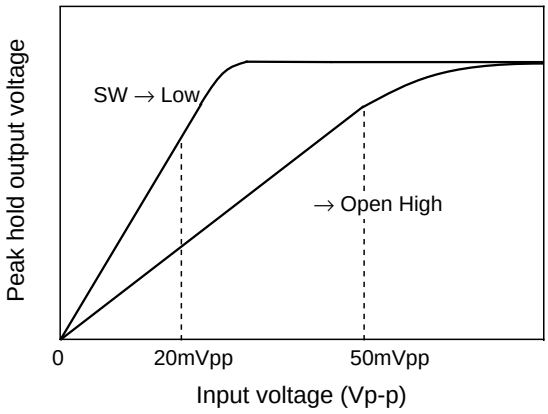


Fig. 5

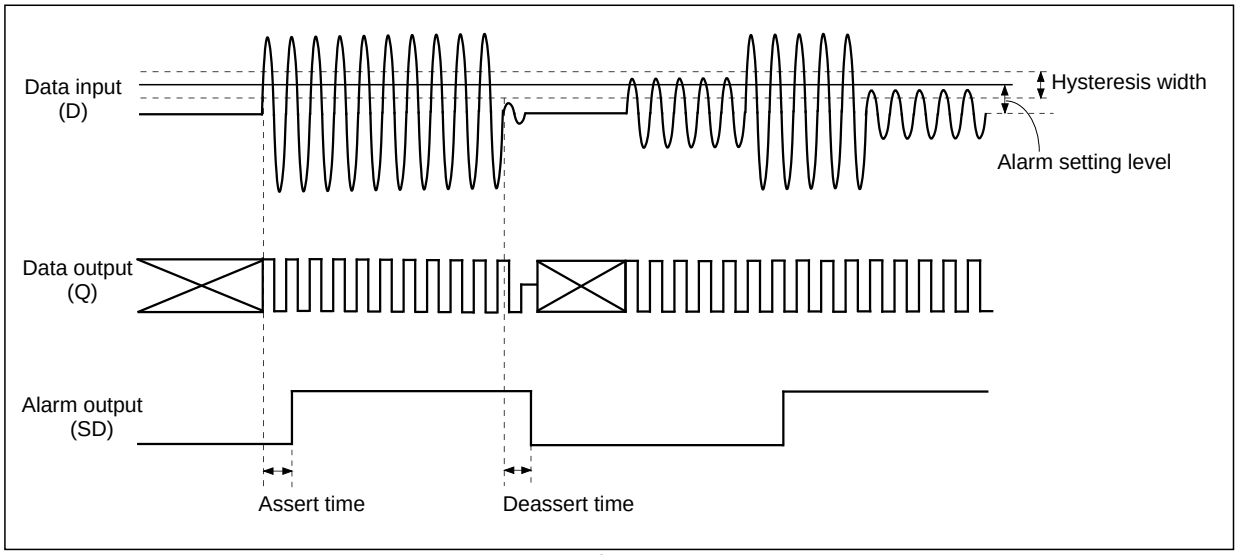


Fig. 6

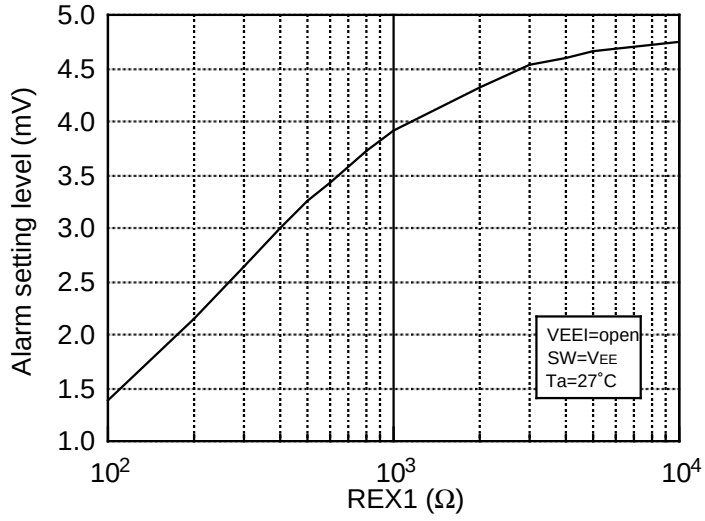


Fig. 7

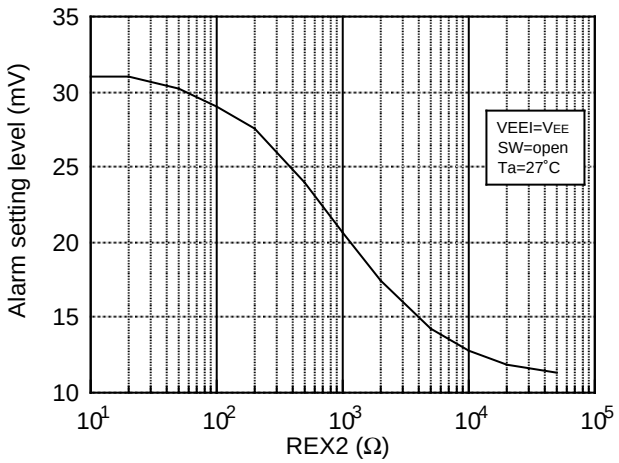


Fig. 8

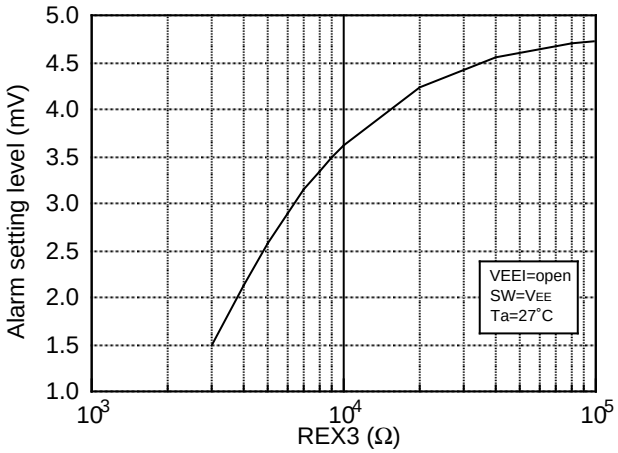


Fig. 9

3. Others

Pay attention to handling this IC because its electrostatic discharge strength is weak.

Example of Representative Characteristics

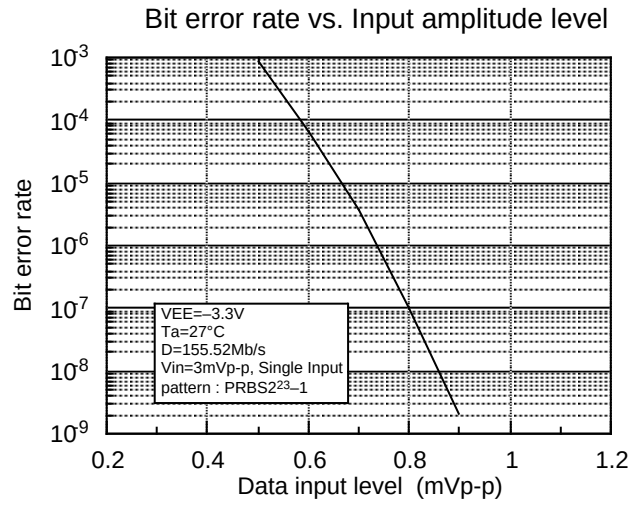


Fig. 10

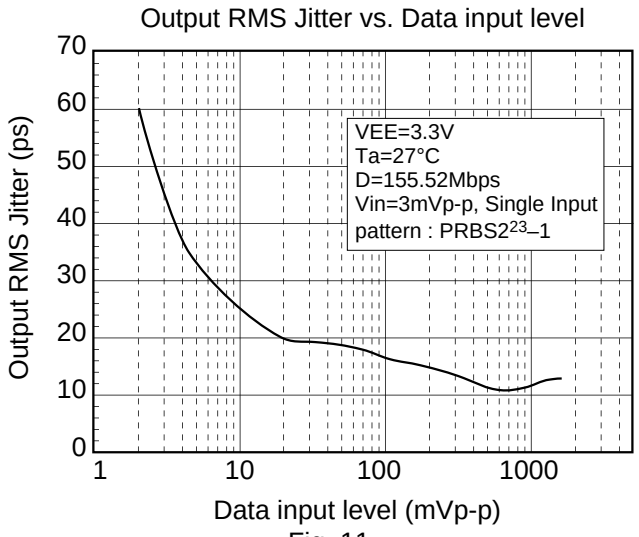
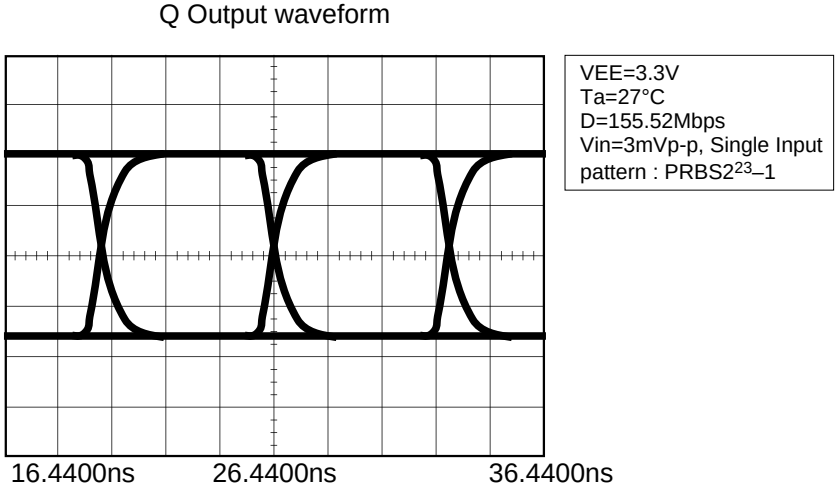


Fig. 11

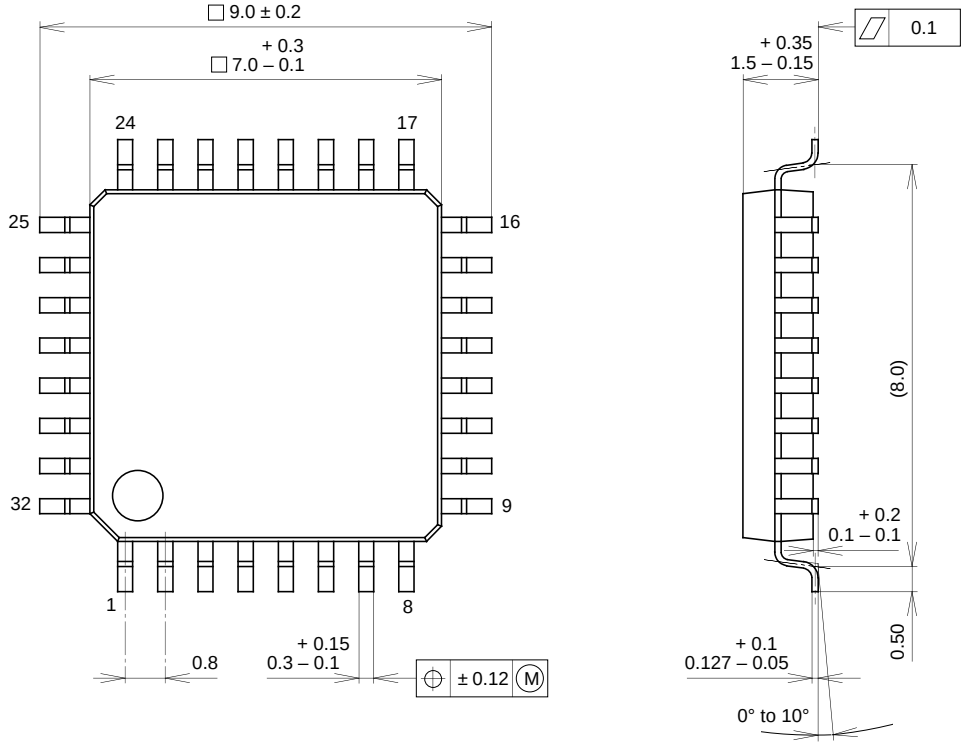


Ch. 1 = 200.0 mVolts/div Offset = 680.0 mVolts
Timebase = 2.00 ns/div Delay = 26.4400 ns

Fig. 12

Package Outline Unit : mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	∗QFP032-P-0707-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g