SONY

CXD1272Q/R

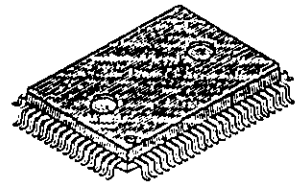
Cellular Phone Filter LSI with On-Chip Compandor

Description

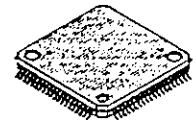
The CXD1272Q/R is a filter LSI for cellular phones. Successor to the CXD1271Q/R, this device features an on-chip compandor a new function fulfilling users' for a more versatile version of the CXD1271Q/R. Furthermore, addition of an attenuator for digital control provides for easy adjustment.

When used in conjunction with the control signal processor CXD1270Q/R IC, a modem can be implemented.

CXD1272Q
80 pin QFP (Plastic)



CXD1272R
80 pin VQFP (Plastic)



Features

- On-chip compandor
- Ultra-low current consumption:
  Operating current – 6mA; Power standby – 1mA
  (For standard 5V operation.)
- Power saver function provided.
- 4-bit attenuation controller facilitates gain adjustment over required range.
- Supports 4 standards
  AMPS, DOC, TACS, and N-TACS.
- Adoption of SCF technology provides stable characteristics
- On-chip 8-level, 3dB step electronic volume.

Functions

- Compandor
- Filtering of received data
- PLL lock detector for received SAT
- Filtering and addition performed on transmitted data
- Audio signal filtering for received/transmitted signals
- Gain controlled through serial data input
- Volume controller (Dual system)

Absolute Maximum Ratings

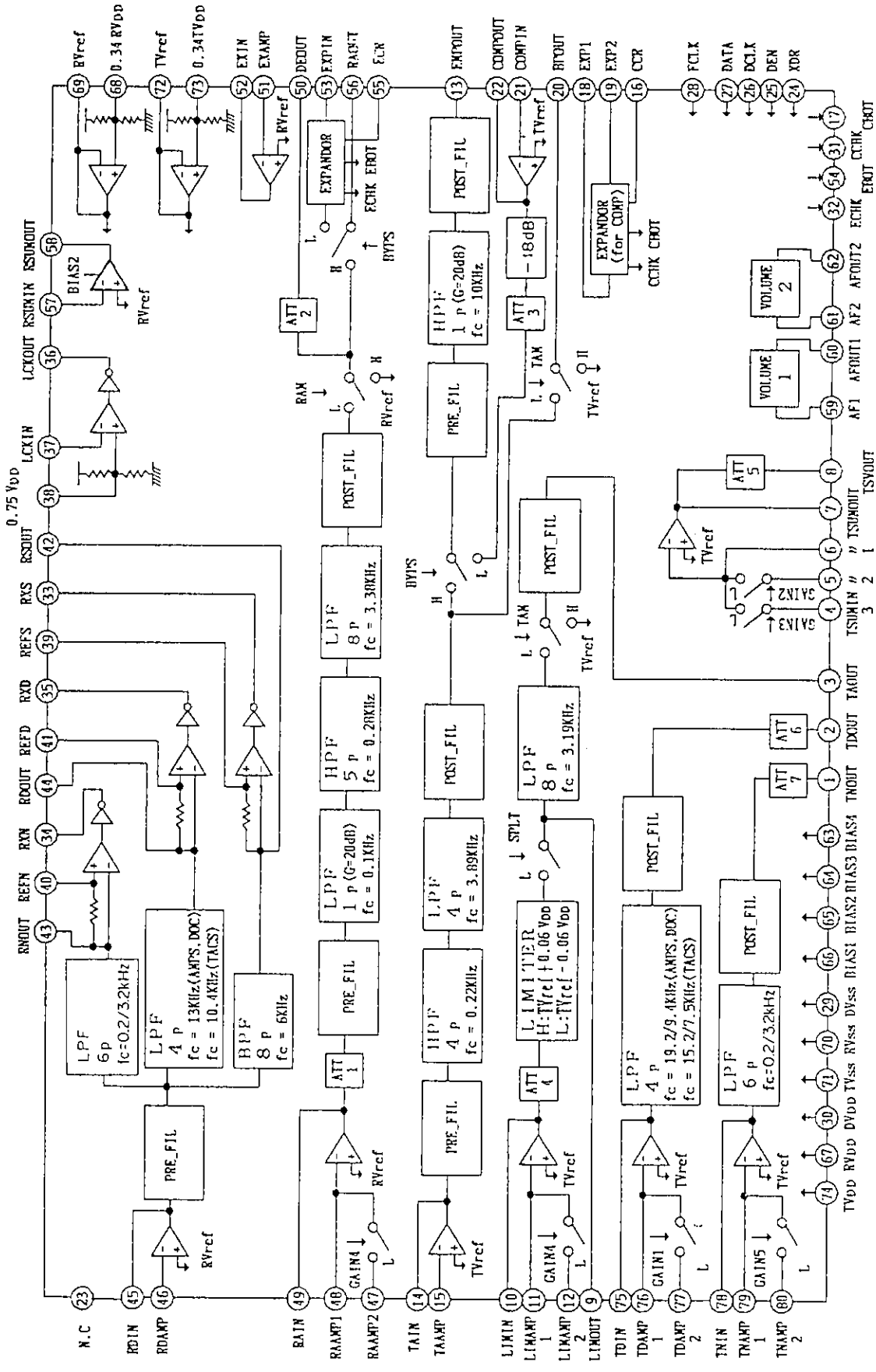
• Supply voltage	V_{DD}	–0.3 to 7.0	V
• Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
• Output voltage	V_{OUT}	–0.3 to V_{DD}+0.3	V
• Operating temperature	Topr	–34 to +85	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75 to 5.25	V
		3.8 to 4.2	V
• Operating temperature	Topr	–34 to +85	°C

E91Z32B35 – ST

Block Diagram



Pin Description

Pin No.		Symbol	I/O	Description
QFP	VQFP			
3	1	TNOUT	O	Filter output for TX (N-TACS standard).
4	2	TDOUT	O	Filter output for TX Wide Band, ST, and SAT.
5	3	TAOUT	O	TX Audio splutter filter output.
6	4	TSUMIN3	I	TX summing amplifier input. Gain is controlled by gain control "GAIN3"
7	5	TSUMIN2	I	TX summing amplifier input. Gain is controlled by gain control "GAIN2"
8	6	TSUMIN1	I	TX summing amplifier input. Used by TSUMIN2 and TSUMIN3 as well as for output data (TDOUT and TNOUT), and audio addition (TAOUT).
9	7	TSUMOUT	O	TX system summing amplifier output.
10	8	TSVOUT	O	Attenuated output for TX system summing amplifier. Controlled by control data "A5C3 to A5C0".
11	9	LIMOUT	I/O	TX audio limiter output. Also used as input for independent measurement of TX splutter filter characteristics of the latter stage.
12	10	LIMIN	O	Gain controller output used for input to limiter.
13	11	LIMAMP1	I	Limiter input 1.
14	12	LIMAMP2	I	Limiter input 2. Gain is controlled by gain control "GAIN4".
15	13	EMPOUT	O	Emphasis output for TX audio.
16	14	TAIN	O	Gain control amplifier output for TX audio input.
17	15	TAAMP	I	Gain control amplifier input from TX audio input.
18	16	CCR	O	Attack recovery time setting of compressor. Satisfy each standard by connecting a 1 µF capacitor between this pin and TVss.
19	17	CBOT	O	Reference voltage output from compressor. (Test pin)
20	18	EXP1	I	Expander input of the compressor structure.
21	19	EXP2	O	Expander output of the compressor structure.
22	20	BPOUT	I	TX audio band-pass filter output.
23	21	COMPIN	I	Gain control amplifier input of compressor input.
24	22	COMPOUT	O	Output from internal compressor.
25	23	—	—	—
26	24	XDR	I	Control data reset. Active at Low.
27	25	DEN	I	Load signal input for inputting serial data to data buffer. Retrieved at the falling edge.
28	26	DCLK	I	Clock signal input for serial data input.
29	27	DATA	I	8-bit serial data input.
30	28	FCLK	I	Clock input for filter. 4.8MHz required.
31	29	DVss	—	Exclusive GND for digital circuits.
32	30	DV_{DD}	—	Exclusive power supply for digital circuits.

Pin No.		Symbol	I/O	Description
QFP	VQFP			
33	31	CCHK	O	Monitor for compressor offset adjustment. (Test pin)
34	32	ECHK	O	Monitor for expander offset adjustment. (Test pin)
35	33	RXS	O	Comparator output for RX SAT.
36	34	RXN	O	Comparator output for RX data (N-TACS standard)
37	35	RXD	O	Comparator output for RX Wide Band Data
38	36	LCKOUT	O	Output for PLL lock detection-use comparator of RX SAT.
39	37	LCKIN	I	Input for PLL lock detection-use comparator of RX SAT.
40	38	0.75V_{DD}	I	Reference voltage input for PLL lock detection-use comparator of RX SAT. Bias at 0.75 times supply voltage. For normal operation, a 1 µF capacitor is externally connected between this pin and RVss.
41	39	REFS	I	Comparator reference voltage input for RX SAT. The offset bias effected by bandpass filter of the former stage can be eliminated by connecting a 0.1 µF capacitor between this pin and RVss
42	40	REFN	I	Comparator reference voltage input for RX data (N-TACS standard). The offset bias effected by low-pass filter of the former stage can be eliminated by connecting a 1 µF capacitor between this pin and RVss.
43	41	REFD	I	Comparator reference voltage input for RX Wide Band Data. The offset bias effected by low-pass filter of the former stage can be eliminated by connecting a 1 µF capacitor between this pin and RVss.
44	42	RSOUT	O	Filter output for RX SAT.
45	43	RNOUT	O	Filter output for N-TACS RX data (N-TACS standard).
46	44	RDOUT	O	Filter output for RX Wide Band Data. Used as a pre-filter for RX audio data.
47	45	RDIN	O	Gain controller amplifier output for RX Wide Band Data and SAT input.
48	46	RDAMP	I	Gain controller amplifier input for RX Wide Band Data and SAT input.
49	47	RAAMP2	I	Input 2 for RX audio data. Gain is controlled by gain control "Gain4".
50	48	RAAMP1	I	Input 1 for RX audio data.
51	49	RAIN	O	Gain control amplifier for RX audio data input.
52	50	DEOUT	O	RX audio filter output.
53	51	EXAMP	I	Gain control amplifier input for expander input.
54	52	EXIN	O	Gain control amplifier output for expander input.
55	53	EXPIN	I	Expander input. (Test pin)
56	54	EBOT	O	Expander reference voltage output.
57	55	ECR	O	Attack recovery time setting of expander. Satisfy each standard by connecting a 1 µF capacitor between this pin and RVss. pin.
58	56	RAOUT	O	Filter output for RX audio data. (BYPS: High) Internal expander output. (BYPS: Low)
59	57	RSUMIN	I	Summing amplifier input for RX system. This signal used by DTMF and audio adder.
60	58	RSUMOUT	O	Summing amplifier output for RX system.
61	59	AF1	I	Volume 1 input.

Pin No.		Symbol	I/O	Description
QFP	VQFP			
62	60	AFOUT1	O	Volume 1 output. Controlled by control data "V1C2 to V1C0".
63	61	AF2	I	Volume 2 input.
64	62	AFOUT2	O	Volume 2 output. Controlled by control data "V2C2 to V2C0".
65	63	BIAS4	I	Determines internal operational amplifier bias current of the compandor. Connect 39kΩ between this pin and RV_{DD}.
66	64	BIAS3	I	Determines internal operational amplifier bias current of the compandor. Connect 15kΩ between this pin and RV_{DD}.
67	65	BIAS2	I	Determines RX summing amplifier bias current. Normally, connect 100kΩ between this pin and RV_{DD}.
68	66	BIAS1	I	Determines internal operation amplifier bias current. Normally, connect 500kΩ between this pin and RV_{DD}.
69	67	RV_{DD}	——	Exclusive power supply for RX system.
70	68	$0.34RV_{DD}$	I	Reference voltage input for RX processing system operational amplifier. Bias at 0.34 times supply voltage. For normal operation, a 1 µF capacitor is connected between this pin and the RVss pin.
71	69	RVref	O	Reference voltage output for RX processing system operational amplifier. Bias at 0.34 times supply voltage. For normal operation, a 1 µF capacitor is connected between this pin and RVss.
72	70	RVss	——	Exclusive GND for RX system.
73	71	TVss	——	Exclusive GND for TX system.
74	72	TVref	O	Reference voltage output for TX processing system operational amplifier. Bias at 0.34 times supply voltage. For normal operation, a 1 µF capacitor is connected between this pin and TVss.
75	73	$0.34TV_{DD}$	I	Reference voltage input for TX processing system operational amplifier. Bias at 0.34 times supply voltage. For normal operation, a 1 µF capacitor is connected between this pin and RVss.
76	74	TV_{DD}	——	Exclusive power supply for TX system.
77	75	TDIN	O	Summing amplifier output for inputting RX Wide Band Data, ST, and SAT data.
78	76	TDAMP1	I	Input for TX SAT.
79	77	TDAMP2	I	Input for TX Wide Band Data and ST. Gain is controlled by gain control "GAIN1".
80	78	TNIN	O	Gain control amplifier output for inputting TX data (N-TACS standard).
1	79	TNAMP1	I	Input 1 for TX data (N-TACS standard).
2	80	TNAMP2	I	Input 2 for TX data (N-TACS standard).

Electrical Characteristics 1

(V_{DD}=5V ± 5%, Ta=–34 to +85°C)

Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Power supply current 1 (N-TACS specification)	I_{DD1}	RV_{DD} TV_{DD} DV_{DD} Total	STD="L" STN="L" V1ST=V2ST="L" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	6	9	mA
Power supply current 2 (Specification other than N-TACS)	I_{DD2}	RV_{DD} TV_{DD} DV_{DD} Total	STD="L" STN="H" V1ST=V2ST="L" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	5.8	8.6	mA
Power supply current 3 (In standby status, excluding volume)	I_{STB1}	RV_{DD} TV_{DD} DV_{DD} Total	STD="H" STN="H" V1ST=V2ST="L" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	1.1	1.5	mA
Power supply current 4 (All in standby status)	I_{STB2}	RV_{DD} TV_{DD} DV_{DD} Total	STD="H" STN="H" V1ST=V2ST="H" BIAS1 resistance=500kΩ BIAS2 resistance=100kΩ	—	1.0	1.3	mA
Digital input voltage "L"	V_{IL}	FCLK, DATA, DCLK, DEN, XDR	—	—	—	0.3V_{DD}	V
Digital input voltage "H"	V_{IH}	FCLK, DATA, DCLK, DEN, XDR	—	0.7V_{DD}	—	—	V
Digital input current "L"	I_{IL}	FCLK, DATA, DCLK, DEN, XDR	V_{IN}=GND	–10	—	10	µA
Digital input current "H"	I_{IH1}	FCLK, DATA, DCLK, DEN, XDR	V_{IN}=V_{DD}	–10	—	10	µA
Digital output voltage "L"	V_{OL}	RXD, RXN, RXS, LCKOUT, ECHK, CCHK	I_{OL}=0.4mA	—	—	0.8	V
Digital output voltage "H"	V_{OH}	RXD, RXN, RXS, LCKOUT, ECHK, CCHK	I_{OH}=–0.4mA	V_{DD}–1	—	—	V
Analog input voltage range	V_{LA}	RDAMP, RAAMP1, RAAMP2, TAAMP, TNAMP1, TNAMP2 TDAMP1, TDAMP2, RSUMIN, TSUMIN1, TSUMIN2, TSUMIN3 AF1, AF2	BIAS1=500kΩ	—	—	1	Vp-p
Analog input resistance	R_I	AF1, AF2	Input pin –0.34V_{DD}	70	130	190	kΩ
Analog switch ON resistance	Rsw	TDAMP2, TSUMIN2, TSUMIN3, EXPOUT, RAOUT, RAAMP2, LIMAMP2, TNAMP2	Input pin –0.34V_{DD}	—	0.6	1.5	kΩ

Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Analog output load resistance 1	R_{L1}	RSUMOUT	Output pin –0.34V_{DD} BIAS2 resistance=100kΩ	2	—	—	kΩ
Analog output load resistance 2	R_{L2}	EXPIN, RAOUT, COMPIN, TAOUT, TDOUT, AFOUT1, EMPIN, TSUMOUT, TSVOUT, AFOUT2, TNOUT	Output pin –0.34V_{DD} BIAS1 resistance=500kΩ	10	—	—	kΩ
Analog output load resistance 3	R_{L3}	RDIN, TAIN, TDIN, TNIN, RAIN	Output pin –0.34V_{DD} BIAS1 resistance=500kΩ	100	—	—	kΩ
Analog output voltage range 1	V_{OA1}	RSUMOUT	BIAS2 resistance=100kΩ Load resistance=2kΩ	—	—	0.4	Vp-p
Analog output voltage range 2	V_{OA2}	RAOUT, EMPOUT, TSVOUT TSUMOUT, TAOUT, TDOUT, RDOUT, TNOUT, AFOUT1, AFOUT2	BIAS1 resistance=500kΩ Load resistance=10kΩ	—	—	0.4	Vp-p
Limiter voltage "L"	V_{LL}	LIMOUT	SPLT="L"	0.34V_{DD} –0.066 V_{DD}	0.34V_{DD} –0.06 V_{DD}	0.34V_{DD} –0.054 V_{DD}	V
Limiter voltage "H"	V_{LH}	LIMOUT	SPLT="L"	0.34V_{DD} +0.054 V_{DD}	0.34V_{DD} +0.06 V_{DD}	0.34V_{DD} +0.066 V_{DD}	V
Electronic volume step	V_{STEP}	AF1 – AFOUT1 AF2 – AFOUT2	—	2.5	3	3.5	dB
Attenuator step1	A_{STEP1}	—	ATT1 to 4, 6, 7	0.1	0.2	0.3	dB
Attenuator step2	A_{STEP2}	TSVOUT	ATT5	0.3	0.4	0.5	dB
RX DATA filter gain 1 (AMPS)	G_{RD1}	RDAMP – RDOUT	Input: –18dBV 13kHz AT="H"	–5	–3	–1	dB
RX DATA filter gain 2 (TACS)	G_{RD2}	RDAMP – RDOUT	Input: –18dBV 10.4kHz AT="L"	–4	–3	–2	dB
RX DATA filter gain 1 (N-TACS)	G_{RN}	RDAMP – RNOUT	Input: –18dBV 0.2kHz NTF="L"	–4	–3	–2	dB
RX DATA filter gain 2 (N-TACS)	G_{RN2}	RDAMP – RNOUT	Input: –18dBV 3.2kHz NTF="H"	–4	–3	–1	dB
RX SAT filter gain	G_{SAT}	RDAMP – RSOUT	Input: –18dBV 6kHz	–1	0	1	dB
TX DATA filter gain 1 (AMPS)	G_{TD1}	TDAMP1 – TDOUT	Input: –18dBV 19.2kHz AT="H", DS="H"	–5	–3	–1	dB
TX DATA filter gain 2 (AMPS)	G_{TD2}	TDAMP1 – TDOUT	Input: –18dBV 9.4kHz AT="H", DS="L"	–4	–3	–2	dB
TX DATA filter gain 3 (TACS)	G_{TD3}	TDAMP1 – TDOUT	Input: –18dBV 15.2kHz AT="L", DS="H"	–5	–3	–1	dB
TX DATA filter gain 4 (TACS)	G_{TD4}	TDAMP1 – TDOUT	Input: –18dBV 7.5kHz NTF="L"	–4	–3	–2	dB
TX DATA filter gain 1 (N-TACS)	G_{TN}	TNAMP – TNOUT	Input: –18dBV 0.2kHz	–4	–3	–2	dB
TX DATA filter gain 2 (NTCS)	G_{TN2}	TNAMP – TNOUT	Input: –18dBV 3.2kHz NTF="H"	–4	–3	–1	dB

Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
RX audio filter gain	G_{RA}	RAAMP1 – RAOUT	Input: –16dBV 1kHz RAM="L", BYPS="H" ATT1=0dB	–1	–0.3	1	dB
RX audio muting volume	G_{RAM}	RAAMP1 – RAOUT	Input: –16dBV 1kHz RAM="H", BYPS="H" ATT1=0dB	50	——	——	dB
RX audio S/N ratio	SN_R	RAAMP1 – RAOUT	Input: –16dBV 1kHz RAM="L", BYPS="H" ATT1=0dB Band: 50Hz to 30kHz	50	——	——	dB
RX audio distortion factor	THD_R	RAAMP1 – RAOUT	Input: –16dBV 1kHz RAM="L", BYPS="H" ATT1=0dB Band: 50Hz to 30kHz	——	——	–50	dB
TX audio gain	G_{TA}	TAAMP – TAOUT	Input: –16dBV 1kHz TAM="L", BYPS="H" SPLT="L" ATT4=0dB	–1	–0.3	1	dB
TX audio muting volume	G_{TAM}	TAAMP – TAOUT	Input: –16dBV 1kHz TAM="H", BYPS="H" SPLT="L" ATT4=0dB	50	——	——	dB
TX audio S/N ratio	SN_T	TAAMP – TAOUT	Input: –16dBV 1kHz TAM="L", BYPS="H" SPLT="L" ATT4=0dB Band: 50Hz to 30kHz	45	——	——	dB
TX audio distortion factor	THD_T	TAAMP – TAOUT	Input: –16dBV 1kHz TAM="L", BYPS="H" SPLT="L" ATT4=0dB Band: 50Hz to 30kHz	——	——	–45	dB

Electrical Characteristics 2

(V_{DD}=4V ± 5%, Ta=–34 to +85°C)

Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Power supply current 1 (N-TACS specification)	I_{DD1}	RV_{DD} TV_{DD} Total DV_{DD}	STD="L" STN="L" V1ST=V2ST="L" BIAS1 resistance=300kΩ BIAS2 resistance=51kΩ	——	5.2	8.2	mA
Power supply current 2 (Specification other than N-TACS)	I_{DD2}	RV_{DD} TV_{DD} Total DV_{DD}	STD="L" STN="H" V1ST=V2ST="L" BIAS1 resistance=300kΩ BIAS2 resistance=51kΩ	——	5.0	7.8	mA
Power supply current 3 (In standby status, excluding volume)	I_{STB1}	RV_{DD} TV_{DD} Total DV_{DD}	STD="H" STN="H" V1ST=V2ST="L" BIAS1 resistance=300kΩ BIAS2 resistance=51kΩ	——	0.9	1.3	mA

Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Power supply current 4 (All in standby status)	I_{STB2}	RV_{DD} TV_{DD} Total DV_{DD}	STD="H" STN="H" V1ST=V2ST="H" BIAS1 resistance=300kΩ BIAS2 resistance=51kΩ	—	0.8	1.1	mA
Analog input voltage range	V_{LA}	RDAMP, RAAMP1, RAAMP2, TAAMP, TNAMP1, TNAMP2 TDAMP1, TDAMP2, RSUMIN, TSUMIN1, TSUMIN2, TSUMIN3 AF1, AF2	BIAS1=300kΩ	—	—	1	Vp-p
Analog input resistance	R_I	AF1, AF2	Input pin $-0.34V_{DD}$	70	130	190	kΩ
Analog switch ON resistance	R_{SW}	TDAMP2, TSUMIN2, TSUMIN3, EXPOUT, RAOUT, RAAMP2, LIMAMP2, TNAMP2	Input pin $-0.34V_{DD}$	—	1.4	4.0	kΩ
Analog output load resistance 1	R_{L1}	RSUMOUT	Output pin $-0.34V_{DD}$ BIAS2 resistance=51kΩ	2	—	—	kΩ
Analog output load resistance 2	R_{L2}	EXPIN, RAOUT, COMPIN, TAOUT, TDOUT, AFOUT1, EMPIN, TSUMOUT, TSVOUT, AFOUT2, TNOUT	Output pin $-0.34V_{DD}$ BIAS1 resistance=300kΩ	10	—	—	kΩ
Analog output load resistance 3	R_{L3}	RDIN, TAIN, TDIN, TNIN, RAIN	Output pin $-0.34V_{DD}$ BIAS1 resistance=300kΩ	100	—	—	kΩ
Analog output voltage range 1	V_{OA1}	RSUMOUT	BIAS2 resistance=51kΩ Load resistance=2kΩ	—	—	0.4	Vp-p
Analog output voltage range 2	V_{OA2}	RAOUT, EMPOUT, TSVOUT TSUMOUT, TAOUT, TDOUT, RDOUT, TNOUT, AFOUT1, AFOUT2	BIAS1 resistance=300kΩ Load resistance=10kΩ	—	—	0.4	Vp-p

Note) The characteristics which isn't written in this table is the same as that of 5V operation.

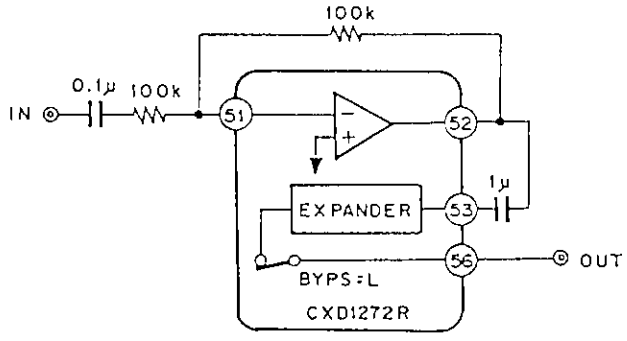
Compander Characteristics

	Item	Symbol	Pin name	Conditions	Min.	Typ.	Max.	Unit
Compressor	Input reference level	Acr	COMPIN–COMPOUT	——	α–0.5	α	α+0.5	dBV
	Output level	Aco	COMPIN–COMPOUT	Input: α–30dBV Input: α–50dBV	α–15.5 α–26	α–15 α–25	α–14.5 α–24	dBV
	Attack time	Tca	COMPIN–COMPOUT	12dB step input	2.4	3.0	3.6	ms
	Recovery time	Tcr	COMPIN–COMPOUT	12dB step input	10.8	13.5	16.2	ms
	Distortion factor + noise	THNc	COMPIN–COMPOUT	Input: α–10dBV (1kHz)	——	–40	–30	dB
	Noise level	Nc	COMPIN–COMPOUT	Input: No signal	——	–40	–35	dBV
Expander	Input reference level	Aer	EXPIN – RAOUT	——	α–1	α	α+1	dBV
	Output level	Aeo	EXPIN – RAOUT	Input: α–15dBV Input: α–30dBV	α–31 α–62	α–30 α–60	α–29 α–58	dBV
	Attack time	Tea	EXPIN – RAOUT	6dB step input	2.4	3.0	3.6	ms
	Recovery time	Ter	EXPIN – RAOUT	6dB step input	10.8	13.5	16.2	ms
	Distortion factor + noise	THNe	EXPIN – RAOUT	Input: α–5dBV (1kHz)	——	–45	–35	dB
	Noise level	Ne	EXPIN – RAOUT	Input: No signal	——	–88	–75	dBV

Note) 1. 0dBV=1Vrms
2. Definition of attack recovery time based on AMPS standard.
3. Distortion factor+noise and noise level measuring range: 50Hz to 30kHz.
4. Output level expressed in value obtained after automatic correction of linearity. (Supply voltage and temperature variations after correction not included.)
5. Measurement circuit shown below.
6. In case 5V power supply is used: α=0, 4V is used: α= −1.94

Compander Measurement Circuit

<Expander>



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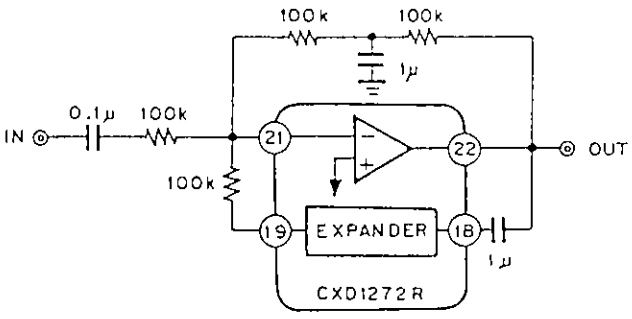


Description of Operation

This IC is a filter IC which is designed for use in cellular car telephones. It conforms to the AMPS (North America), TACS (United Kingdom), DOC (Canada), and N-TACS standards. When this filter IC is combined with the CXD1270Q/R control signal processing LSI chip, a modem is constituted with the following functions:

(1) Received WIDE BAND DATA filtering
(2) Received SAT filtering
(3) Received SAT PLL lock detection
(4) Received N-TACS data filtering
(5) Transmitted WIDE BAND DATA, ST, and SAT summing
(6) Transmitted WIDE BAND DATA, ST, and SAT filtering
(7) Transmitted N-TACS data filtering
(8) Received voice filtering
(9) Transmitted voice filtering
(10) Attenuator and volume control
(11) Serial data input
(12) Compander

These functions are detailed below:

1. Received WIDE BAND DATA filtering

In a cellular car telephone system, data is exchanged in the line connection and hand-off processes between land stations (base stations) and mobile stations (mobile switching offices) for channel setup and other purposes. The data consists of Manchester code which is called WIDE BAND DATA. The specified data transmission rate for the AMPS/DOC standard is 20kbaud, and the TACS standard is 16kbaud. The received WIDE BAND DATA is passed through the gain control amplifier and prefilter and fed to the fourth-order Butterworth low-pass filter which functions as a DATA demodulation rolloff filter. The low-pass filter cutoff frequency varies with the cellular system standard and is controlled according to serial data. In the AMPS or DOC cellular system, a low-pass filter cutoff frequency of 13kHz (typical value) is obtained when AT="High". In the TACS or N-TACS system, a low-pass filter cutoff frequency of 10.4kHz (typical value) is obtained when AT="Low".Bandwidth limiting is provided in this manner so as to minimize the error rate.

After the filter output is wave-shaped to CMOS logic levels by a comparator, it is transmitted to the CXD1270Q/R.

2. Received SAT filtering

While the cellular car telephone line is connected (during mobile telephone conversation), the land and mobile stations exchange a sine wave signal called SAT (supervisory audio tone) to acknowledge one another. Each cellular system standard provides three different SAT frequencies: 5.97kHz, 6.00kHz, and 6.03kHz. In the line connection and hand-off processes, one of these three frequencies is chosen. The land station sends 2-bit data called SCC (SAT color code) to the mobile station to notify which frequency is used. While the line is connected, the mobile and land stations receive the SAT from one another to recognize each other.

As is the case with the WIDE BAND DATA, the SAT transmitted from the land station passes through the gain control amplifier and prefilter and then goes through the 6kHz eighth-order Butterworth bandpass filter which is provided to protect the SAT from the voice components (300Hz to 3kHz) and reduce weak electric field high-frequency noise (6kHz to 13kHz). As a bandpass filter having a center frequency of 6kHz is formed, SAT detection is accomplished with high-efficiency. The 6kHz bandpass filter output is wave-shaped to CMOS logic levels by a comparator and then transmitted to the CXD1270Q/R.

3. Received SAT PLL lock detection

When the SAT having a frequency designated by the SCC is received by the CXD1270Q/R, the DPLL is locked. The CXD1271Q/R incorporates a lock /unlock judgment comparator. The output of this comparator switches from the "Low" to the "High" level when the CXD1270Q/R SAT lock detection output (SDET) exceeds the reference voltage ($0.75V_{DD}$).

4. Received N-TACS data filtering

When the CXD1272Q/R is intended for use in the non-N-TACS standard, it can be used as an audio filter by changing control data NFP to "High" to change over the cutoff frequency to 3.2kHz. To obtain 100Hz data to be used in an N-TACS system, the received N-TACS data is passed through the sixth-order Butterworth low-pass filter having a cutoff frequency of 200Hz. The filter output is wave-shaped to CMOS logic levels by a comparator and then transmitted.

5. Transmitted WIDE BAND DATA, ST, and SAT summing

In a cellular car telephone system, the mobile station sends the WIDE BAND DATA or ST and SAT to the land station.

The ST is a signal transmitted for telephone conversation termination or bell ringing purposes. Its frequency is 10kHz (AMPS/DOC standard) or 8kHz (TACS/N-TACS standard). WIDE BAND DATA, ST, and SAT input from the CXD1270Q/R to the CXD1272Q/R is accomplished via an attenuation pad.

The CXD1271Q/R incorporates an inverting summing amplifier which is used to sum up the WIDE BAND DATA, ST, and SAT signals before transmission. As the transmission filer subsequent to the summing amplifier, the fourth-order Butterworth low-pass filter having a cutoff frequency of 19.2kHz (AMPS/DOC standard) or 15.2kHz (TACS/N-TACS standard) is selected at the time of WIDE BAND DATA transmission, or the fourth-order Butterworth low-pass filter having a cutoff frequency of 9.4kHz (AMPS/DOC standard) or 7.5kHz (TACS/N-TACS standard) is chosen at the time of ST transmission.

To compensate for the amplitude characteristics difference between the 19.2kHz (15.2kHz) and 9.4kHz (7.5kHz) low-pass filters at a ST frequency of 10kHz, two different summing amplifiers gains can be selected. For ST transmission, the gain control data (GAIN1) is set to "Low" to obtain a gain of + (plus) several dB or set to "High" to obtain a gain of – (minus) several dB. An external resistor is to be adjusted to obtain the optimum gain.

6. Transmitted WIDE BAND DATA, ST, and SAT filtering

A low-pass filter is provided subsequently to the summing amplifier to eliminate the high-order harmonic content of the summing amplifier output. The AMPS/DOC prescribes that a 20kHz±10% fourth-order Butterworth low-pass filter be used as the transmitted WIDE BAND DATA rolloff filter. Therefore, the CXD1271Q/R employs a 19.2kHz fourth-order Butterworth low-pass filter to meet the AMPS 60kHz attenuation requirement (38dB min.). Further, the cutoff frequency of this transmission filter needs to be lower than 19.2kHz because the ST and SAT transmission frequencies are 10kHz and 6kHz, respectively. The CXD1271Q/R provides control according to serial data. When AT="High" and DS="High", a cutoff frequency of 19.2kHz (typical value) is obtained. When AT="High" and DS="Low", the obtained cutoff frequency is 9.4kHz (typical value).

As for the TACS/N-TACS system, the transmission speed difference is compensated for by obtaining a cutoff frequency of 15.2kHz (typical value) when AT="Low" and DS="High", or a cutoff frequency of 7.5kHz (typical value) when AT="Low" and DS="Low".

7. Transmitted N-TACS data filtering

For the N-TACS system, the sixth-order Butterworth low-pass filter having a cutoff frequency of 200Hz is employed as the transmitted data rolloff filter as is the case with the received N-TACS data. Similarly, the filter may be used as an audio filter by changing its cutoff frequency to 3.2kHz.

8. Received voice filtering

Three Butterworth filters are employed to meet each cellular standard.

The input stage is equipped with a gain control amplifier and a loopback distortion elimination prefilter. The output stage is provided with a carrier elimination postfilter.

The RDOUT output is fed into the gain control amplifier, passed through the prefilter, deemphasized by the first-order Butterworth low-pass filter, bandlimited by the fifth-order Butterworth high-pass and low-pass filter, and transferred out via the postfilter.

RAM provides muting control. Expander bypass control is exercised according to the BYPS control data.

9. Transmitted voice filtering

In the transmitter system, the voice is passed through the gain control amplifier and prefilter, bandlimited by the fourth-order Butterworth high-pass filter and low-pass filter, passed through the postfilter prefilter, emphasized by the first-order Butterworth high-pass filter, and transferred out via the postfilter.

Further, the output is entered into the limiter via the gain control amplifier, clipped at 1.7±0.3V (V_{DD}=5V typ.), passed through the eighth-order Butterworth low-pass filter which serves as an abrupt splatter filter, and transferred out via the postfilter.

TAM exercises muting control, and the BYPS control data provides bypass control of compressor.

SPLT is normally at "Low". However, when it is placed at "High", the splatter filter characteristics can be observed without being affected by the limiter.

10. Attenuator and volume control

4-bit control attenuators (ATT1 to ATT7) are provided at places where the voice signal level needs to be fine tuned. Therefore, final level adjustments can be made according to serial data.

Further, two 3-bit control electrical volume controls are incorporated to adjust the loudness of the speaker and exercise linking and other volume control.

* ATT1 to 7

C3	C2	C1	C0	GAIN	
				ATT5	Other
1	1	1	1	–2.8	–1.4
1	1	1	0	–2.4	–1.2
1	1	0	1	–2.0	–1.0
1	1	0	0	–1.6	–0.8
1	0	1	1	–1.2	–0.6
1	0	1	0	–0.8	–0.4
1	0	0	1	–0.4	–0.2
1	0	0	0	0	0
0	1	1	1	0.4	0.2
0	1	1	0	0.8	0.4
0	1	0	1	1.2	0.6
0	1	0	0	1.6	0.8
0	0	1	1	2.0	1.0
0	0	1	0	2.4	1.2
0	0	0	1	2.8	1.4
0	0	0	0	3.2	1.6

dB

* VOLUME1, 2

C2	C1	C0	GAIN
1	1	1	–21
1	1	0	–18
1	0	1	–15
1	0	0	–12
0	1	1	–9
0	1	0	–6
0	0	1	–3
0	0	0	0

dB

11. Serial data input

The CXD1271Q/R IC receives internal control data input in the form of 8-bit serial data. The four high-order bits are used for address indication, whereas the remaining four low-order bits are handled as data.

In the input process, 8-bit serial data is entered into the internal shift register when the DCLK clock pulse rises, and put into the internal buffer designated by the address upon receipt of the DEN load signal.

When the XDR reset signal is received, the internal buffer is initialized.

Serial data structure descriptions, timing chart, and switching characteristics descriptions are presented below.

Serial Data Format (8-bit serial)

7	6	5	4	3	2	1	0

7	6	5	4	3	2	1	0	
0	0	0	0	AT $_0$	DS $_1$	STN $_1$	STD $_1$	
0	0	0	1	RAM $_1$	TAM $_1$	BYPS $_0$	SPLT $_0$	
0	0	1	0	GAIN1 $_0$	GAIN2 $_0$	GAIN3 $_0$	CAL $_1$	
0	0	1	1	EA5 $_1$	EA4 $_0$	EA3 $_0$	EA2 $_0$	
0	1	0	0	EA1 $_0$	EA0 $_0$	CA1 $_0$	CA0 $_0$	
0	1	0	1	CA5 $_1$	CA4 $_0$	CA3 $_0$	CA2 $_0$	
0	1	1	0	V1C2 $_1$	V1C1 $_1$	V1C0 $_1$	V1ST $_1$	VOLUME1
0	1	1	1	V2C2 $_1$	V2C1 $_1$	V2C0 $_1$	V2ST $_1$	VOLUME2
1	0	0	0	A1C3 $_1$	A1C2 $_0$	A1C1 $_0$	A1C0 $_0$	ATT1
1	0	0	1	A2C3 $_1$	A2C2 $_0$	A2C1 $_0$	A2C0 $_0$	ATT2
1	0	1	0	A3C3 $_1$	A3C2 $_0$	A3C1 $_0$	A3C0 $_0$	ATT3
1	0	1	1	A4C3 $_1$	A4C2 $_0$	A4C1 $_0$	A4C0 $_0$	ATT4
1	1	0	0	A5C3 $_1$	A5C2 $_0$	A5C1 $_0$	A5C0 $_0$	ATT5
1	1	0	1	A6C3 $_1$	A6C2 $_0$	A6C1 $_0$	A6C0 $_0$	ATT6
1	1	1	0	A7C3 $_1$	A7C2 $_0$	A7C1 $_0$	A7C0 $_0$	ATT7
1	1	1	1		NTF $_0$	GAIN4 $_0$	GAIN5 $_0$	

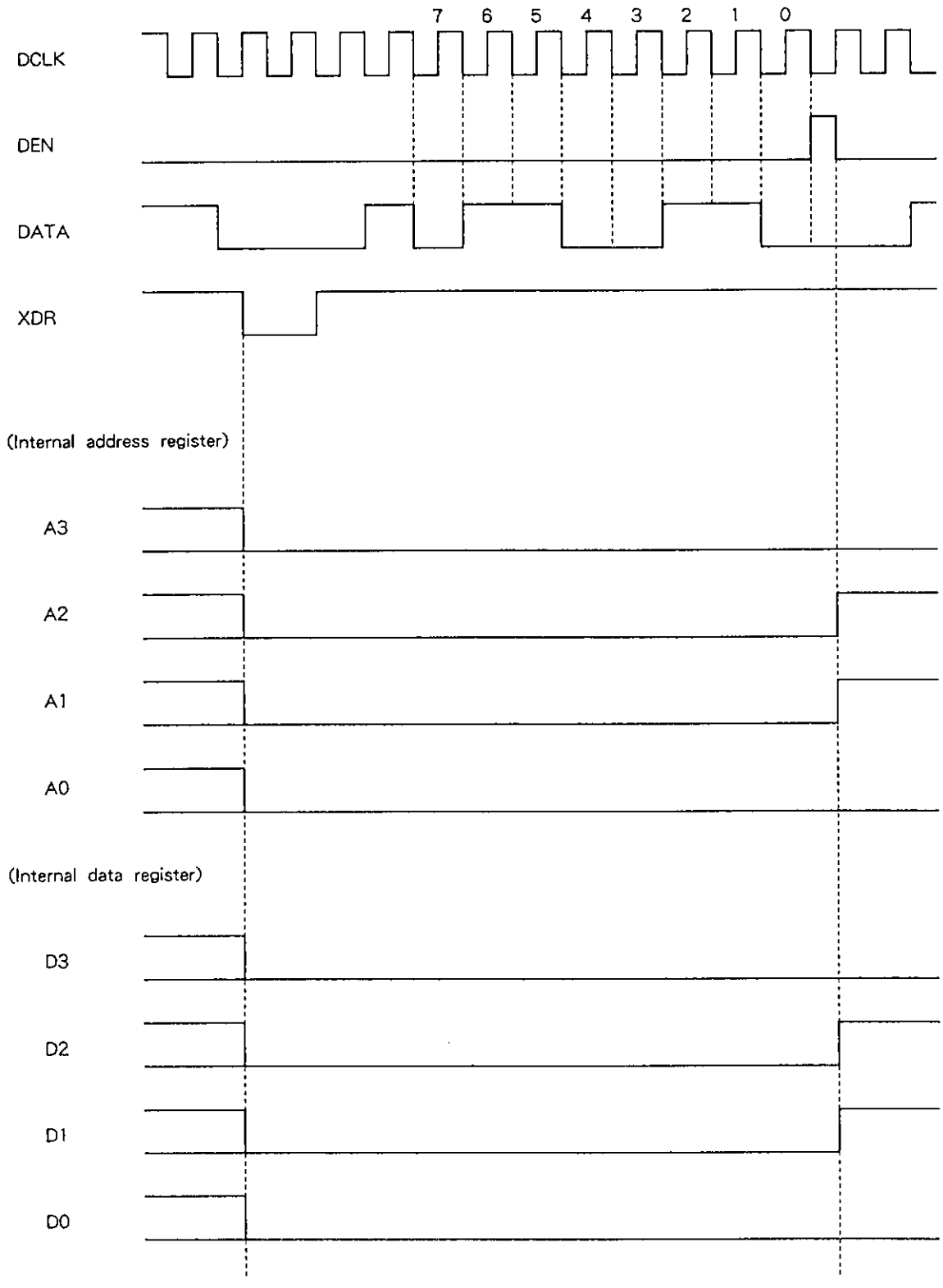
Address Data

Note) The state ("0" or "1") prevailing upon data reset (XDR="Low") is indicated at the lower right-hand corner of above table columns.

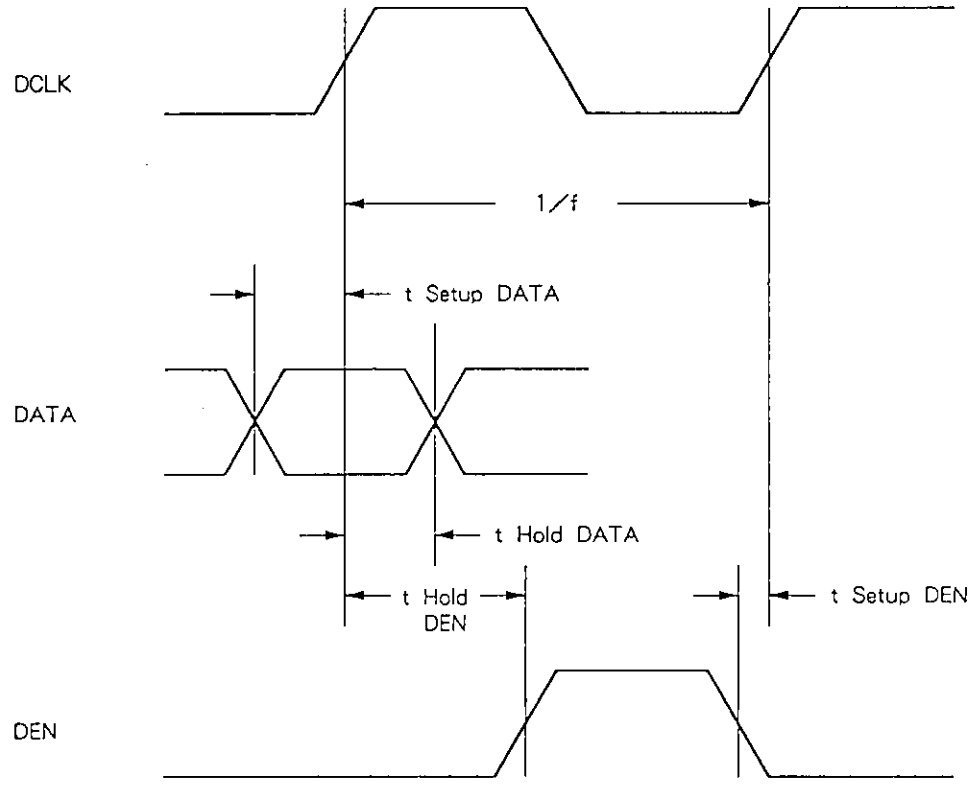
Control Data Description

Data name	Description
AT	AMPS/DOC system is used at "High"; TACS/N-TACS system is used at "Low".
DS	WBD transmitted at "High"; ST/SAT transmitted at "Low".
STN	N-TACS data processing block in standby mode at "High".
STD	Power save mode at "High". (However, the data reception block operates at all times.)
RAM	Received voice is muted at "High".
TAM	Transmitted voice is muted at "High".
BYPS	Compander is bypassed at "High".
SPLT	Input through LIMOUT at "High" to evaluate the splatter filter characteristics.
GAIN1	Gain control of transmitted data summing input. TDAMP2 input switch is left open at "High".
GAIN2	Gain control of transmitted data summing amplifier. TSUMIN2 input switch is left open at "High".
GAIN3	Gain control of transmitted data summing amplifier. TSUMIN3 input switch is left open at "High".
CAL	Automatic correction mode of comander linearity at "High". Not used when CAL="Low".
EA5 to EA0	Linearity adjustment of expander. Valid only when (MSB: EA5) CAL="Low".
CA5 to CA0	Linearity adjustment of compressor. Valid only when (MSB: CA5) CAL="Low".
V1C2 to V1C0	VOLUME1 gain control (3-bit control; MSB: V1C2).
V1ST	VOLUME1 in standby mode at "High".
V2C2 to V2C0	VOLUME2 gain control (3-bit control; MSB: V2C2).
V2ST	VOLUME2 in standby mode at "High".
A1C3 to A1C0	ATT1 gain control (4-bit control; MSB: A1C3).
A2C3 to A2C0	ATT2 gain control (4-bit control; MSB: A2C3).
A3C3 to A3C0	ATT3 gain control (4-bit control; MSB: A3C3).
A4C3 to A4C0	ATT4 gain control (4-bit control; MSB: A4C3).
A5C3 to A5C0	ATT5 gain control (4-bit control; MSB: A5C3).
A6C3 to A6C0	ATT6 gain control (4-bit control; MSB: A6C3).
A7C3 to A7C0	ATT7 gain control (4-bit control; MSB: A7C3).
NTF	Switchover of the filter fc for transmitted and received N-TACS. ("Low" for 0.2k, "High" for 3.2k)
GAIN4	Gain control of limitter input amplifier. LIMAMP2 input switch is left open at "High".
GAIN5	Gain control of transmitted N-TACS input. TNAMP2 input switch is left open at "High".

Serial Data Timing Chart



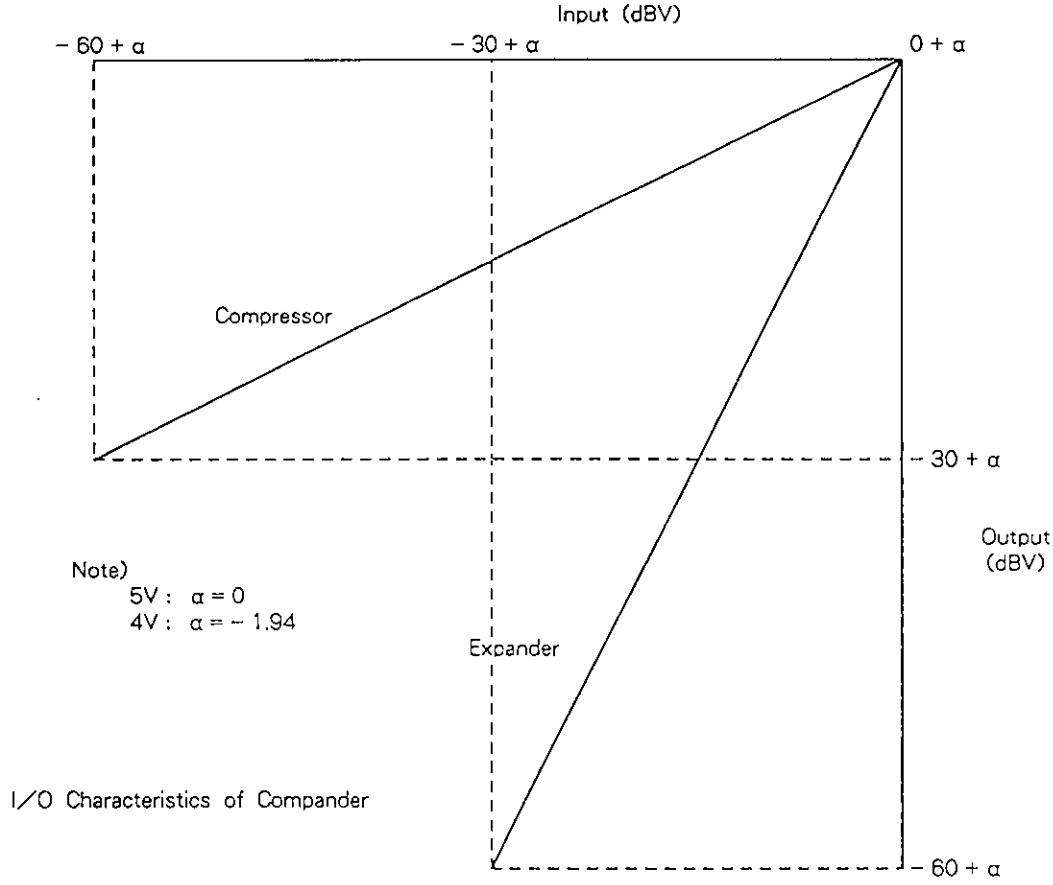
Serial Data Switching Characteristics



Item	Symbol	Min.	Typ.	Max.	Unit
DATA setup time	t Setup DATA	500	—	—	ns
DATA hold time	t Hold DATA	500	—	—	ns
DEN setup time	t Setup DEN	100	—	—	ns
DEN hold time	t Hold DEN	500	—	—	ns
DCLK frequency	f	—	—	1.2	MHz

Compander

A feature of the expander is that, as shown in the graph below, the expander has 0dBV cross point (reference level) which is also its maximum input level, and acts only in the direction that the signal is attenuated. A compressor is configured by applying negative feedback to the expander through an operational amplifier. Therefore, the compressor, like the expander, has 0dBV reference level and its maximum input level.
(In case 5V power supply is used)



I/O Characteristics of Compander

a) Setting of reference level (Refer to the next page.)

When a system is to be configured, the reference level must be brought to almost the middle of the compander input range. For this purpose, gain control amplifiers are provided.
In the expander, the apparent signal level can be lowered by amplifying the signal (AdB) before it is supplied to the expander so that the reference level can be set at a point - 2 times the gain (- 2dBV).
In the compressor, 18dB attenuation is accomplished after the compressor. Therefore, the reference point is set at a point - 36dBV, which is twice the value, but it can be freely set by changing the gain (AdB) of the compressor input stage.

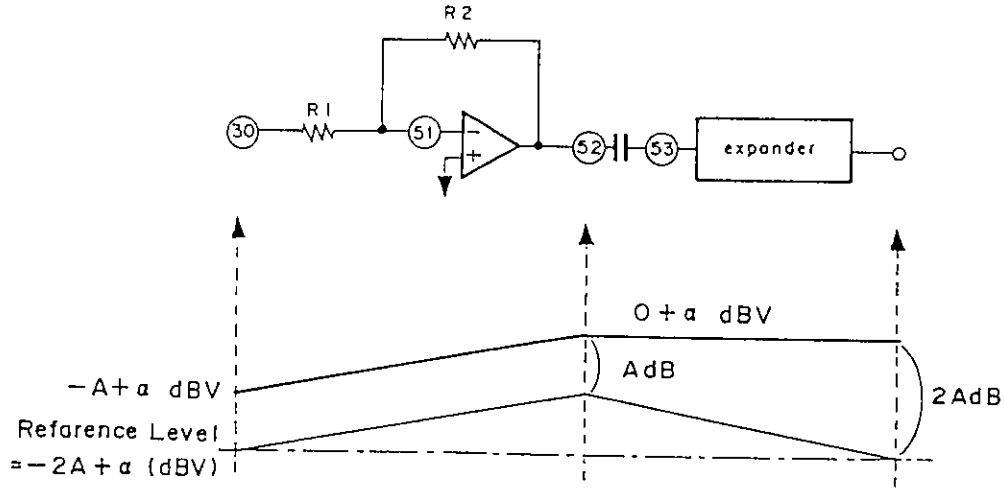
b) Automatic correction of linearity

To maintain good linearity, the compander executes automatic correction of linearity when it switches from the standby state to the active state (STD switches from "High" to "Low"). More precisely, the compander starts automatic correction when recognition of control data CAL being "High" causes STD to fall from "High" to "Low". Note that forced muting is done at the time. Forced muting is canceled when correction is completed. The time required for correction is 31 ms maximum.
When CAL is "Low", no automatic correction will be executed, but control data for linearity correction will be valid. Although correction can be made by the control data, considerable difficulties will be encountered. For this reason, when CAL="Low", use of the compander is inhibited.

Setting of Reference Level

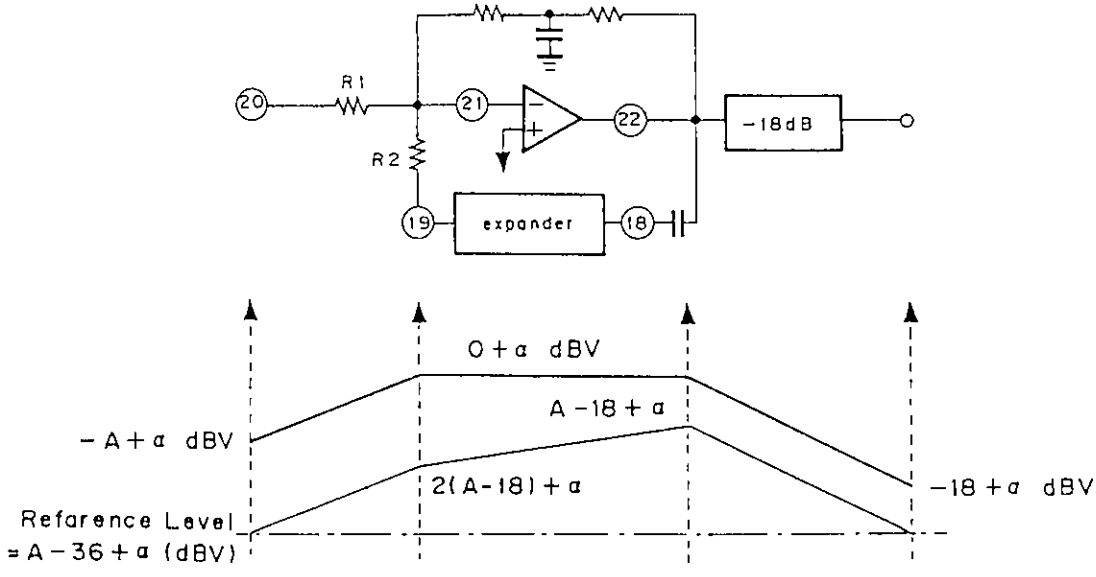
<Expander>

AdB = 20log (R2/R1)



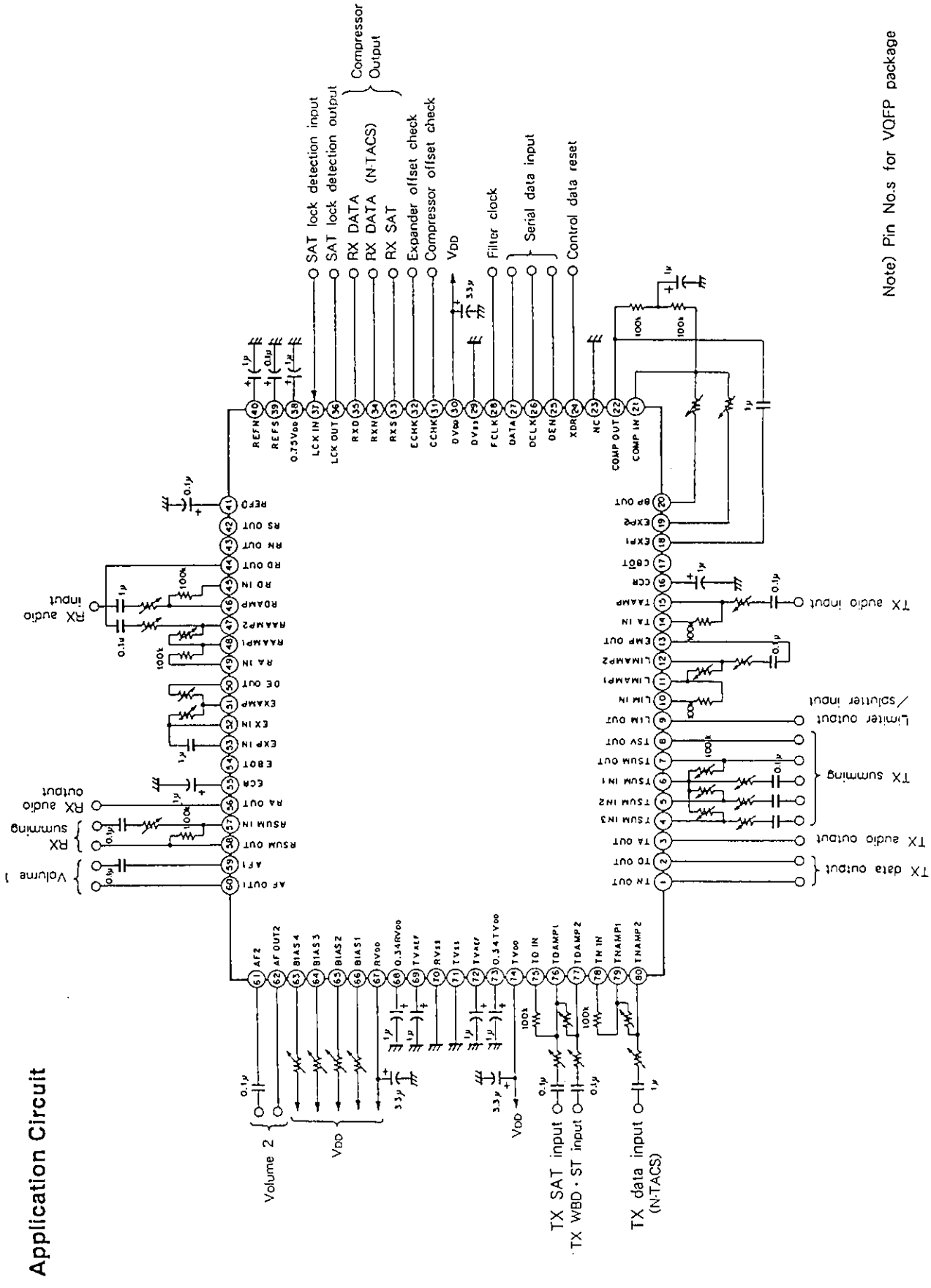
<Compressor>

AdB = 20log (R2/R1)



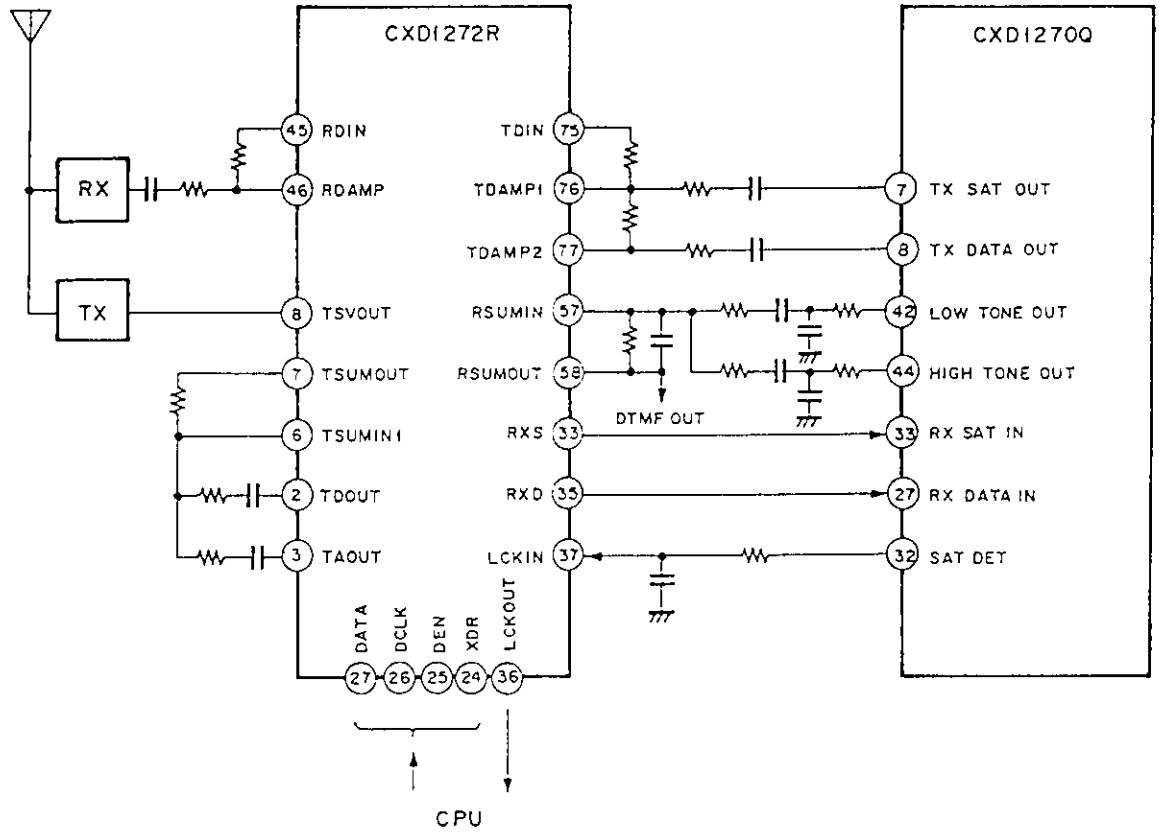
Note) 5V: α =0
4V: α = −1.94

Application Circuit



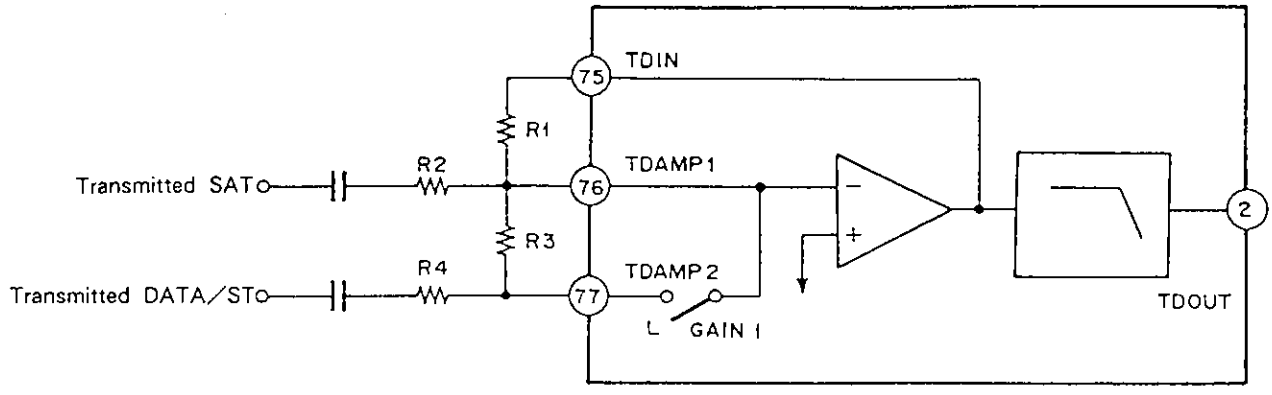
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Connection Example of CXD1272R and CXD1270Q



Notes on Operation

1. Transmitted Data Summing Amplifier Gain Adjustment



Note) The indicated pin numbers are for the VQFP package.

Resistors R2 and R1 in the above circuit adjust the transmitted SAT attenuation, whereas resistors R4, R3, and R1 adjust the transmitted DATA/ST attenuation. The recommended amount of attenuation is –20dB. Further, the transmitted output level difference between the DATA and ST is compensated for by the Resistor R3.

For ST transmission, the GAIN1 data is set to "Low" to raise the gain. For DATA transmission, the GAIN1 data is set to "High" to lower the gain.

2. Cellular System Setup and Transmitted Data Changeover

The data filter cutoff frequency is controlled to match the employed cellular system and transmitted data. For this control, the AT and DS control data are used.

Transmitted data / Cellular system	WBD	ST, SAT
AMPS, DOC	AT=H DS=H	AT=H DS=L
TACS, N-TACS	AT=L DS=H	AT=L DS=L

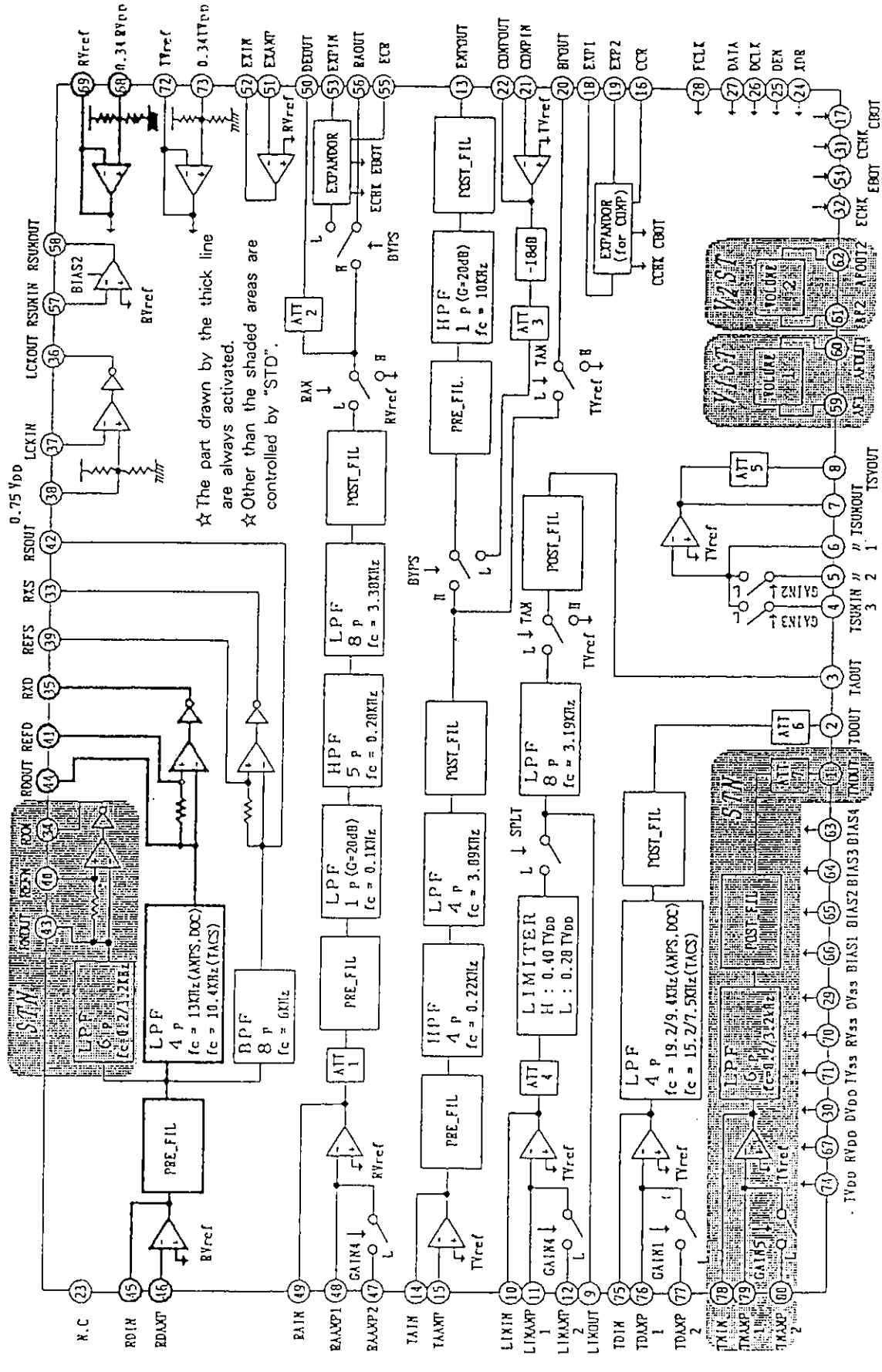
3. Standby Control

Standby control is exercised independently by the "STD", "STN", "V1ST", "V2ST" control data.

Control data	Control block	"H"	"L"
STD	Blocks other than VOLUME1, VOLUME2, and N-TACS data processing blocks	Only blocks up to RDAMP-RXD, and the RVref generator circuit are active	Active
STN	N-TACS data processing block (fc=0.2kHz, sixth-order LPF)	Standby	Active
V1ST	VOLUME1	Standby	Active
V2ST	VOLUME2	Standby	Active

Note) The condition in which STD="High" and STN="Low" is strictly prohibited.

Standby Control Diagram (CXD1272R)



4. Output Voltage Range and Supply Current Adjustment

The CXD1271Q/R varies its output level range and supply current depending on the BIAS resistor (resistor connected between the BIAS1 and RV_{DD} pins).

The data presented under Electrical Characteristics are obtained at a BIAS resistance of 500kΩ with 10kΩ output load.

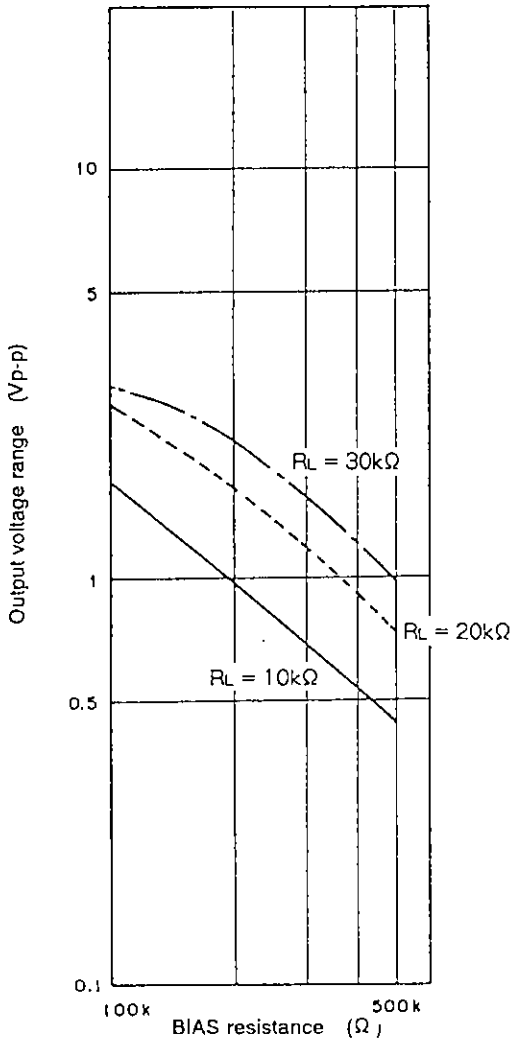
As the BIAS resistance determines the internal operational amplifier bias current, decreasing the BIAS resistance enlarges the output level range and supply current, and increasing the BIAS resistance reduces the output level range and supply current.

Therefore, the output voltage range and supply current can be adjusted as desired by varying the BIAS resistance.

For reference, the relation between the BIAS resistance and output level range/supply current is indicated below (V_{DD}=5V, Ta=25°C).

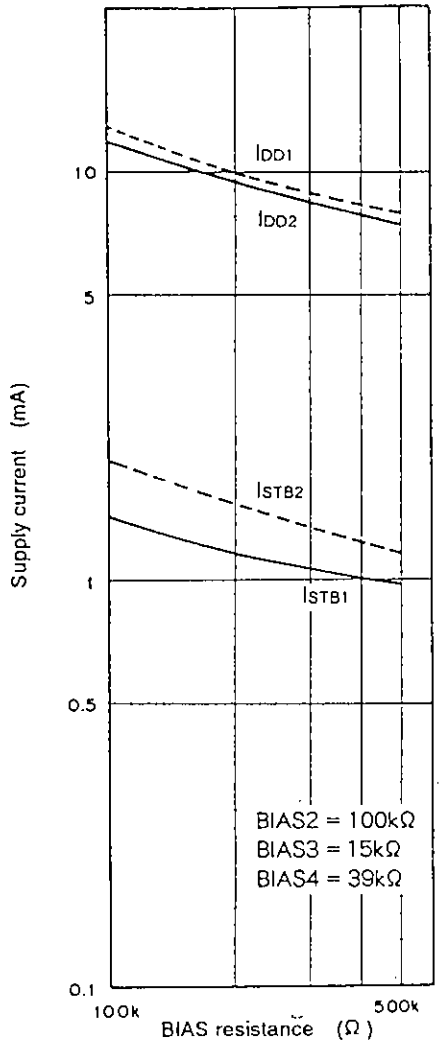
(BIAS1)

BIAS resistance vs. Output voltage range



(BIAS1)

BIAS resistance vs. Supply current



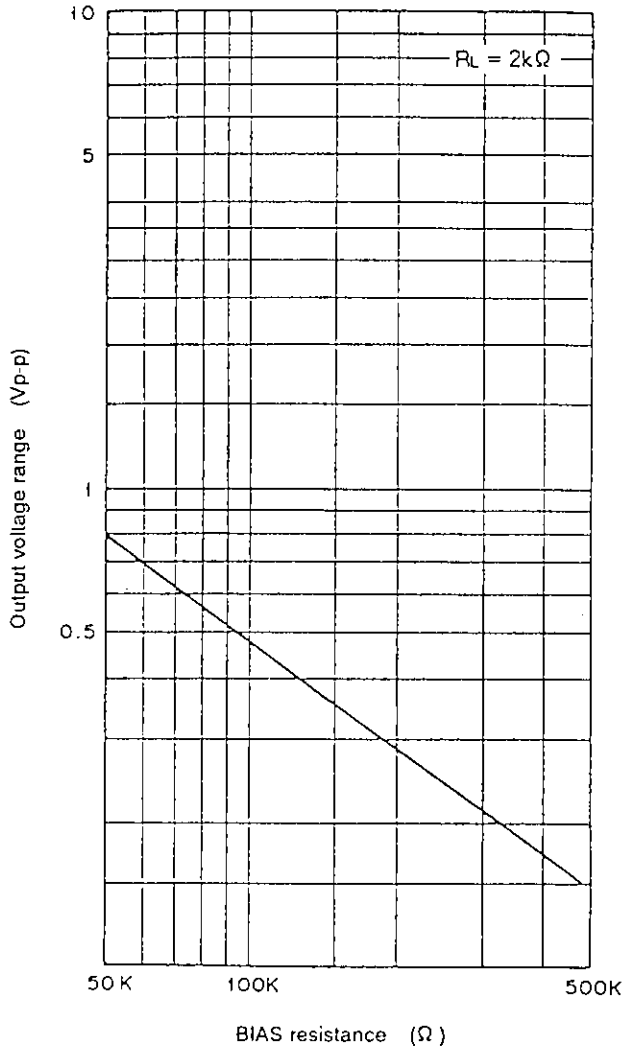
5. High-load Operational Amplifier Output Voltage Range Adjustment

As stated in the preceding section, the output voltage range can be adjusted by varying the BIAS resistance. However, the output voltage range of the receiver system summing amplifier (RSUMIN-RSUMOUT) can be independently varied by adjusting the other BIAS resistance (connected between the BIAS2 and RV_{DD} pins). This feature is convenient in driving a heavy load without significantly affecting the supply current.

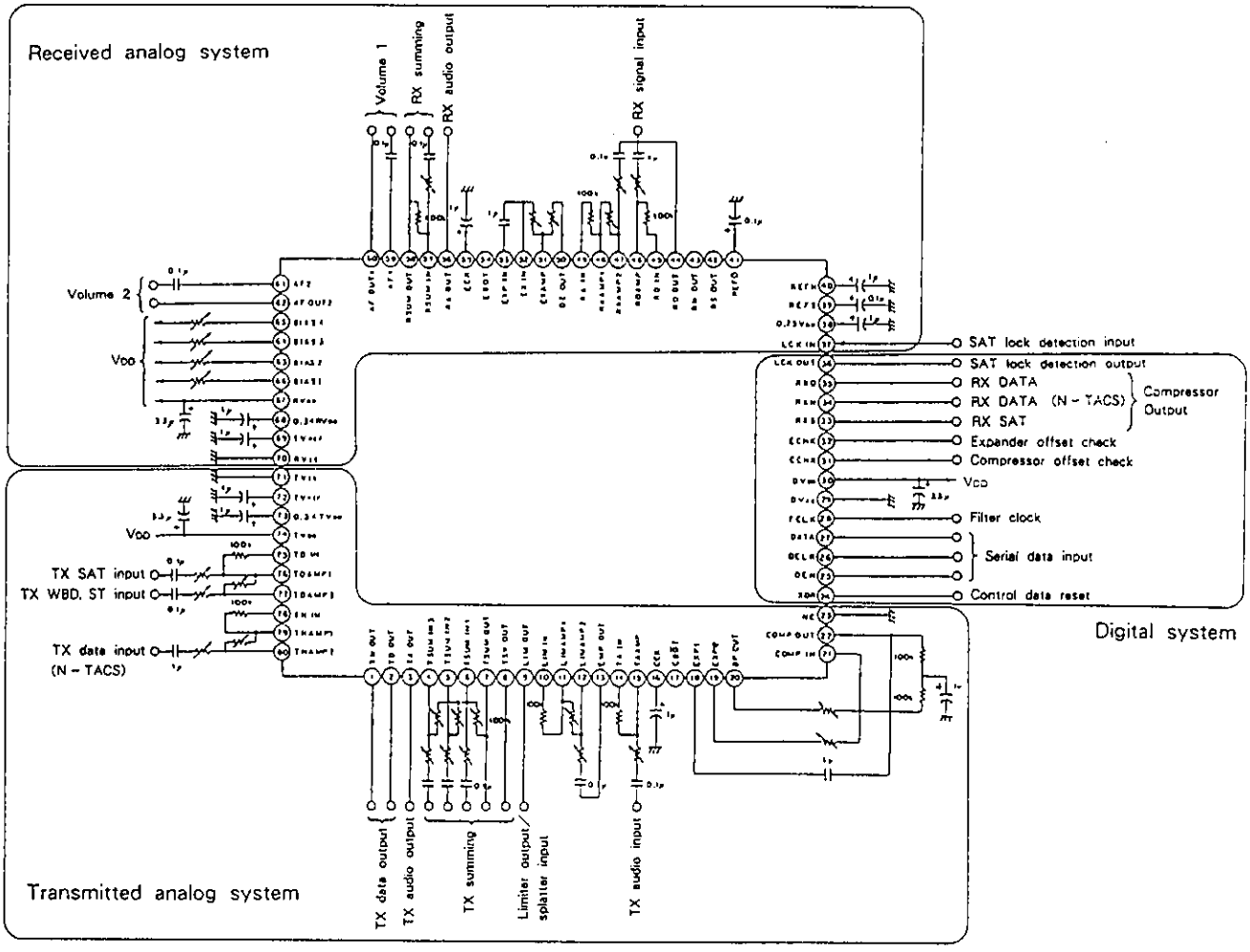
For reference, the relationship between the BIAS resistance and output voltage range is indicated below (V_{DD}=5V, load resistance=2kΩ).

(BIAS2)

BIAS resistance vs. Output voltage range



6. Notes for Board Layout



① The power supply and GND are divided into three systems, received analog, transmitted analog and digital systems as shown above. For protection against latch-up, put the power supply and GND wires of the three systems together near the set power supply.

② Make sure that the wires of the three systems do not cross one another whenever possible.

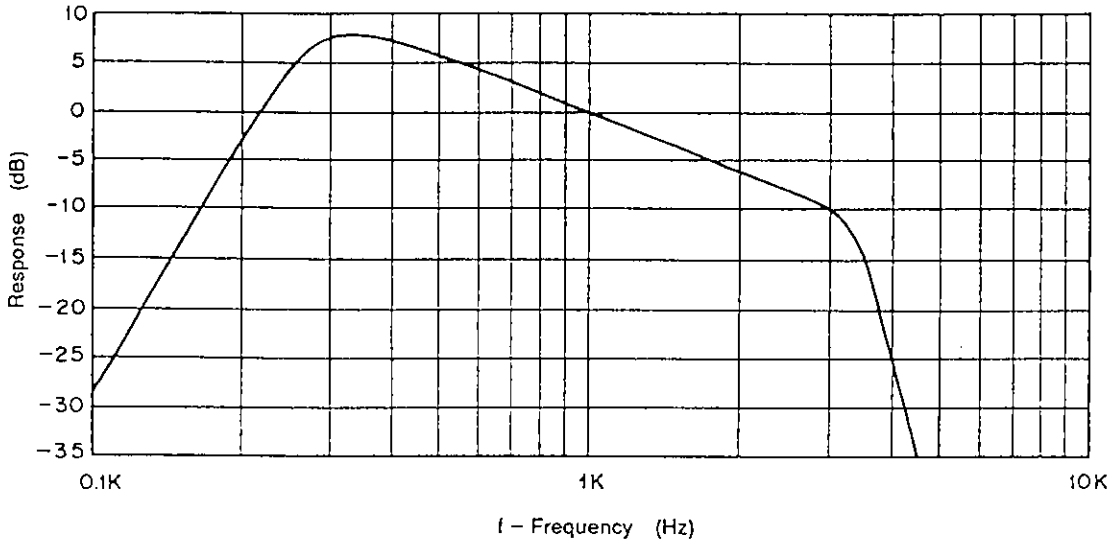
③ A by-pass capacitor should be connected directly near the pins.

④ Compander smoothing capacitors (Pins 55 and 16) and comparator capacitors (Pins 39 to 41) should be directly connected near the pins.

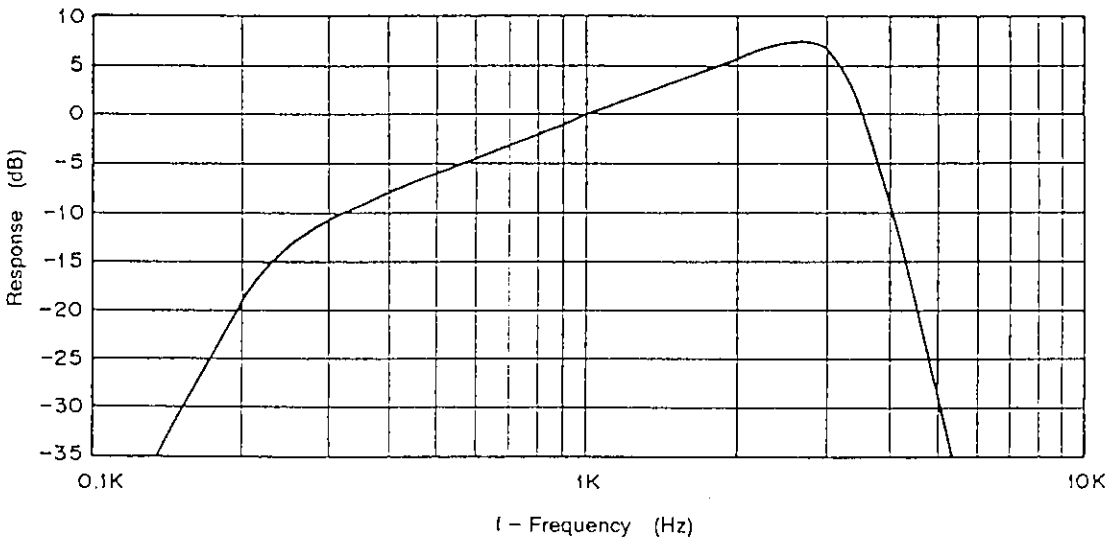
⑤ A compressor configuration circuit (Pins 18 to 22) should be compactly arranged at a position as close to the pins as possible.

Filter Characteristics

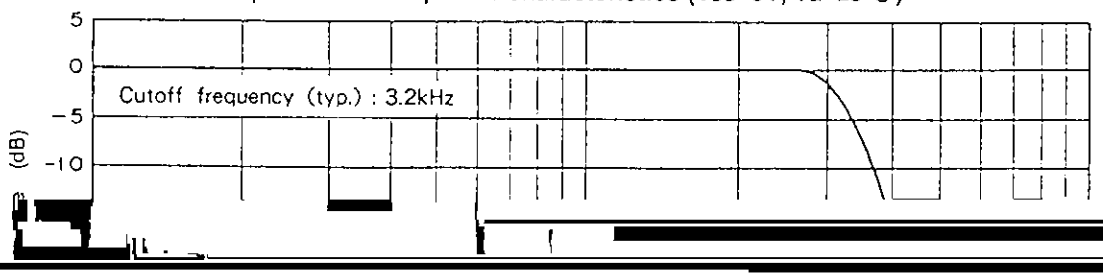
Received voice filter amplitude characteristic (V_{DD}=5V, Ta=25°C)



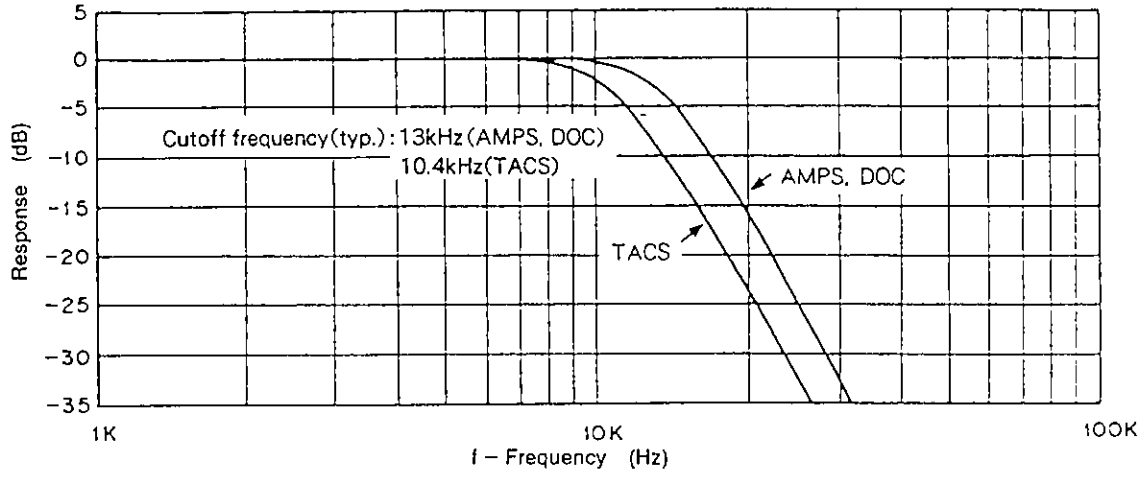
Transmitted voice filter (splatter filter included) amplitude characteristics (V_{DD}=5V, Ta=25°C)



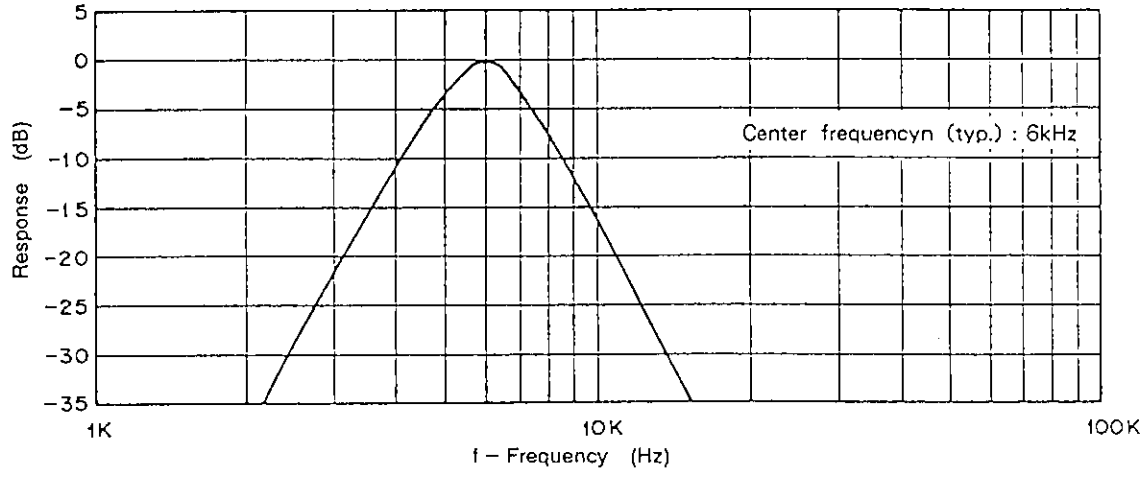
Splatter filter amplitude characteristics (V_{DD}=5V, Ta=25°C)



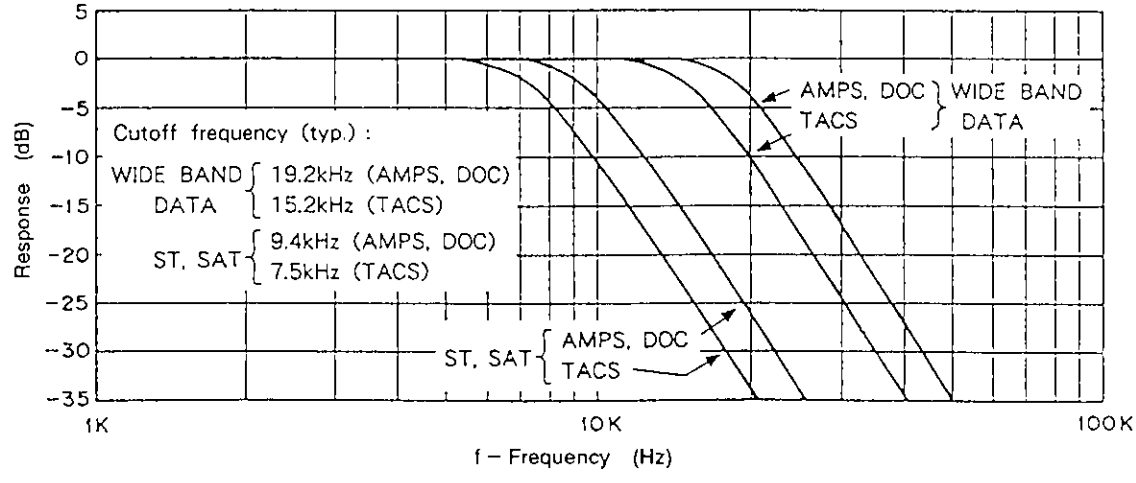
Received WIDE BAND DATA LPF amplitude characteristics (V_{DD}=5V, Ta=25°C)



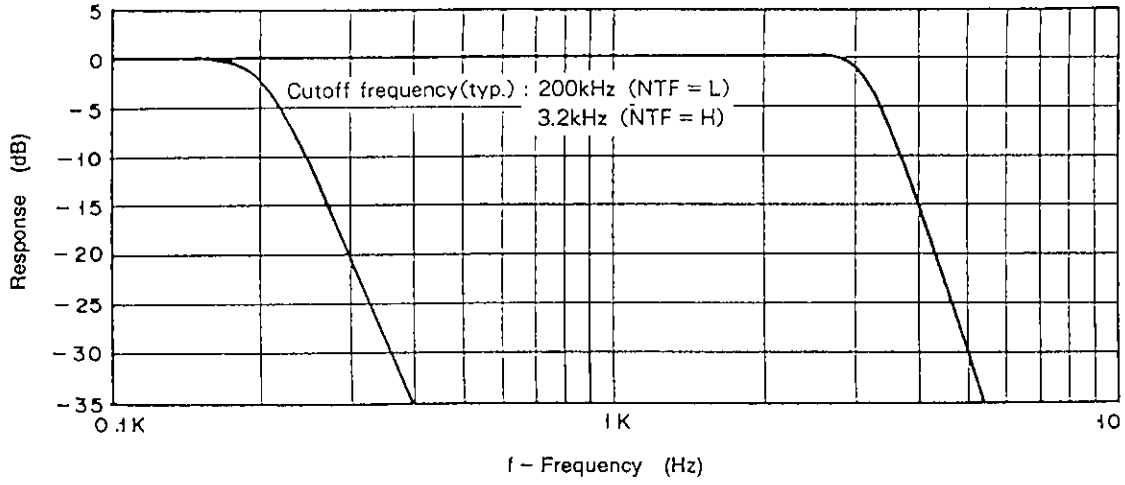
Received SAT BPF amplitude characteristics (V_{DD}=5V, Ta=25°C)



Transmitted WIDE BAND DATA, ST, SAT LPF amplitude characteristics (V_{DD}=5V, Ta=25°C)



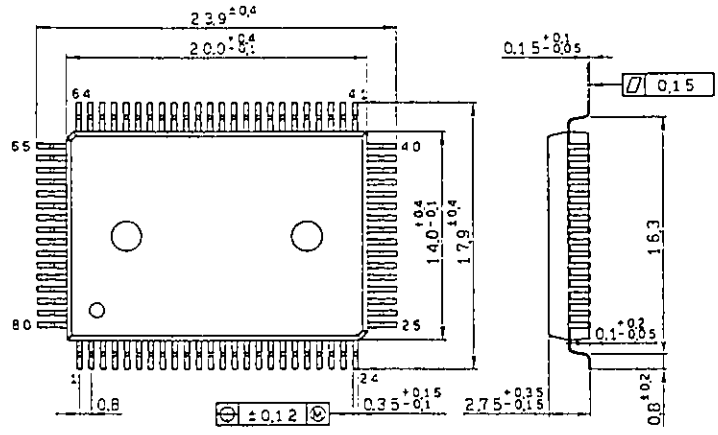
Received/Transmitted N-TACS data LPF amplitude characteristics (V_{DD}=5V, Ta=25°C)



Package Outline Unit : mm

CXD1272Q

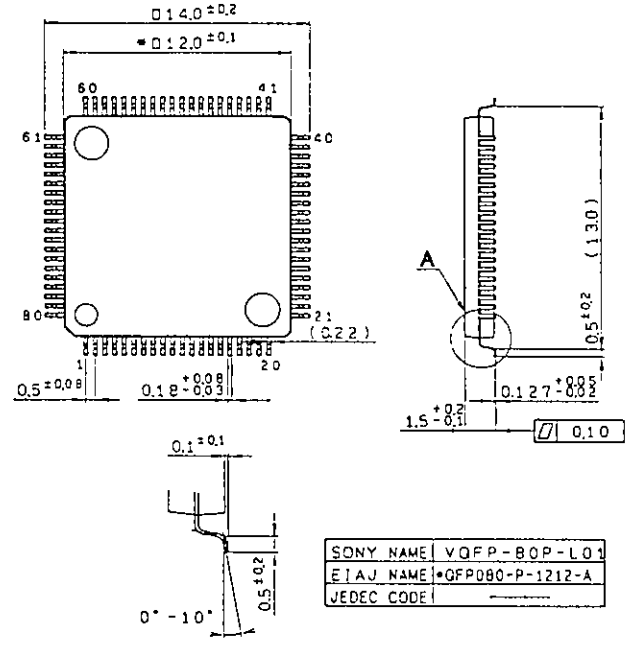
80pin QFP (Plastic) 1.6g



SONY NAME	QFP-80P-L01
EIAJ NAME	*QFP080-P-1420-A
JEDEC CODE	———

CXD1272R

80pin VQFP (Plastic) 0.5g



SONY NAME	VQFP-80P-L01
EIAJ NAME	*QFP080-P-1212-A
JEDEC CODE	———

Detailed diagram of A

Note) Dimensions marked with * does not include resin residue.