SONY

# CXD2460R

## Timing Generator for Progressive Scan CCD Image Sensor

### Description

The CXD2460R is an IC developed to generate the timing pulses required by Progressive Scan CCD image sensors as well as signal processing circuits.

### Features

- Electronic shutter function
- Supports non-interlaced operation
- Base oscillation frequency 28.636MHz
- Horizontal drive frequency switchable between 14.3/7.2MHz
- Switchable between FINE (Progressive Scan) mode or DRAFT (high-speed draft) mode
- Built-in vertical driver

### Applications

Progressive Scan CCD cameras

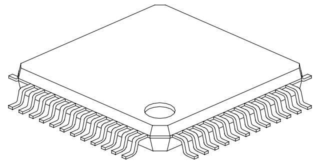
### Structure

Silicon gate CMOS IC

### Applicable CCD Image Sensor

ICX205AK

48 pin LQFP (Plastic)



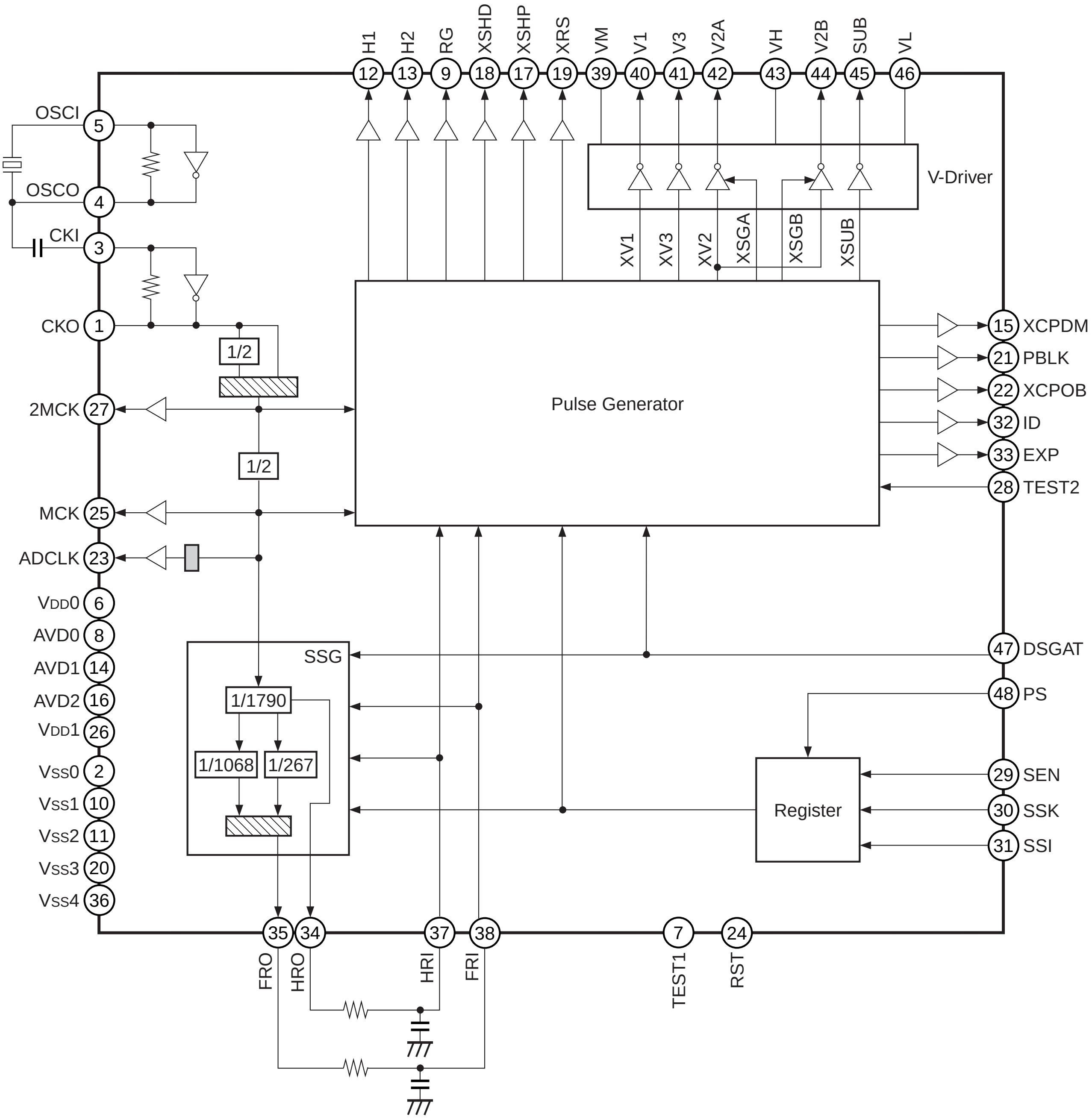
### Absolute Maximum Ratings

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}a$, $V_{DD}b$, $V_{DD}c$, $V_{DD}d$ | Vss – 0.5 to Vss + 7.0 | V |
| • Supply voltage | $V_{SS}$ | VL – 0.5 to VL + 26.0 | V |
| • Supply voltage | VH | VL – 0.5 to VL + 26.0 | V |
| • Supply voltage | VM | VL – 0.5 to VL + 26.0 | V |
| • Input voltage | $V_I$ | Vss – 0.5 to $V_{DD}$a,b,c,d + 0.5 | V |
| • Output voltage | $V_O$ | Vss – 0.5 to $V_{DD}$a,b,c,d + 0.5 | V |
| • Operating temperature | Topr | –20 to +75 | °C |
| • Storage temperature | Tstg | –55 to +150 | °C |

### Recommended Operating Conditions

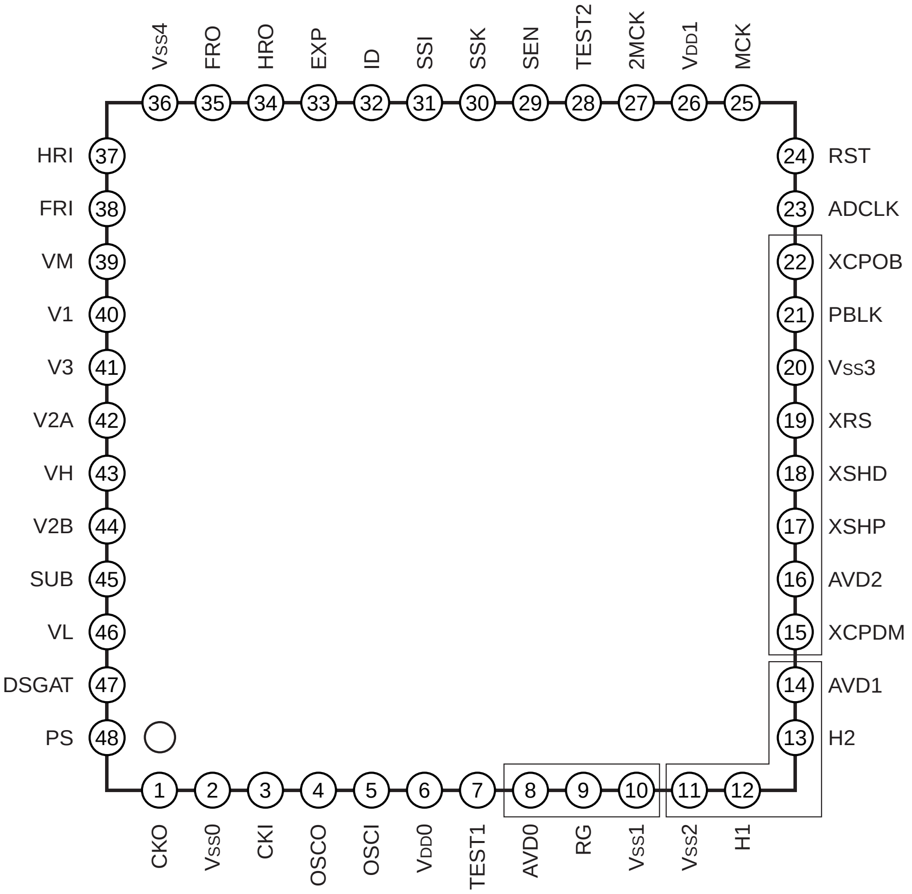
| | | | |
|---|---|---|---|
| • Supply voltage 1 | $V_{DD}a$, $V_{DD}b$, $V_{DD}d$ | 3.0 to 3.6 | V |
| • Supply voltage 2 | $V_{DD}c$ | 3.0 to 5.25 | V |
| • Supply voltage 3 | VH | 14.25 to 15.75 | V |
| • Supply voltage 4 | VL | –9.0 to –5.0 | V |
| • Supply voltage 5 | VM | 0 | V |
| • Operating temperature | Topr | –20 to +75 | °C |

## Block Diagram



XSGA and XSGB are readout pulses that use V2A and V2B, respectively, as the VH value.

**Pin Configuration** (Top View)



The enclosed pins use separate power supplies.

## Pin Description

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 1 | CKO | O | Oscillator output. (28.6MHz) |
| 2 | Vss0 | — | GND |
| 3 | CKI | I | Oscillator input. (28.6MHz) |
| 4 | OSCO | O | Inverter output for oscillation. (28.6MHz) |
| 5 | OSCI | I | Inverter input for oscillation. (28.6MHz) |
| 6 | VDD0 | — | Power supply. |
| 7 | TEST1 | I | Test. With pull-down resistor. Fix to low. |
| 8 | AVD0 | — | Power supply. |
| 9 | RG | O | Reset gate pulse output. |
| 10 | Vss1 | — | GND |
| 11 | Vss2 | — | GND |
| 12 | H1 | O | Clock output for horizontal CCD drive. |
| 13 | H2 | O | Clock output for horizontal CCD drive. |
| 14 | AVD1 | — | Power supply. |
| 15 | XCPDM | O | Clamp pulse. |
| 16 | AVD2 | — | Power supply. |
| 17 | XSHP | O | Sample-and-hold pulse. |
| 18 | XSHD | O | Sample-and-hold pulse. |
| 19 | XRS | O | Sample-and-hold pulse. |
| 20 | VSS3 | — | GND |
| 21 | PBLK | O | Blanking cleaning pulse. |
| 22 | XCPOB | O | Clamp pulse. |
| 23 | ADCLK | O | Clock output for AD conversion. |
| 24 | RST | I | Reset (Low: Reset, High: Normal operation).<br>Always input one reset pulse during power-on. |
| 25 | MCK | O | Clock output for digital circuit. |
| 26 | VDD1 | — | Power supply. |
| 27 | 2MCK | O | Clock output for digital circuit. |
| 28 | TEST2 | I | Test. Fix to high. |
| 29 | SEN | I | PS = High: Drive frequency setting input.<br>PS = Low: Serial setting strobe input. |
| 30 | SSK | I | PS = High: Readout method setting input.<br>PS = Low: Serial setting clock input. |
| 31 | SSI | I | PS = High: Shutter speed setting input.<br>PS = Low: Serial setting data input. |
| 32 | ID | O | Line identification signal output write enable pulse output or XSUB output. |
| 33 | EXP | O | Pulse output indicating exposure is underway or checksum result output. |

| Pin No. | Symbol | I/O | Description |
|---|---|---|---|
| 34 | HRO | O | Horizontal sync signal (HR) output or XSGA output. |
| 35 | FRO | O | Vertical sync signal (FR) output or XSGB output. |
| 36 | $V_{SS}4$ | — | GND |
| 37 | HRI | I | Horizontal sync signal (HR) input. |
| 38 | FRI | I | Vertical sync signal (FR) input. |
| 39 | VM | — | GND (vertical clock driver GND). |
| 40 | V1 | O | Clock output for vertical CCD drive. |
| 41 | V3 | O | Clock output for vertical CCD drive. |
| 42 | V2A | O | Clock output for vertical CCD drive. |
| 43 | VH | — | 15V power supply (vertical clock driver power supply). |
| 44 | V2B | O | Clock output for vertical CCD drive. |
| 45 | SUB | O | CCD electric charge sweep pulse output. |
| 46 | VL | — | –8.0V power supply (vertical clock driver power supply). |
| 47 | DSGAT | I | Output stop (Same operation control as SLP when low). |
| 48 | PS | I | Parallel/serial switching for mode setting input method.<br>(High: Parallel, Low: Serial) With pull-down resistor. |

## Electrical Characteristics

### DC Characteristics

(Within the recommended operating conditions)

| Item | Pins | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage 1 | $V_{DD}0$, $V_{DD}1$, | $V_{DD}a$ |  | 3.0 | 3.3 | 3.6 | V |
| Supply voltage 2 | AVD0 | $V_{DD}b$ |  | 3.0 | 3.3 | 3.6 | V |
| Supply voltage 3 | AVD1 | $V_{DD}c$ |  | 3.0 | 5.0 | 5.25 | V |
| Supply voltage 4 | AVD2 | $V_{DD}d$ |  | 3.0 | 3.3 | 3.6 | V |
| Supply voltage 5 | VH | VH |  | 14.5 | 15.0 | 15.5 | V |
| Supply voltage 6 | VM | VM |  | — | 0.0 | — | V |
| Supply voltage 7 | VL | VL |  | –9.0 |  | –5.0 | V |
| Input voltage 1 | CKI | $V_{IH1}$ |  | $0.7V_{DD}a$ |  |  | V |
|  |  | $V_{IL1}$ |  |  |  | $0.3V_{DD}a$ | V |
| Input voltage 2 | TEST1, PS | $V_{IH2}$ |  | $0.7V_{DD}a$ |  |  | V |
|  |  | $V_{IL2}$ |  |  |  | $0.3V_{DD}a$ | V |
| Input voltage 3 | RST, TEST2, SEN, SSK, SSI, HRI, FRI, DSGAT | $V_{t+1}$ |  | $0.8V_{DD}a$ |  |  | V |
|  |  | $V_{t-1}$ |  |  |  | $0.2V_{DD}a$ | V |
| Output voltage 1 | CKO, MCK, 2MCK | $V_{OH1}$ | Feed current where $I_{OH}$ = –10.0mA | $V_{DD}a$ – 0.8 |  |  | V |
|  |  | $V_{OL1}$ | Pull-in current where $I_{OL}$ = 7.2mA |  |  | 0.4 | V |
| Output voltage 2 | RG | $V_{OH2}$ | Feed current where $I_{OH}$ = –3.3mA | $V_{DD}b$ – 0.8 |  |  | V |
|  |  | $V_{OL2}$ | Pull-in current where $I_{OL}$ = 2.4mA |  |  | 0.4 | V |
| Output voltage 3 | H1, H2 | $V_{OH3}$ | Feed current where $I_{OH}$ = –36.0mA | $V_{DD}c$ – 0.8 |  |  | V |
|  |  | $V_{OL3}$ | Pull-in current where $I_{OL}$ = 24.0mA |  |  | 0.4 | V |
| Output voltage 4 | XCPDM, XSHP, XSHD, XRS, PBLK, XCPOB | $V_{OH4}$ | Feed current where $I_{OH}$ = –3.3mA | $V_{DD}d$ – 0.8 |  |  | V |
|  |  | $V_{OL4}$ | Pull-in current where $I_{OL}$ = 2.4mA |  |  | 0.4 | V |
| Output voltage 5 | ID, EXP, HRO, FRO | $V_{OH5}$ | Feed current where $I_{OH}$ = –2.4mA | $V_{DD}a$ – 0.8 |  |  | V |
|  |  | $V_{OL5}$ | Pull-in current where $I_{OL}$ = 4.8mA |  |  | 0.4 | V |
| Output voltage 6 | SUB | $V_{OH6}$ | Feed current where $I_{OH}$ = –4.0mA | VH – 0.25 |  |  | V |
|  |  | $V_{OL6}$ | Pull-in current where $I_{OL}$ = 5.4mA |  |  | VL + 0.25 | V |
| Output voltage 7 | V1, V3 | $V_{OM7}$ | Feed current where $I_{OH}$ = –5.0mA | VM – 0.25 |  |  | V |
|  |  | $V_{OL7}$ | Pull-in current where $I_{OL}$ = 10.0mA |  |  | VL + 0.25 | V |
| Output voltage 8 | V2A, V2B | $V_{OM101}$ | Feed current where $I_{OH}$ = –7.2mA | VH – 0.25 |  |  | V |
|  |  | $V_{OM102}$ | Pull-in current where $I_{OL}$ = 5.0mA |  |  | VM + 0.25 | V |
|  |  | $V_{OL8}$ | Feed current where $I_{OH}$ = –5.0mA | VM – 0.25 |  |  | V |
|  |  | $V_{OL8}$ | Pull-in current where $I_{OL}$ = 10.0mA |  |  | VL + 0.25 | V |

### Inverter I/O Characteristics for Oscillation

(Within the recommended operating conditions)

| Item | Pins | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Logical Vth | OSCI | LVth | | | $V_{DD}a/2$ | | V |
| Input voltage | OSCI | $V_{IH}$ | | $0.7V_{DD}a$ | | | V |
| | | $V_{IL}$ | | | | $0.3V_{DD}a$ | V |
| Output voltage | OSCO | $V_{OH}$ | Feed current where $I_{OH}$ = –6.0mA | $V_{DD}a/2$ | | | V |
| | | $V_{OL}$ | Pull-in current where $I_{OL}$ = 6.0mA | | | $V_{DD}a/2$ | V |
| Feedback resistor | OSCI, OSCO | RFB | $V_{IN} = V_{DD}a$ or Vss | 500k | 2M | 5M | Ω |
| Oscillator frequency | OSCI, OSCO | f | | 20 | | 50 | MHz |

### Base Oscillation Clock Input Characteristics

(Within the recommended operating conditions)

| Item | Pins | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Logical Vth | CKI | LVth | | | $V_{DD}a/2$ | | V |
| Input voltage | | $V_{IH}$ | | $0.7V_{DD}a$ | | | V |
| | | $V_{IL}$ | | | | $0.3V_{DD}a$ | V |
| Input amplitude | | $V_{IN}$ | fmax 50MHz sine wave | 0.3 | | | Vp-p |

*1 Input voltage is the input voltage characteristics for direct input from an external source. Input amplitude is the input amplitude characteristics for input through capacitor.

### Switching Characteristics

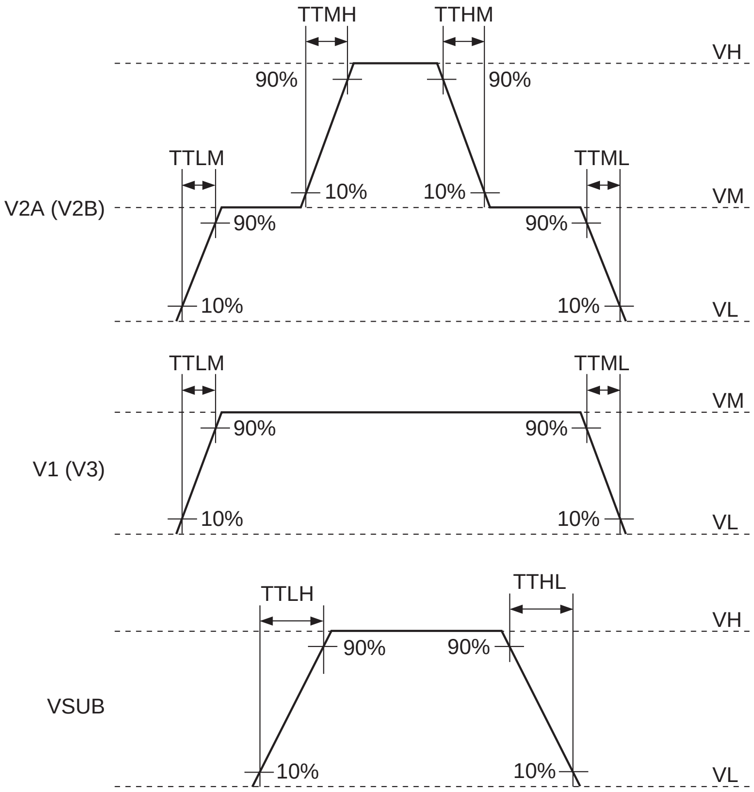
(VH = 15.0V, VM = GND, VL = –8.5V)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Rise time | TTLM | VL to VM | | 350 | 550 | ns |
| | TTMH | VM to VH | | 450 | 700 | ns |
| | TTLH | VL to VH | | 50 | 80 | ns |
| Fall time | TTML | VM to VL | | 250 | 400 | ns |
| | TTHM | VH to VM | | 300 | 450 | ns |
| | TTHL | VH to VL | | 50 | 80 | ns |
| Output noise voltage | VCLH | | | | 1.0 | V |
| | VCLL | | | | 1.0 | V |
| | VCMH | | | | 1.0 | V |
| | VCML | | | | 1.0 | V |

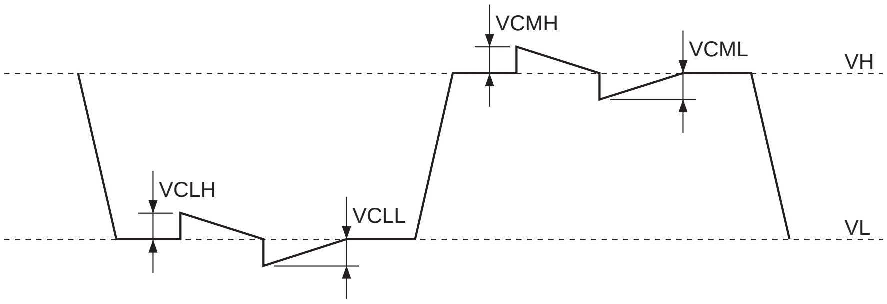
*1 The MOS structure of this IC has a low tolerance for static electricity, so full care should be given for measures to prevent electrostatic discharge.

*2 For noise and latch-up countermeasures, be sure to connect a bypass capacitor (0.1µF or more) between each power supply pin (VH, VL) and GND.

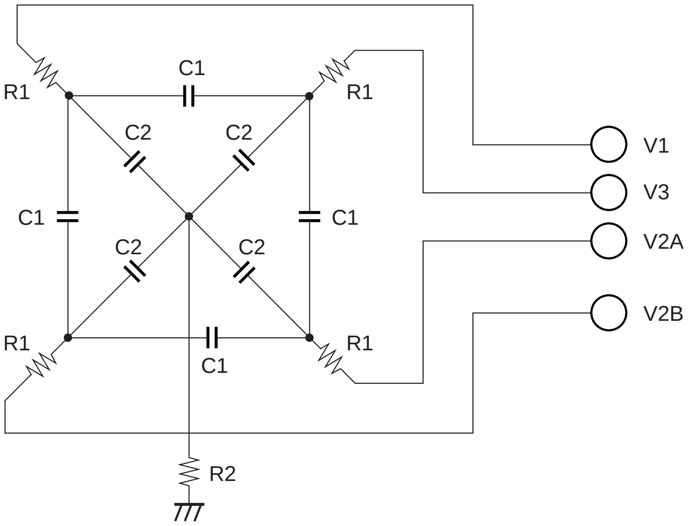
## Switching Waveforms



## Waveform Noise



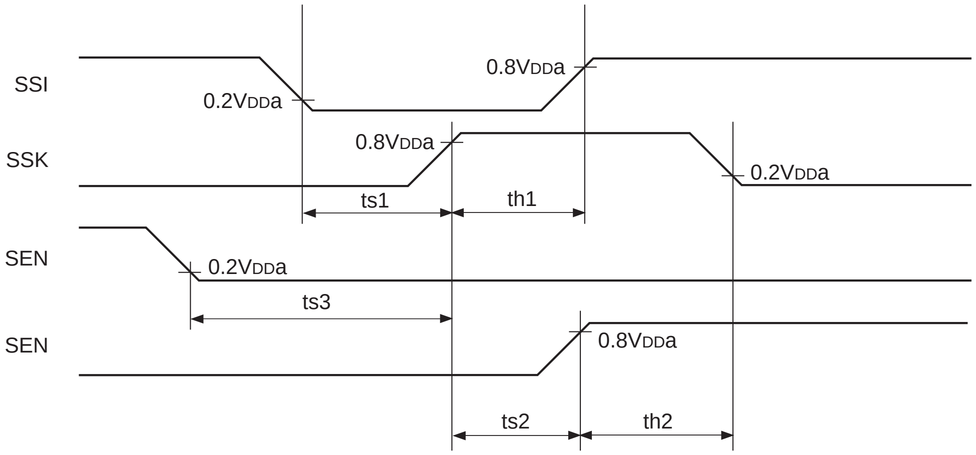
## Measurement Circuit



R1: 27Ω
R2: 5Ω
C1: 1500pF
C2: 3300pF

## AC Characteristics

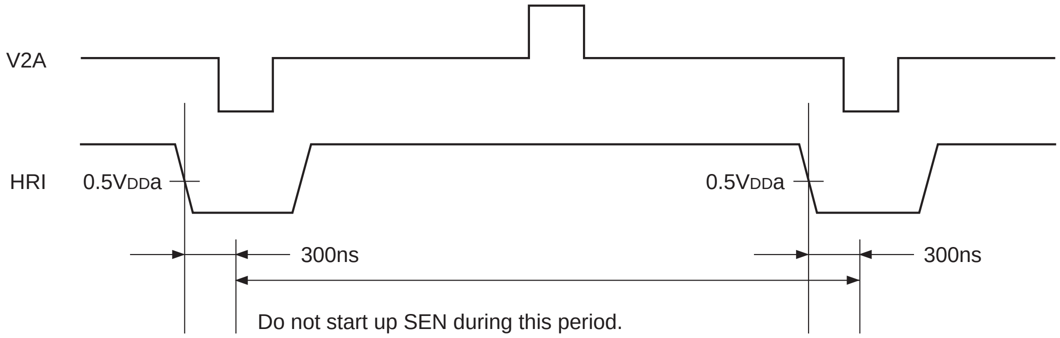
### 1) AC characteristics between the serial interface clocks



(Within the recommended operating conditions)

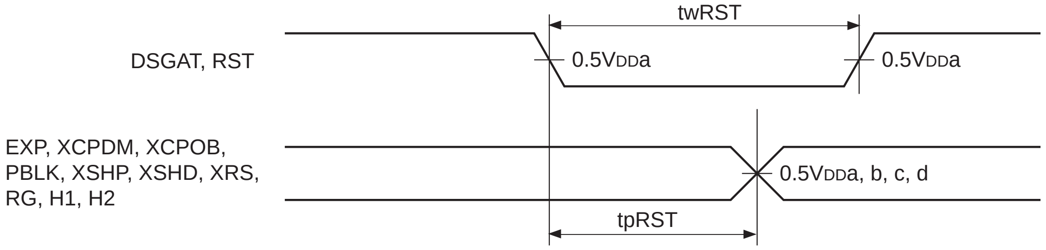
| Symbol | Definition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| ts1 | SSI setup time, activated by the rising edge of SSK | 20 | | | ns |
| th1 | SSI hold time, activated by the rising edge of SSK | 20 | | | ns |
| ts2 | SSK setup time, activated by the rising edge of SEN | 20 | | | ns |
| th2 | SSK hold time, activated by the rising edge of SEN | 20 | | | ns |
| ts3 | SEN setup time, activated by the rising edge of SSK | 20 | | | ns |
| fk | SSK frequency | | | 7.15 | MHz |

### 2) Serial interface clock internal loading characteristics



Do not start up SEN during this period.
(From 300ns from the falling edge of HRI immediately before generation of XSGA pulse to 300ns from the falling edge of HRI immediately after generation of XSGA pulse)

### 3) Output timing characteristics using DSGAT and RST

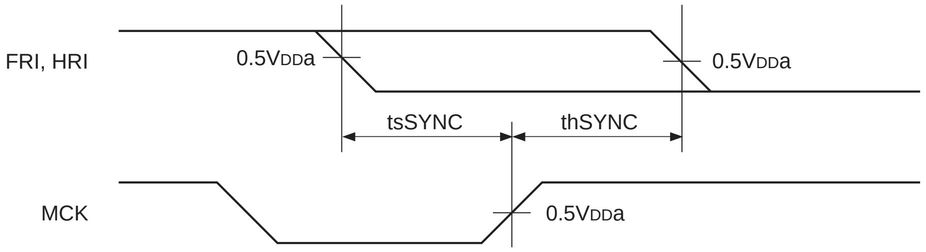


H1 and H2 load = 270pF

EXP, XCPDM, PBLK, XSHP, XSHD, XRS and RG load = 10pF (Within the recommended operating conditions)

| Symbol | Definition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| tpRST | Time until the above outputs reach the specified value after the fall of DSGAT and RST | | | 125 | ns |
| twRST | RST and DSGAT pulse width | 10 | | | ns |

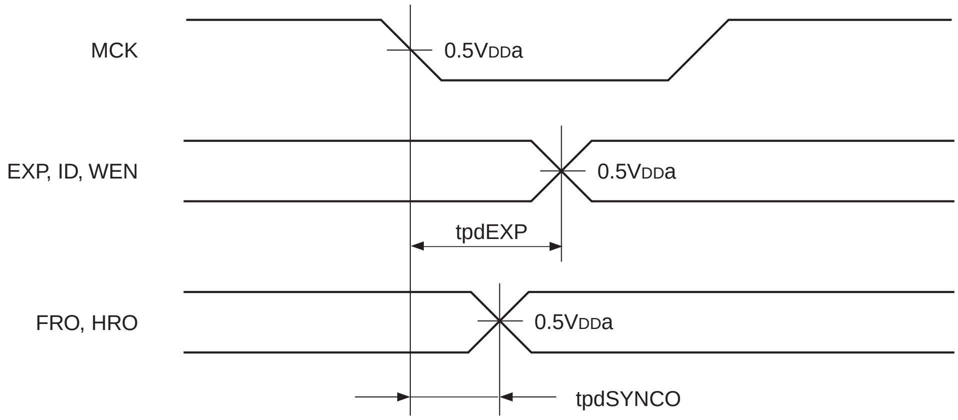
### 4) FRI and HRI loading characteristics



MCK load = 35pF (Within the recommended operating conditions)

| Symbol | Definition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| tsSYNC | FRI and HRI setup time, activated by the rising edge of MCK | 5 | | | ns |
| thSYNC | FRI and HRI hold time, activated by the rising edge of MCK | 5 | | | ns |

### 5) Output variation characteristics of ID, WEN, EXP, FRO and HRO



EXP, ID and WEN load = 10pF (Within the recommended operating conditions)

| Symbol | Definition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| tpdEXP | Time until the WEN, ID and EXP outputs change after the fall of MCK | 0.5 | | 8.5 | ns |
| tpdSYNCO | Time until the FRO and HRO outputs change after the fall of MCK | 0.5 | | 3.5 | ns |

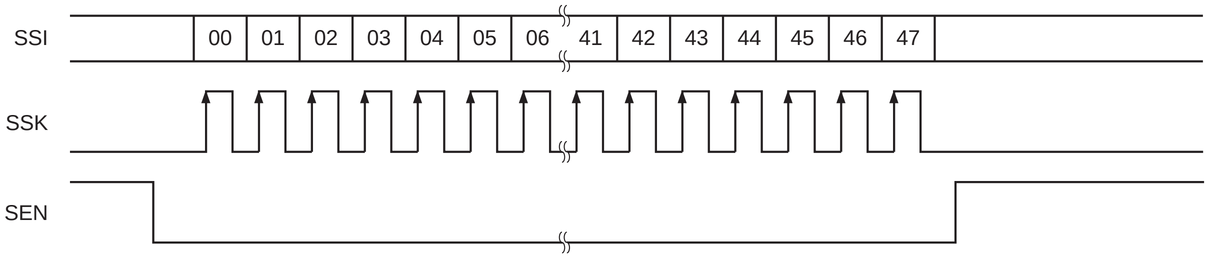
## Description of Operation

### 1. Progressive Scan CCD drive pulse generation

- Combining this IC with a crystal oscillator generates a fundamental frequency of 28.636MHz.
- CCD drive pulse generation is synchronized with HRI and FRI.
- The CCD drive method can be changed to various modes by inputting serial data or parallel data to the CXD2460R.
- The various drive methods possessed by the CXD2460R are shown in the Timing Charts A-1 to 3 (V rate) and B-1 to 6 (H rate).

### 2. Serial data input method

- All CXD2460R operations can be controlled via the serial data. The serial data format is as follows.



**Serial data format**

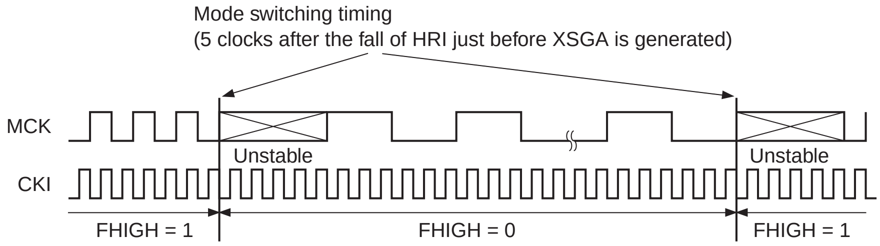
**Serial data**

| Data | Symbol | Function | | When reset |
|---|---|---|---|---|
| D00 to D07 | CHIP | Chip switching | See D00 to D07 CHIP. | All 0 |
| D08 to D11 | CTGRY | Category switching | See D08 to D11 CTGRY. | All 0 |
| D12 to D39 | DATA | Control data for each category<br>The meaning of this CTGRY control data differs according to the category set by D08 to D11. | See D12 to D39 DATA. | All 0 |
| D40 to D47 | Checksum bits | Checksum bits | See D40 to D47 CHKSUM. | All 0 |

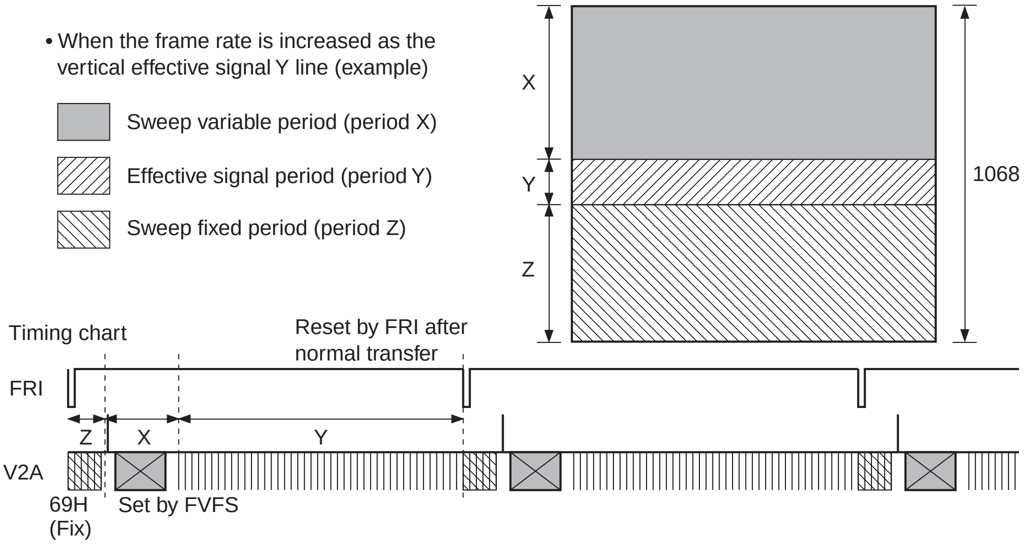
### 3. Serial data and description of functions

<table>
<tr><th></th><th>Detailed description</th></tr>
<tr><td>D00<br>to<br>D07<br>CHIP</td><td>The serial interface data is loaded to the CXD2460R when D00 and D07 are "1". However, this assumes that D40 to D47 CHKSUM is satisfied.
<table>
<tr><th>D07</th><th>D06</th><th>D05</th><th>D04</th><th>D03</th><th>D02</th><th>D01</th><th>D00</th><th>Function</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Loading to the CXD2460R</td></tr>
</table></td></tr>
<tr><td>D08<br>to<br>D11<br>CTGRY</td><td>This CTGRY data indicates the functions that the serial interface data controls.
<table>
<tr><th>D11</th><th>D10</th><th>D09</th><th>D08</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Mode control data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Electronic shutter control data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>High-speed phase adjustment data (Set all of D12 to D39 to "0".)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>System setting data</td></tr>
</table>
Input of values other than those listed above is prohibited.</td></tr>
</table>

**CTGRY: Mode control data**

<table>
<tr><th></th><th>Detailed description</th></tr>
<tr><td>D12<br>FHIGH</td><td>0: Power saving drive mode<br>1: High-speed drive mode<br><br>When FHIGH = 0, the clock input to CKI is immediately frequency divided by 1/2 and loaded internally.


The high-speed phases of H1, H2, RG, XSHP, XSHD, XRS, ADCLK and other pulses are always logically the same phase with respect to MCK.</td></tr>
<tr><td>D13<br>FINE</td><td>0: DRAFT mode<br>1: FINE mode<br><br>In FINE mode, image data is taken by the normal Progressive Scan method.<br>In DRAFT mode, image data is taken by pulse elimination readout. This enables a frame rate four times that during FINE mode. The mode is switched at the fall of HRI just before XSGA.<br>Note that the FRO output is also switched accordingly. (DRAFT mode: 267H, FINE mode: 1068H)</td></tr>
<tr><td>D14<br>NSG</td><td>0: Normal operation<br>1: Readout prohibited mode<br><br>In readout prohibited mode, a readout pulse is not added even at the timing when a readout pulse is added to V2A and V2B (VH value). (V1, V2 and V3 are not modulated.)<br>The mode is normally switched at the fall of HRI just before the position where the readout pulse is added.</td></tr>
</table>

| | Detailed description |
|---|---|
| D15<br>FS | 0: Normal operation<br>1: FS mode<br>In order to increase the frame rate, a certain portion of the captured image of CCD can be cut out by performing high-speed sweep.<br>In FS mode, high-speed sweep is performed for the V registers of the entire image (period Z) after FRI input. Next, high-speed sweep is performed again for only the desired period (period X) after generating the XSGA/XSGB pulses. Then, after performing normal V transfer and outputting the effective signal (period Y), high-speed sweep is performed for the entire image again by inputting FRI at the desired timing. This makes it possible to take only the desired portion in the V direction, thus effectively increasing the frame rate.<br>Operation is fixed during period Z, with 20 lines swept every 1H and repeating over a 69H period. During period X, first XSGA/XSGB are generated. These pulses are dependent on serial data FINE. In other words, if FINE = 1, then both XSGA and XSGB are generated, while if FINE = 0, only XSGA is generated. Next, sweep operation starts. This period is set in serial data FVFS (system setting data: D21 to D26) in HRI units. If FINE = 1, sweeping is performed at 8 lines per 1H, and if FINE = 0, sweeping is performed at 20 lines per 1H.<br>The operations of V1, V2 and V3 after readout during period Y differ depending on the FINE data.<br> |
| D16<br>to<br>D17 | Set to "0". |

| | Detailed description |
|---|---|
| D17<br>to<br>D18<br>STB | Operation control settings |

Operation control settings

The operating mode control bits are loaded to the CXD2460R at the rise timing of the SEN input, and control is applied immediately.

| D19 | D18 | Symbol | Control mode |
|---|---|---|---|
| 0 | 0 | CAM | Normal operation mode |
| 0 | 1 | SLP | Sleep mode (mode for the status where CCD drive is not required) |
| 1 | X | STN | Standby mode |

**Pin status during operation control**

| Pin No. | Symbol | CAM | SLP | STN | RST* | Pin No. | Symbol | CAM | SLP | STN | RST* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | CKO | ACT | ACT | ACT | ACT | 25 | MCK | ACT | ACT | ACT | ACT |
| 2 | $V_{SS}0$ | — | — | — | — | 26 | $V_{DD}1$ | — | — | — | — |
| 3 | CKI | ACT | ACT | ACT | ACT | 27 | 2MCK | ACT | ACT | ACT | ACT |
| 4 | OSCO | ACT | ACT | ACT | ACT | 28 | TEST2 | — | — | — | — |
| 5 | OSCI | ACT | ACT | ACT | ACT | 29 | SEN | ACT | ACT | — | — |
| 6 | $V_{DD}0$ | — | — | — | — | 30 | SSK | ACT | ACT | — | — |
| 7 | TEST1 | — | — | — | — | 31 | SSI | ACT | ACT | — | — |
| 8 | AVD0 | — | — | — | — | 32 | ID | ACT | L | L | L |
| 9 | RG | ACT | L | L | L | 33 | EXP | ACT | L | L | L |
| 10 | $V_{SS}1$ | — | — | — | — | 34 | HRO | ACT | ACT | L | L |
| 11 | $V_{SS}2$ | — | — | — | — | 35 | FRO | ACT | ACT | L | L |
| 12 | H1 | ACT | L | L | L | 36 | $V_{SS}4$ | — | — | — | — |
| 13 | H2 | ACT | L | L | L | 37 | HRI | ACT | ACT | — | — |
| 14 | AVD1 | — | — | — | — | 38 | FRI | ACT | ACT | — | — |
| 15 | XCPDM | ACT | L | L | L | 39 | VM | — | — | — | — |
| 16 | AVD2 | — | — | — | — | 40 | V1 | ACT | VM | VM | VM |
| 17 | XSHP | ACT | L | L | L | 41 | V3 | ACT | VM | VM | VM |
| 18 | XSHD | ACT | L | L | L | 42 | V2A | ACT | VH | VH | VH |
| 19 | XRS | ACT | L | L | L | 43 | VH | — | — | — | — |
| 20 | $V_{SS}3$ | — | — | — | — | 44 | V2B | ACT | VH | VH | VH |
| 21 | PBLK | ACT | L | L | L | 45 | SUB | ACT | VH | VH | VH |
| 22 | XCPOB | ACT | L | L | L | 46 | VL | — | — | — | — |
| 23 | ADCLK | ACT | L | L | L | 47 | DSGAT | ACT | ACT | L | L |
| 24 | RST | ACT | ACT | ACT | ACT | 48 | PS | ACT | ACT | ACT | ACT |

* See "6. RST pulse" for a detailed description of RST.

**Note)** ACT indicates circuit operation, and L indicates "low" output level in the controlled status. For sleep mode or standby mode, stop supplying VH and VL power supplies with CCD image sensor.

| | Detailed description |
|---|---|
| D20<br>EXPXEN | 0: The EXP pulse indicating the exposure period is generated (when PS = low).<br>1: The EXP pulse indicating the exposure period is not generated (when PS = low), and is constantly fixed to low.<br>This bit is invalid when STATUS = 1.<br>Note that the STB setting has priority. |
| D21<br>to<br>D24 | Invalid data |
| D25<br>to<br>D29<br>VSHUT | Low-speed electronic shutter setting.<br>The value set here is the number of FR during which readout operation is not performed even if there is input. The setting range is from "0" to "31". When set to "0", readout operation is performed at the first FR.<br>When FS = 1, this bit is invalid. |
| D30<br>to<br>D39 | Invalid data |

| MSB | | | | LSB | Function |
|---|---|---|---|---|---|
| D29 | D28 | D27 | D26 | D25 | Number of FR during which readout operation is not performed |

**CXD2460R clock system**

When using a 28.636MHz crystal

| | FHIGH | FINE | MCK frequency | 2MCK pin output | Frame rate | |
|---|---|---|---|---|---|---|
| Mode1 | 1 | 1 | 14.3MHz | 28.6MHz | 7.5Frame/s | Basic |
| Mode2 | 1 | 0 | 14.3MHz | 28.6MHz | 30Frame/s | DRAFT |
| Mode3 | 0 | 0 | 7.2MHz | 14.3MHz | 15Frame/s | Power-save |

**Note)** Combinations of FHIGH and FINE other than those listed above are prohibited.

**CTGRY: Electronic shutter control data**

<table>
<tr><th></th><th>Detailed description</th></tr>
<tr><td>D12<br>to<br>D22<br>HSHUT</td><td>High-speed electronic shutter setting.<br>The value set here is the number of SUB pulses from FR to the next FR.
<table>
<tr><td>MSB</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>LSB</td><td>Function</td></tr>
<tr><td>D22</td><td>D21</td><td>D20</td><td>D19</td><td>D18</td><td>D17</td><td>D16</td><td>D15</td><td>D14</td><td>D13</td><td>D12</td><td>Number of SUB pulses setting</td></tr>
</table></td></tr>
<tr><td>D23<br>to<br>D39</td><td>Input "0".</td></tr>
</table>

High-speed and low-speed electronic shutter can be used together. Therefore, the exposure time is as follows:

FR cycle × VSHUT + (fv – HSHUT) × HR cycle + 634/MCK frequency [Hz] = Exposure time [s]

(fv: Number of HR in 1FR)

**CTGRY: System setting data**

<table>
<tr><th></th><th>Detailed description</th></tr>
<tr><td>D12<br>SGXEN</td><td>0: Internal SSG (Sync Signal Generator) functions operate to generate FRO and HRO.<br>1: Internal SSG functions are stopped, and the FRO and HRO pulses are fixed to low.<br>Note that the STB setting has priority. Set SGXEN to "1" in the case of input of a CXD2460R sync signal from the outside.</td></tr>
<tr><td>D13<br>EXSG</td><td>0: Normal operation<br>1: XSGA and XSGB are output from the HRO and FRO pins.<br>Note that the output pulse amplitude is $V_{SS}$ to $V_{DD}$a.</td></tr>
<tr><td>D14<br>to<br>D15<br>IDSEL</td><td>These bits select the pulse output from the ID pin.
<table>
<tr><th colspan="2" rowspan="2"></th><th colspan="2">D15</th></tr>
<tr><th>0</th><th>1</th></tr>
<tr><td rowspan="2">D14</td><td>0</td><td>ID pulse output</td><td>WEN pulse output</td></tr>
<tr><td>1</td><td>XSUB pulse output</td><td>ID pulse output</td></tr>
</table>
XSUB: Inverted SUB pulse output at the amplitude of $V_{SS}$ to $V_{DD}$a</td></tr>
<tr><td>D16<br>VTXEN</td><td>0: VT (readout clock) is added to V2A, V2B and V3 as normal.<br>1: VT is not added to V2A, V2B and V3.<br>During readout, only the modulation necessary for readout is performed.<br>Note that this setting has priority over mode control data NSG (D14).</td></tr>
<tr><td>D17<br>CHKSUM</td><td>0: Checksum is not performed and the checksum data is invalid. (However, dummy data must be set in the CHKSUM register.)<br>1: Checksum is performed. This data is reflected even if the checksum results are NG.</td></tr>
<tr><td>D18<br>STATUS</td><td>0: The EXP pulse is output from the EXP pin.<br>1: High is indicated if the checksum results from the EXP pin are OK, and low if the results are NG.<br>This pulse is output at the rise of SEN, and reset high again at the fall of SEN. This pulse has priority over mode control data EXP.</td></tr>
<tr><td>D19<br>to<br>D22</td><td>Input "0".</td></tr>
<tr><td>D23<br>to<br>D29<br>FVFS</td><td>These bits set the high-speed sweep period (unit: H) in FS mode.
<table>
<tr><td colspan="7">MSB LSB</td></tr>
<tr><td>D29</td><td>D28</td><td>D27</td><td>D26</td><td>D25</td><td>D24</td><td>D23</td></tr>
</table>
The high-speed sweep is perfomed for 8 lines for every 1H when FINE = 1, and 20 lines for every 1H when FINE = 0.</td></tr>
</table>

| | Detailed description |
|---|---|
| D30<br>XVCK | 0: Normal operation<br>1: V1, V2 and V3 are inverted and output as XV1, XV2 and XV3. The amplitude is from VL to VM. |
| D31<br>to<br>D39 | Invalid data |

**CHKSUM**

| | Detailed description |
|---|---|
| D40<br>to<br>D47 | These are the checksum bits.<br>MSB LSB<br>D07 D06 D05 D04 D03 D02 D01 D00<br>D15 D14 D13 D12 D11 D10 D09 D08<br>D23 D22 D21 D20 D19 D18 D17 D16<br>D31 D30 D29 D28 D27 D26 D25 D24<br>D39 D38 D37 D36 D35 D34 D33 D32<br>+) $\boxed{\text{D47 D46 D45 D44 D43 D42 D41 D40}}$ → $\boxed{\text{CHKSUM}}$<br>If the total = 0, the checksum results are OK.<br>Serial data is loaded to the internal registers only when checksum is OK.<br>Data is not reflected to the registers if checksum is NG.<br>Also, when CHKSUM = 0, the checksum results are always OK and the data is reflected to the registers. |

### 4. Shutter speed setting specifications when PS = H

When PS = H, the CXD2460R can be controlled without inputting serial data by using the SEN, SSK and SSI pins.

<table>
<tr><th>Pin</th><th></th><th>When L</th><th>When H</th></tr>
<tr><td>SEN</td><td>FHIGH<br>(horizontal drive frequency)</td><td>Serial register FHIGH = 0.</td><td>Serial register FHIGH = 1.</td></tr>
<tr><td>SSK</td><td>FINE<br>(readout method)</td><td>Serial register FINE = 0 and the CXD2460R operates in DRAFT mode.</td><td>Serial register FINE = 1 and the CXD2460R operates in FINE mode.</td></tr>
<tr><td>SSI</td><td>HSHUT,<br>VSHUT<br>(exposure time)</td><td colspan="2">Number of SUB pulses when PS = H
<table>
<tr><th colspan="2" rowspan="2"></th><th colspan="2">SSK</th></tr>
<tr><th>L</th><th>H</th></tr>
<tr><td rowspan="2">SEN</td><td>L</td><td>251<br>201</td><td>1052<br>1002</td></tr>
<tr><td>H</td><td>235<br>134</td><td>1034<br>935</td></tr>
</table>
Upper number: When SSI = H (1/250)<br>Lower number: When SSI = L (1/60)</td></tr>
</table>

Other registers hold the value input when PS = L, and assume the status indicated by STB when the RST pulse is input.

## 5. Reflection position of each data

Each serial data is reflected at the timing shown in the table below. The reflection position is the same when PS = H. When using the low-speed electronic shutter, the data is not reflected at FR where XSG is not generated (a readout pulse is not added to V2A).

**Table 5-1. Serial data reflection timing**

| Data | Reflection position |
|---|---|
| Mode control data (STB) | SEN rise |
| Mode control data (EXPXEN) | XSGA pulse rise |
| Mode control data (other than STB and EXPXEN) | HRI*1 fall just before XSGA pulse generation |
| Electronic shutter control data | HRI*2 fall just after XSGA pulse generation |
| High-speed phase adjustment data | HRI*1 fall just before XSGA pulse generation |
| System setting data (SGXEN) | SEN rise |
| System setting data (other than SGXEN) | HRI*2 fall just before XSGA pulse generation |

*1 For FS mode, 7HRI later from FRI fall.

*2 For FS mode, 8HRI later from FRI fall.

## 6. RST pulse

Setting Pin 30 to low resets the system. The serial data values after reset are as shown in the "Serial data" table.

Also, some internal circuits stop operating when RST = L. For a description of the pin status when RST = L, see the "Pin status during operation control" table given in the detailed description of STB under "3. Serial data and description of functions".

## 7. DSGAT

DSGAT is ON when low and the CXD2460R is set to sleep mode as with SLP of STB.

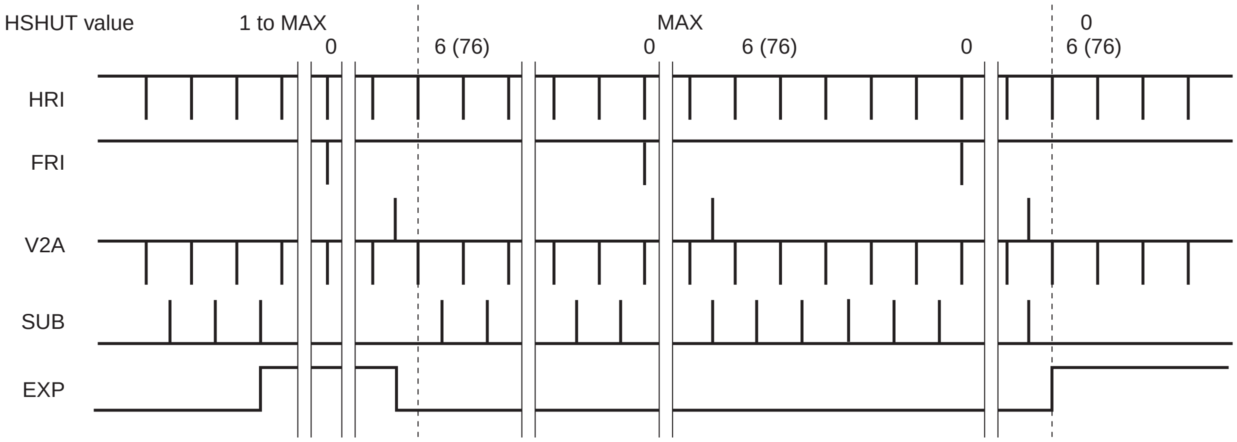
Note that control is applied when either or both of DSGAT and SLP are ON. Also, when STN is ON, the CXD2460R is set to standby mode regardless of the DSGAT status.

## 8. EXP pulse

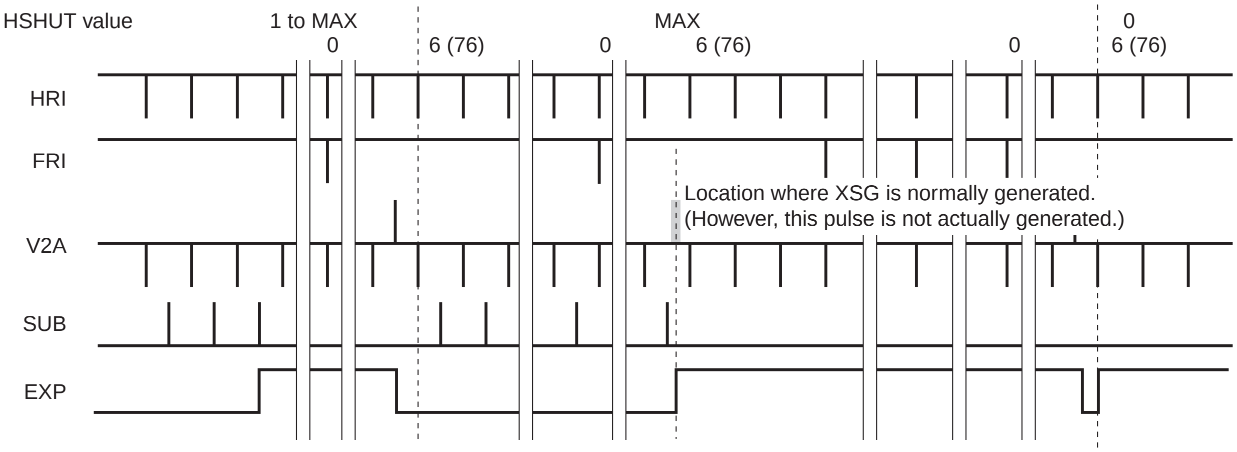
The EXP pulse indicates the exposure period.

The details are shown on the following pages.

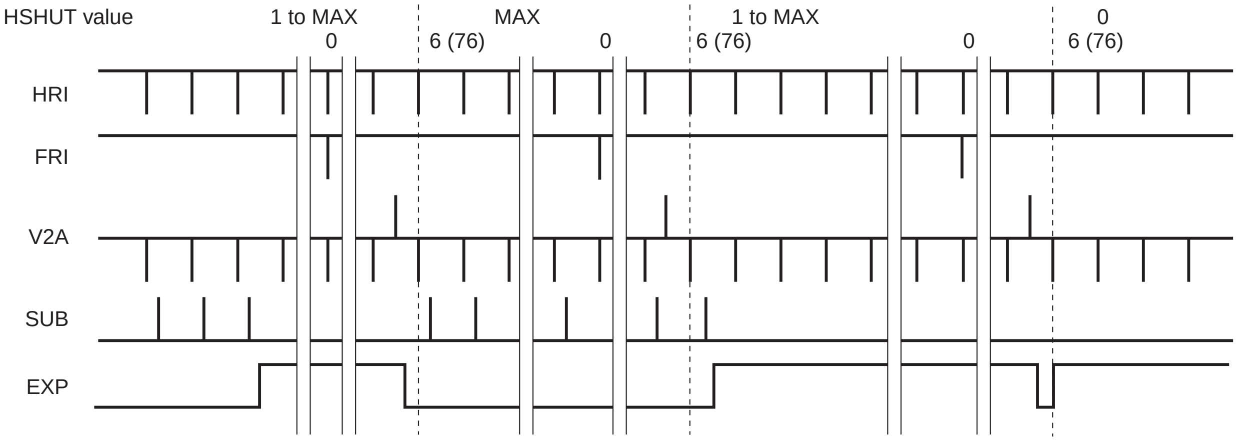
(1) HSHUT ≥ MAX



(2) HSHUT ≥ MAX (with low-speed electronic shutter)

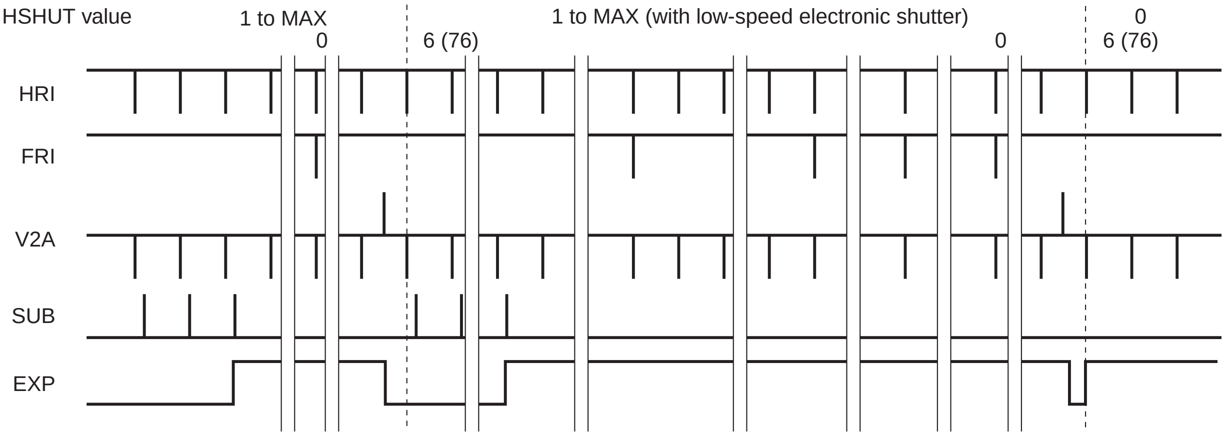


(3) 1 ≤ HSHUT < MAX

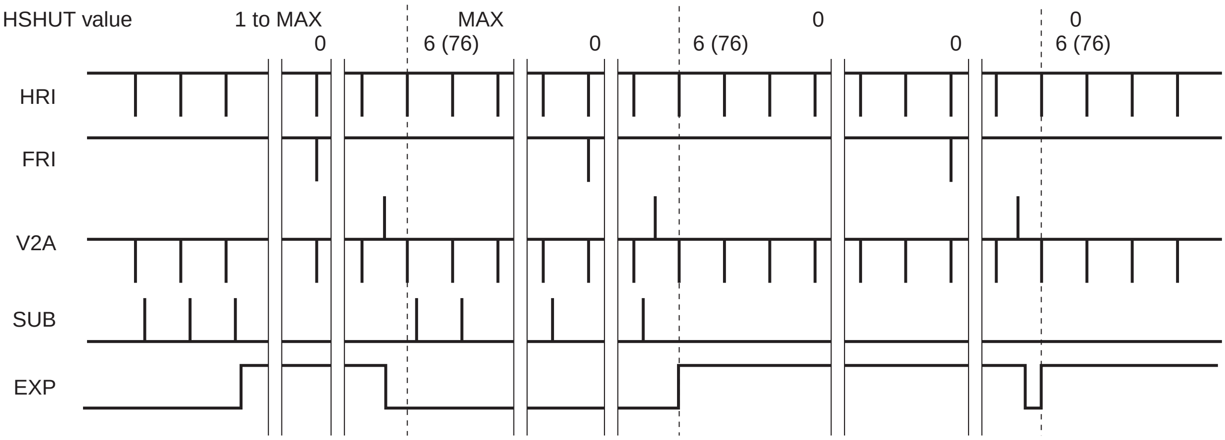


Numbers in parentheses are for FS mode.

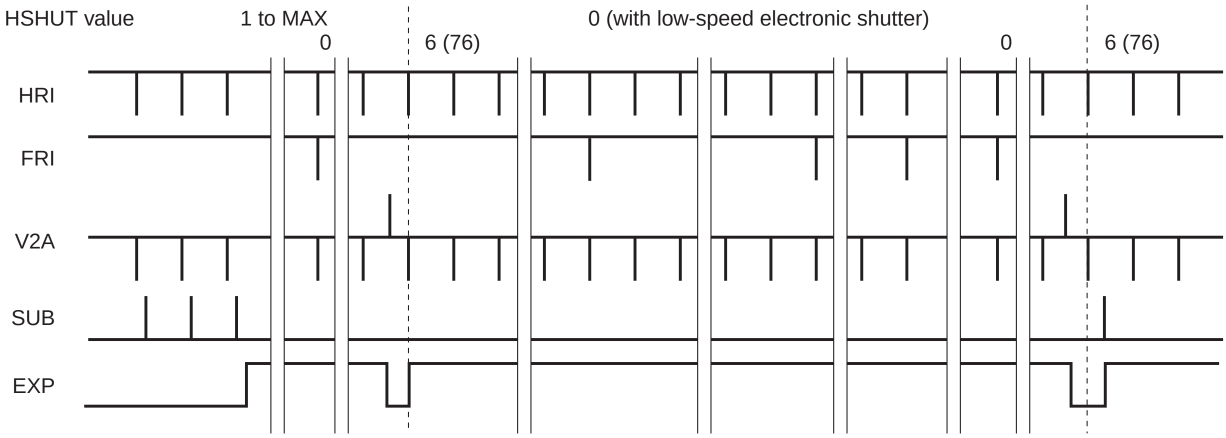
(4) 1 ≤ HSHUT < MAX (with low-speed electronic shutter)



(5) HSHUT = 0

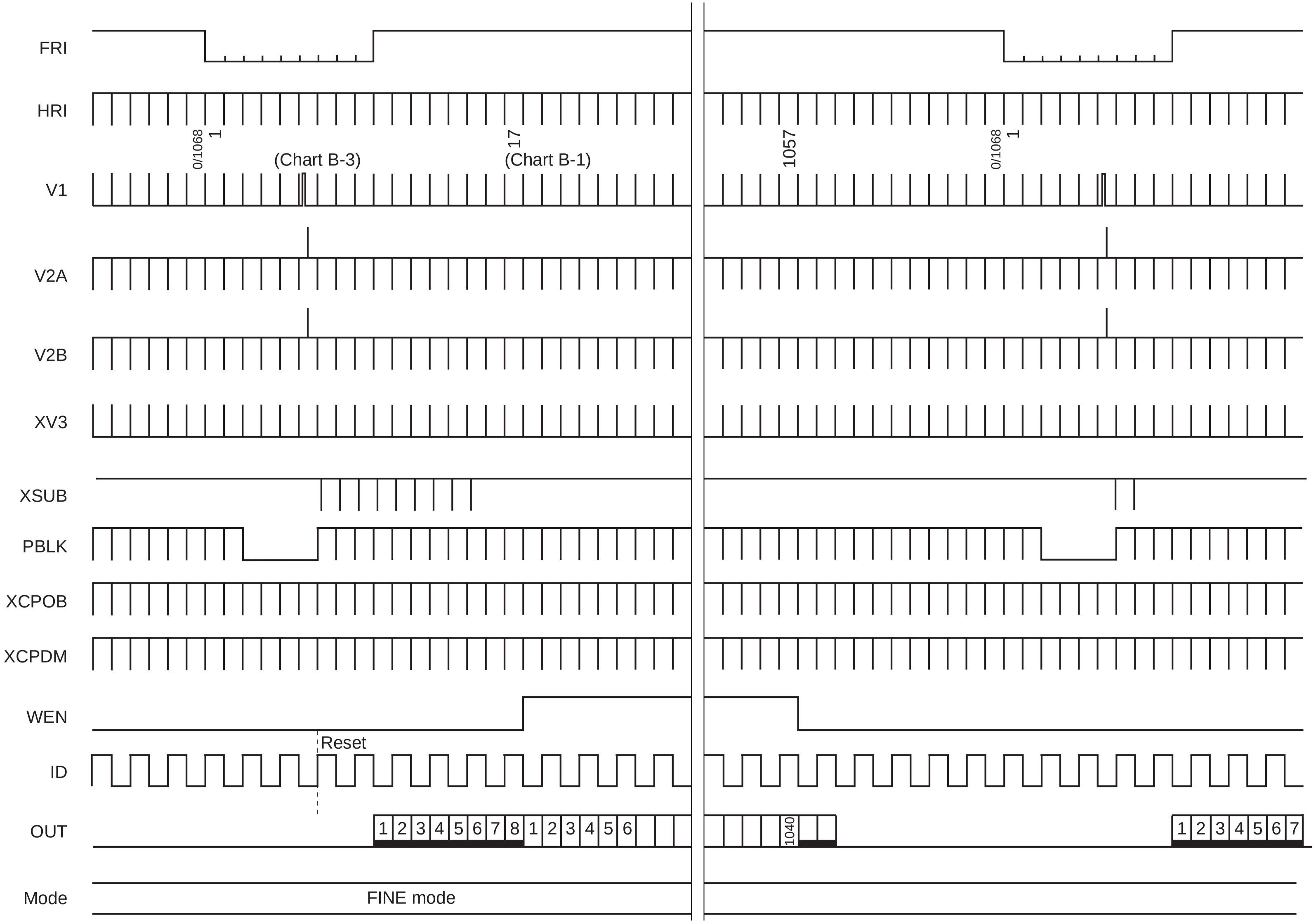


(6) HSHUT = 0 (with low-speed electronic shutter)

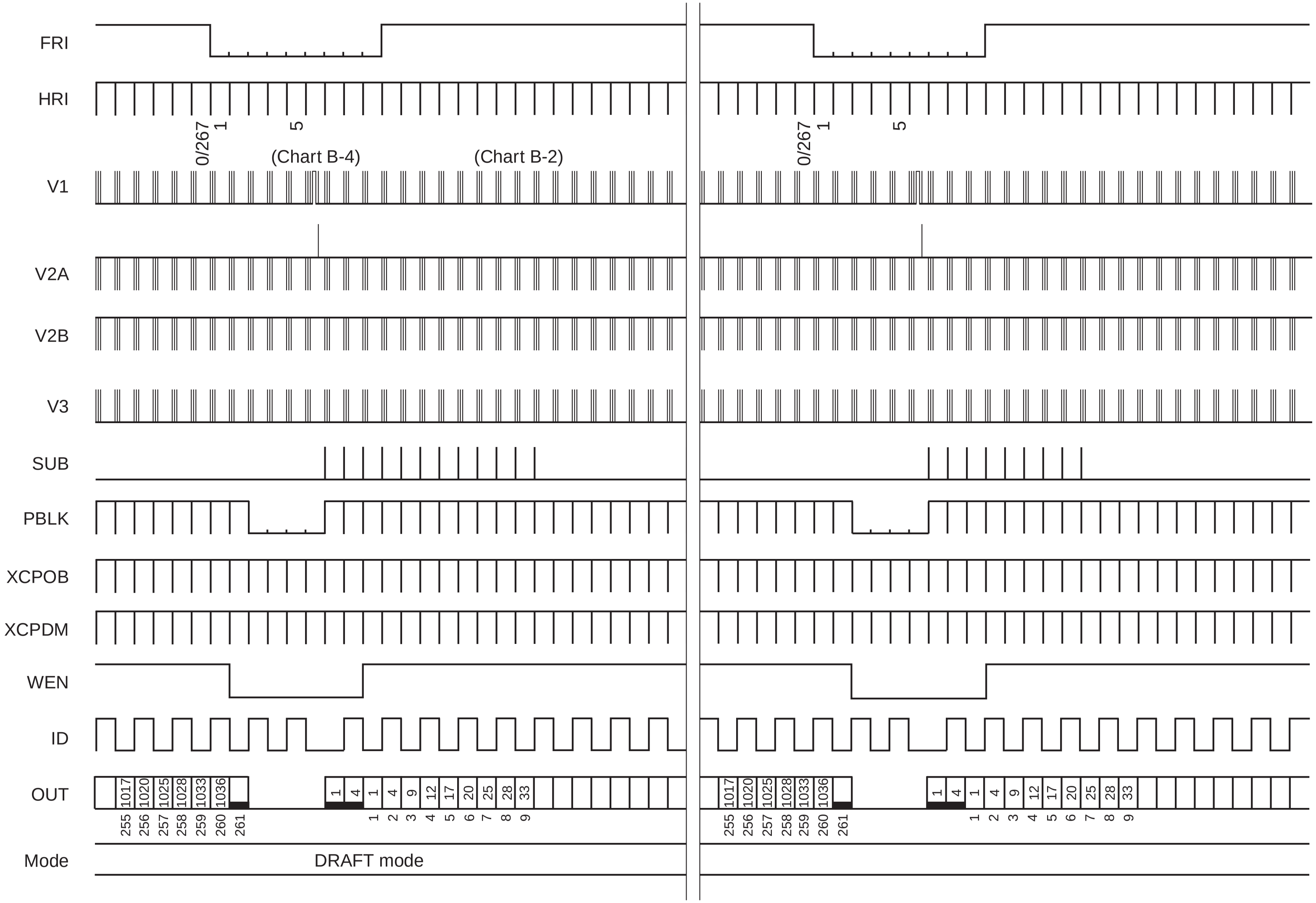


Numbers in parentheses are for FS mode.

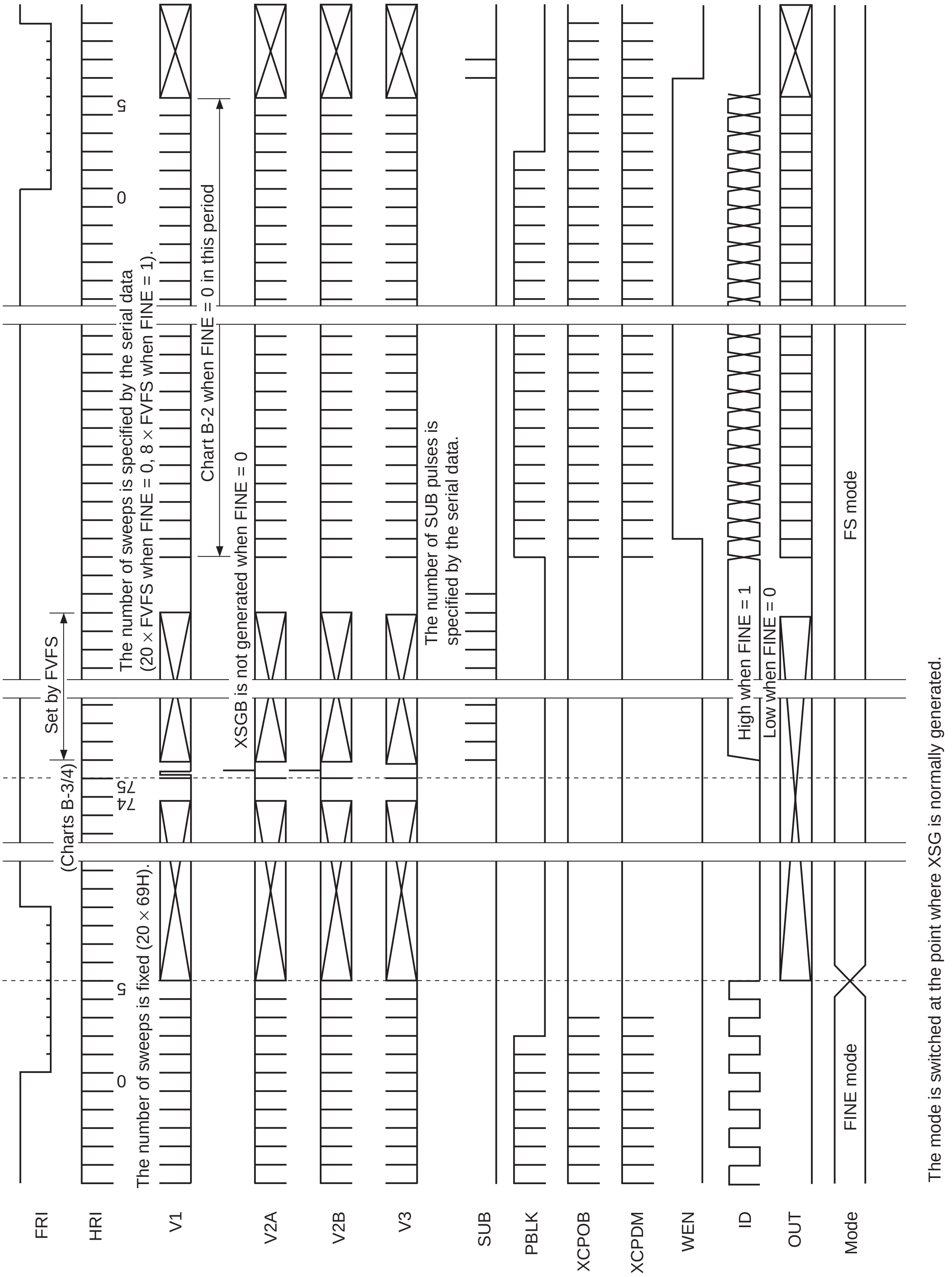
## Chart A-1. FINE Mode (Vertical synchronization)



### Chart A-2. DRAFT Mode (Vertical synchronization)



## Chart A-3. FS Mode (Vertical synchronization)



The number of sweeps is fixed (20 × 69H).

The number of sweeps is specified by the serial data (20 × FVFS when FINE = 0, 8 × FVFS when FINE = 1).

XSGB is not generated when FINE = 0

Chart B-2 when FINE = 0 in this period

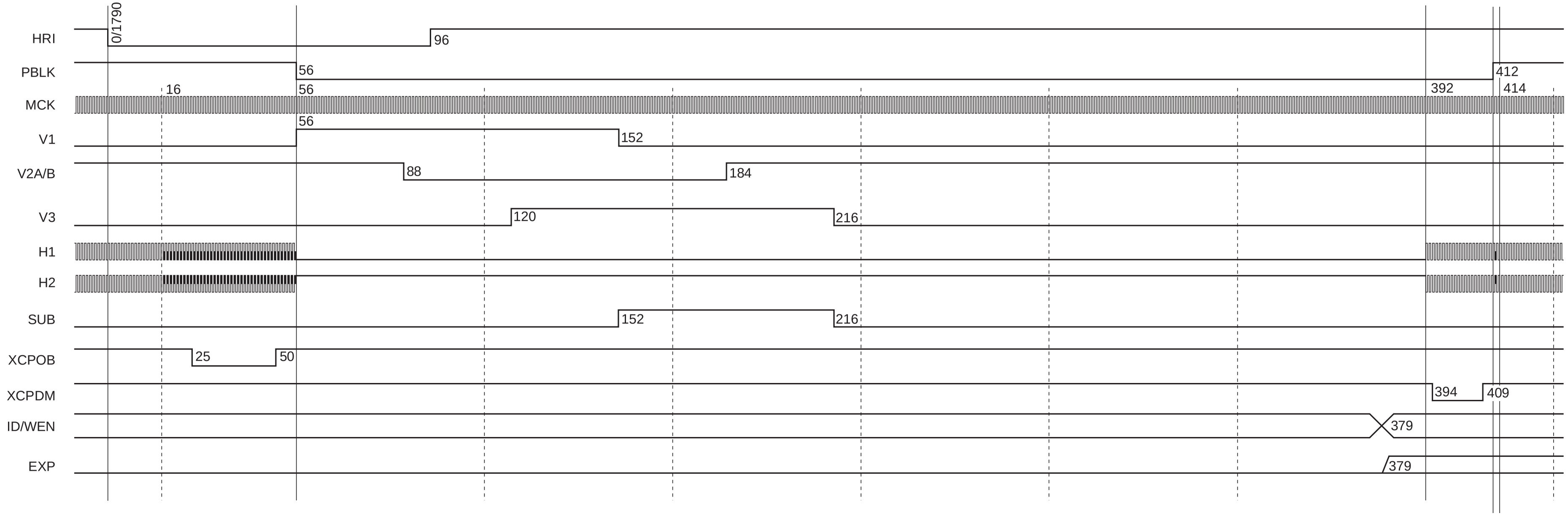
The number of SUB pulses is specified by the serial data.

High when FINE = 1

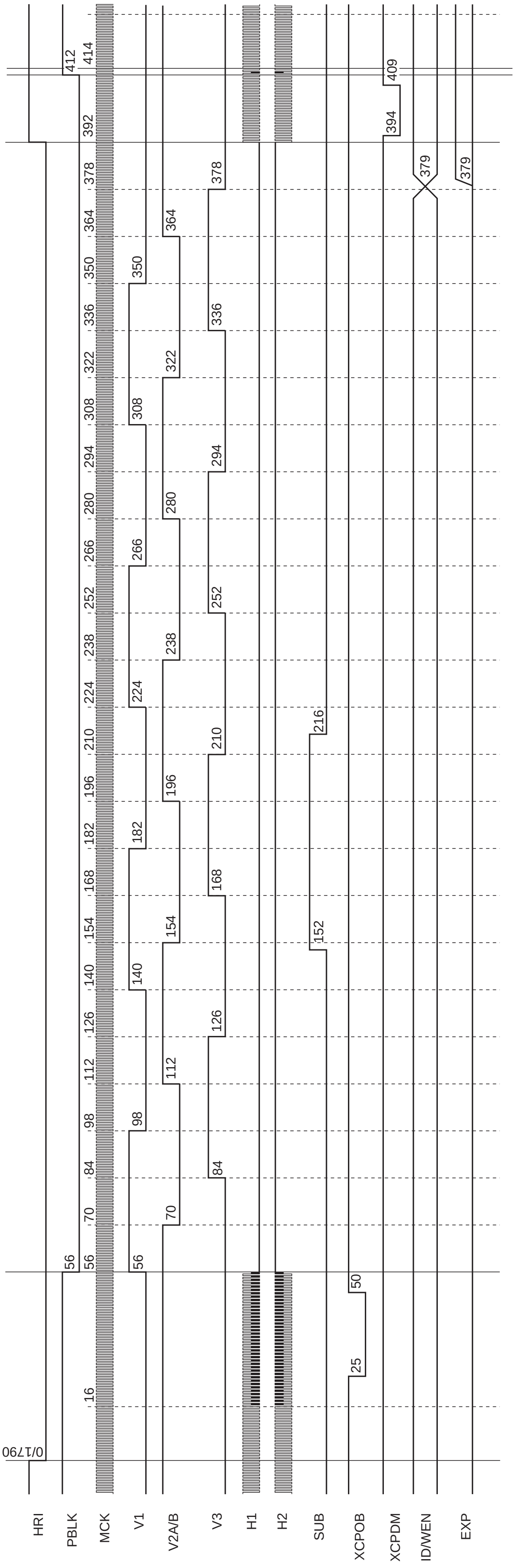
Low when FINE = 0

The mode is switched at the point where XSG is normally generated.

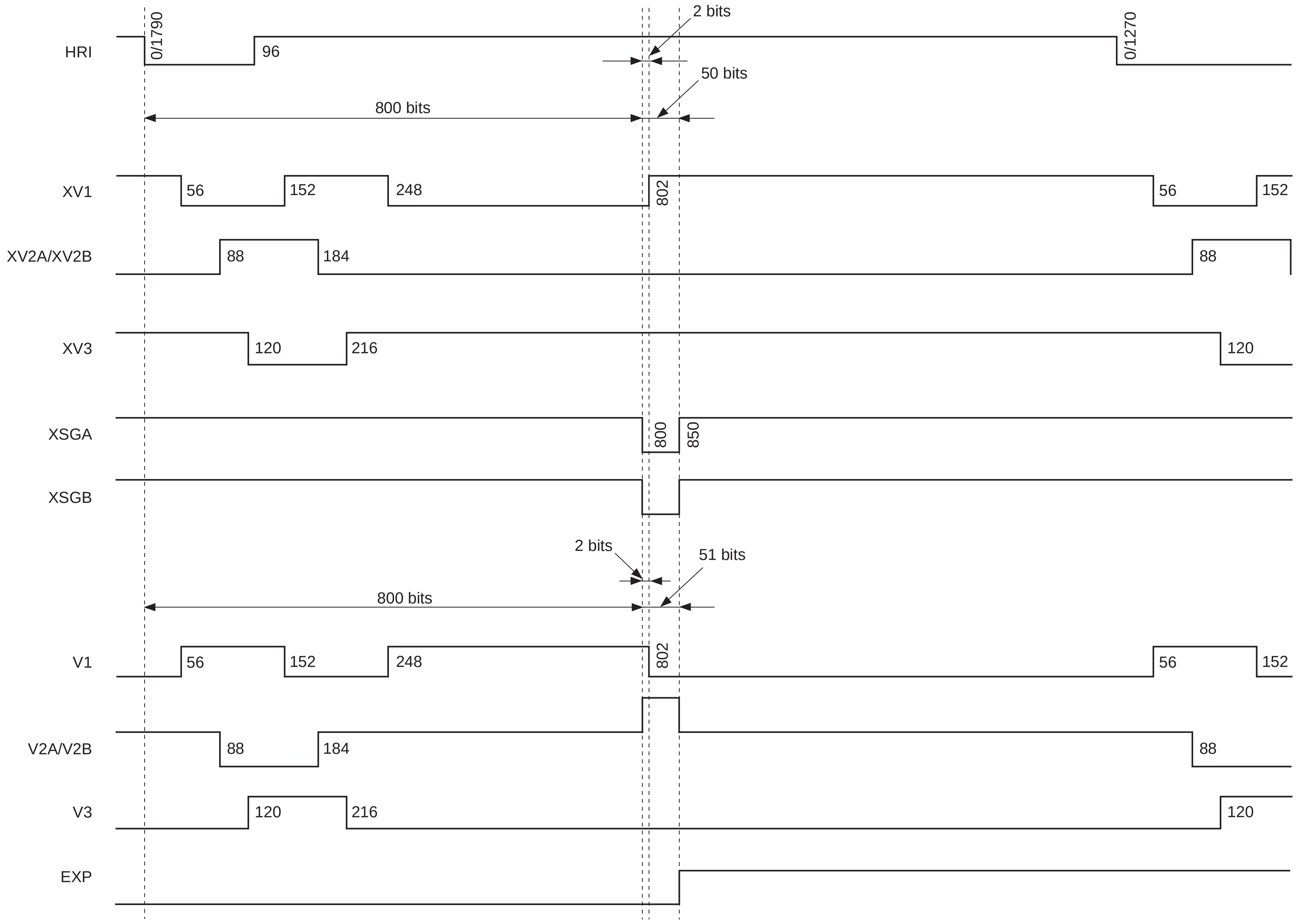
## Chart B-1. FINE Mode (Horizontal synchronization)



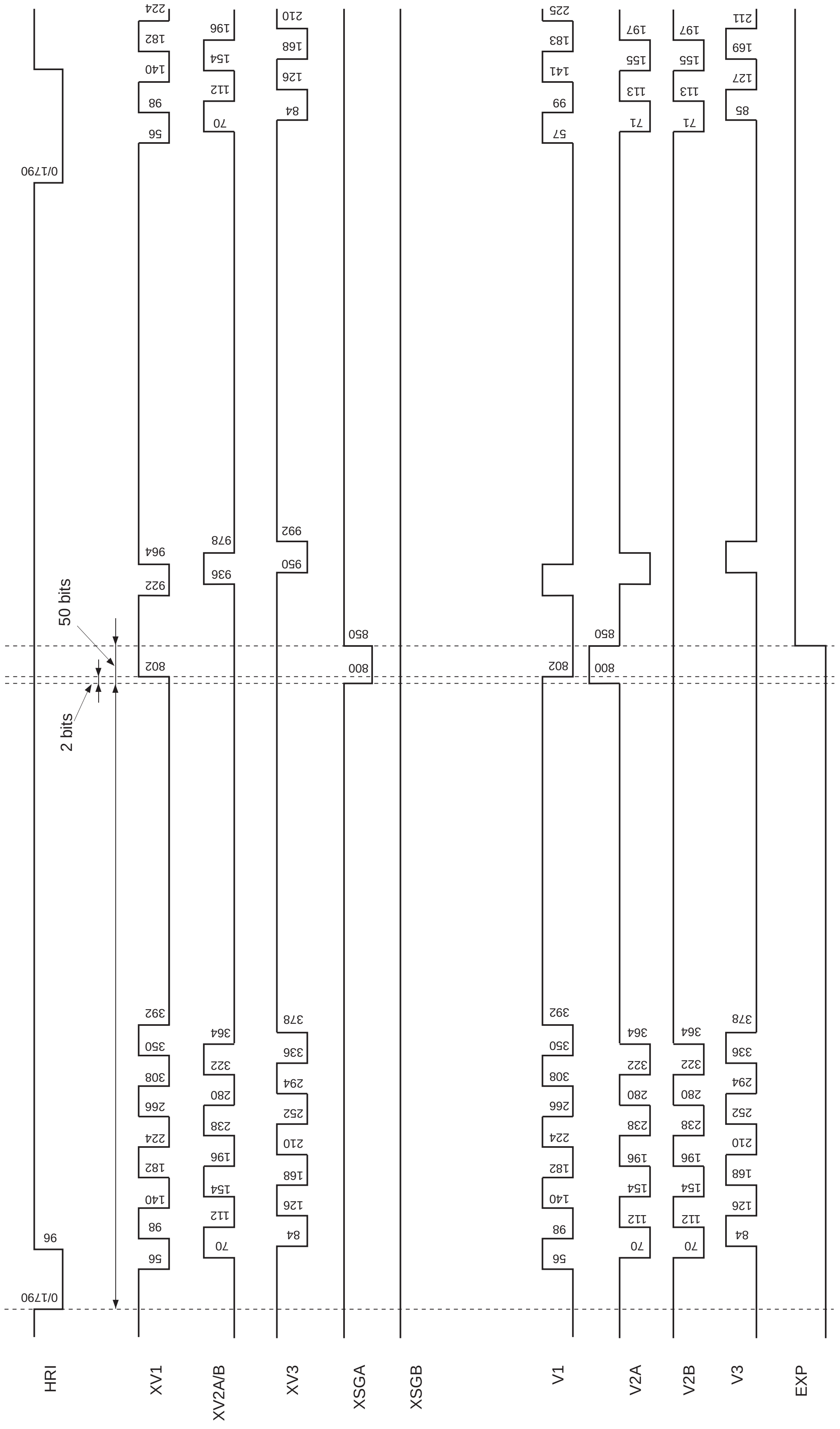
## Chart B-2. DRAFT Mode (Horizontal synchronization)



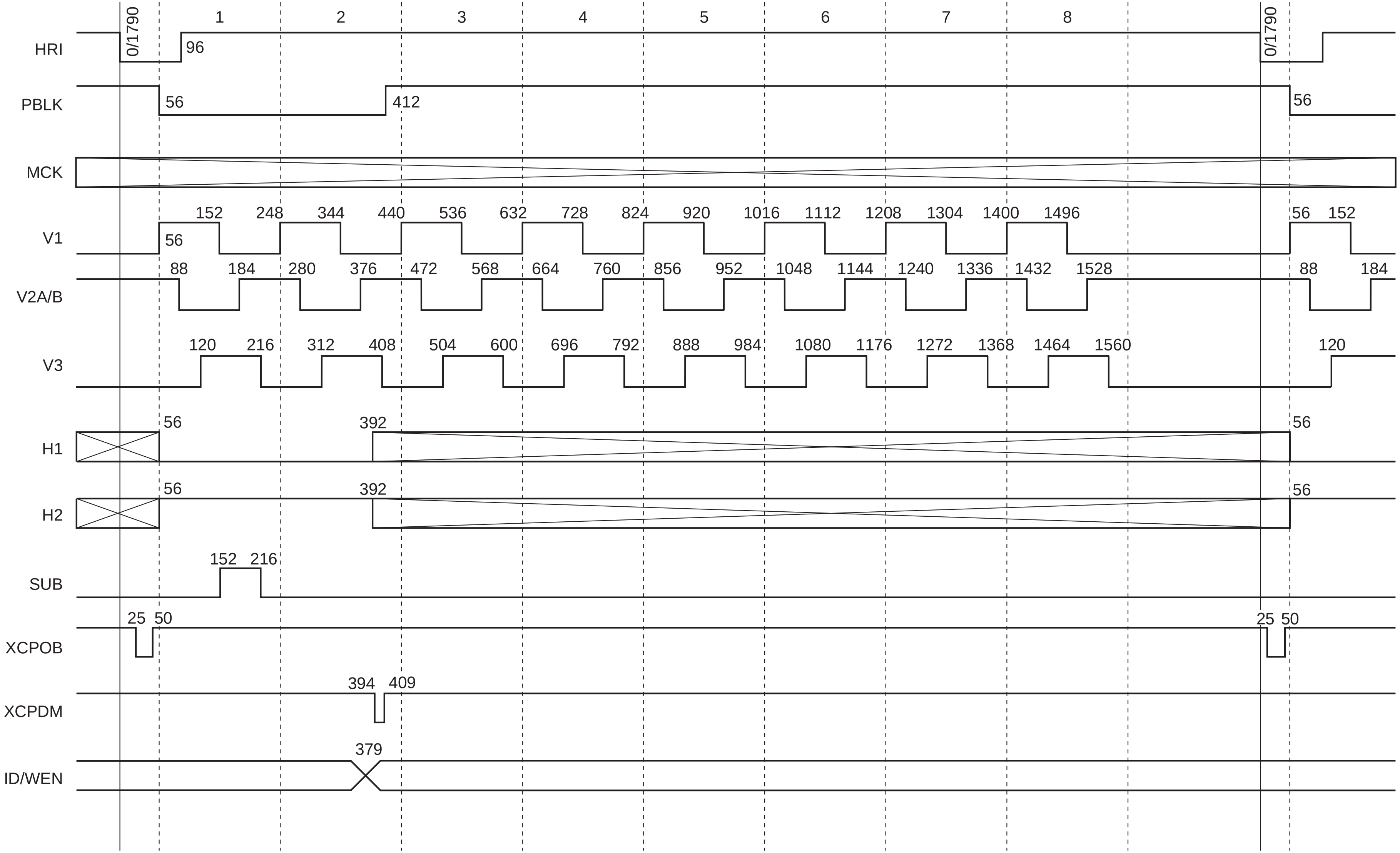
## Chart B-3. Readout Timing (FINE mode)



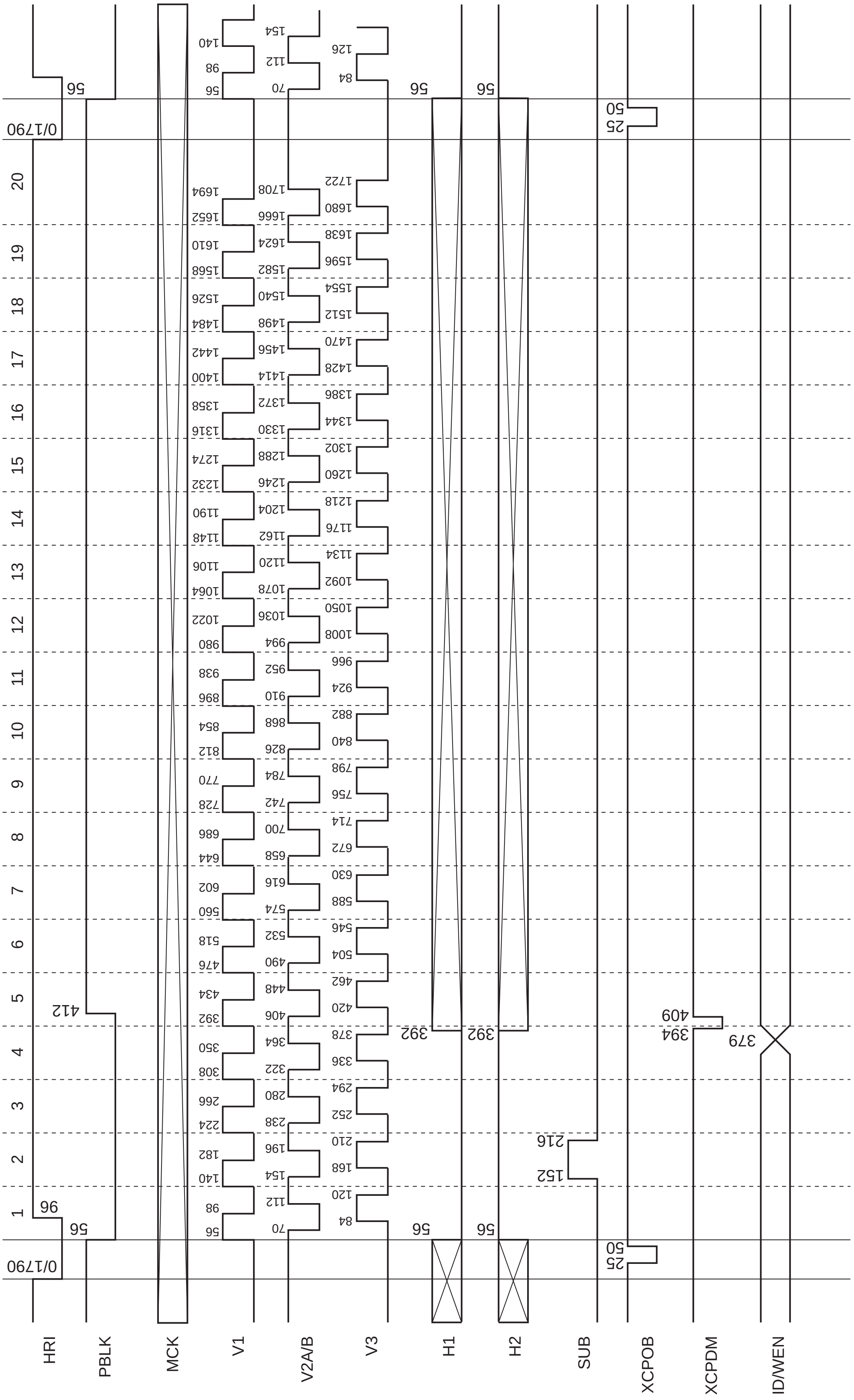
## Chart B-4. Readout Timing (DRAFT mode)



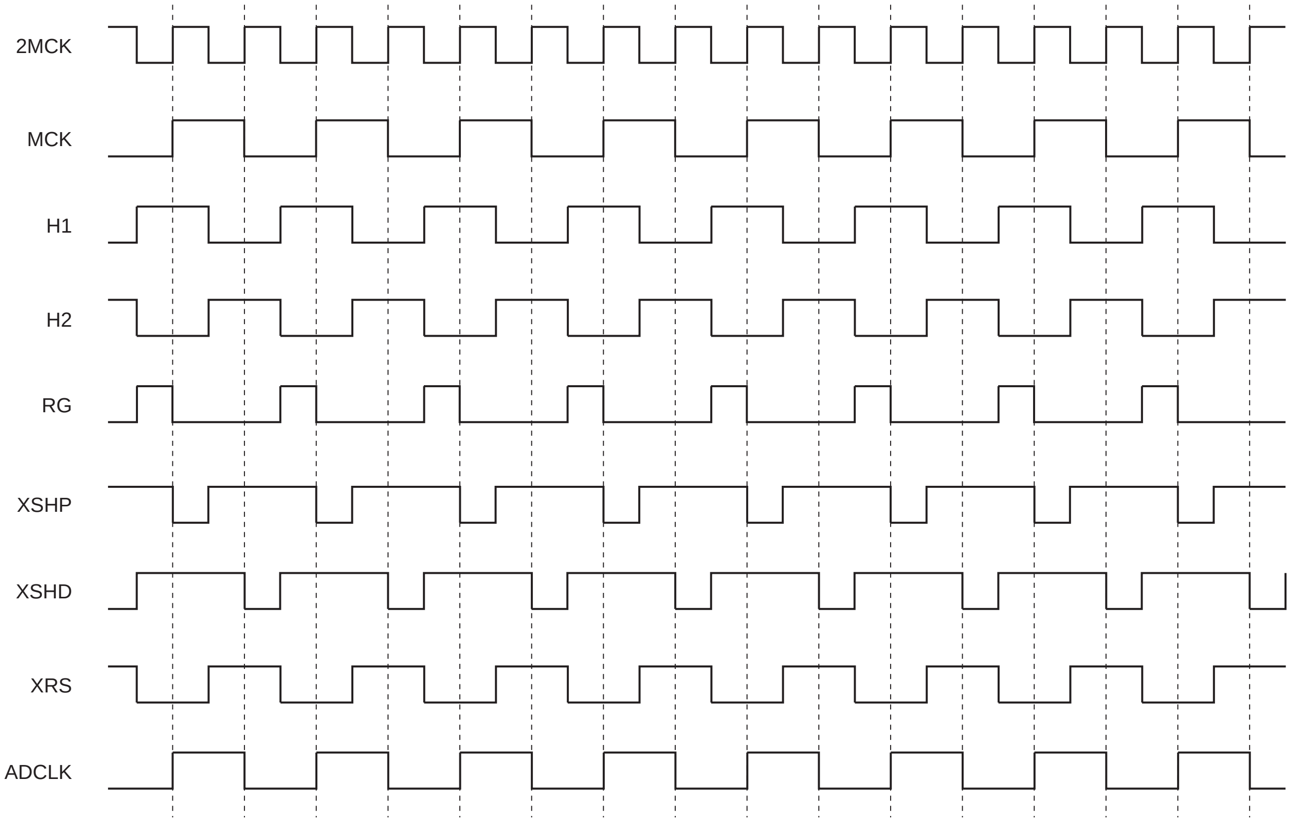
### Chart B-5. FS Mode: V clock continuous drive (FINE = 1)



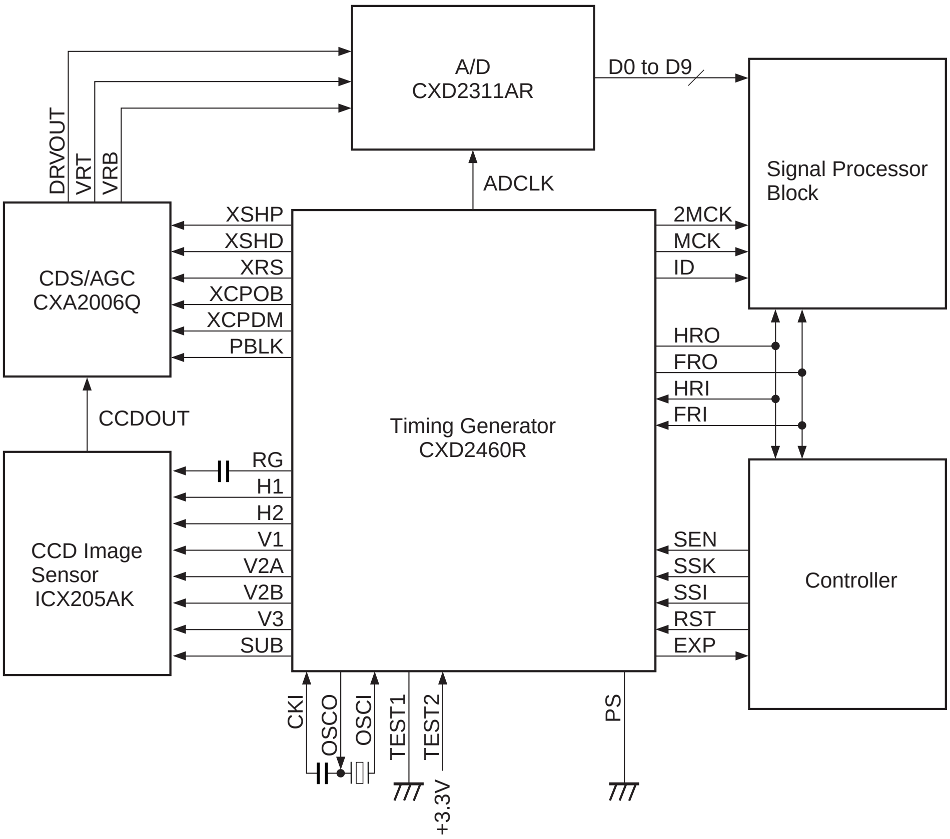
## Chart B-6. FS Mode: V clock continuous drive (FINE = 0)



## Logical Phase



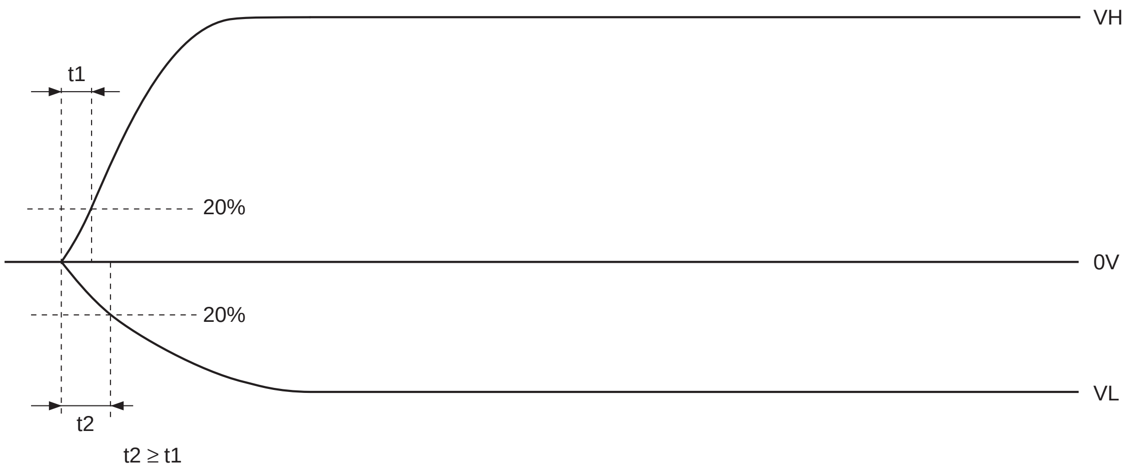
### Application Circuit



For making FR and HR outside the CXD2460R, configure a circuit that counts MCK. (Using 2MCK, CKO, etc. is not recommended.) Also, set system setting data, SGXEN (D12) to "1" and stop a built-in SSG.
Use crystal oscillator (fundamental wave) as base oscillation. Be sure to input duty 50% pulse when crystal oscillator is used.

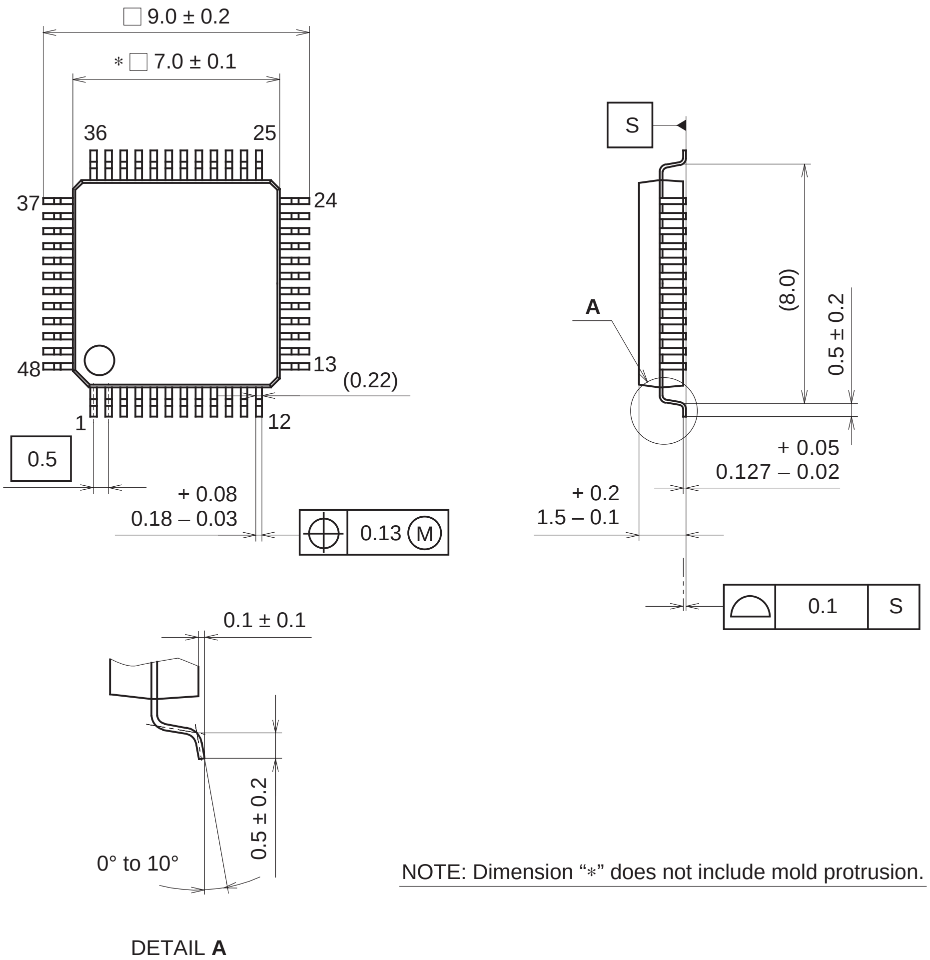
## Notes on Turning Power ON

To avoid setting VSUB pin of the CCD image sensor negative potential, the former two power supplies should be raised by the following order among three power supplies, VL and VH.



**Package Outline** Unit: mm

## 48PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

PACKAGE STRUCTURE

| | |
|---|---|
| SONY CODE | LQFP-48P-L01 |
| EIAJ CODE | LQFP048-P-0707 |
| JEDEC CODE | ———— |

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER/PALLADIUM PLATING |
| LEAD MATERIAL | 42/COPPER ALLOY |
| PACKAGE MASS | 0.2g |