SONY

CXD3205R

IEEE1394 LSI for D-STB, D-VHS, DTV

Description

The CXD3205R is an LSI integrating Link Layer and Physical Layer conforming to the IEEE1394-1995 serial bus standard on a single chip.

Link Layer provides MPEG2 transport stream dedicated input interface and output interface, IEC958 audio stream I/O interface and output interface for D/A converter as a data interface for isochronous communication. Also, a maximum 512 bytes of asynchronous communication is possible.

Physical Layer provides three ports for 1394 cable interface, and supports transfer speed of 200/100M bit/s. Also, this layer provides received packet data regeneration repeat function, arbitration function and bus initialization logic.

This IC utilizes Apple Computer's Fire Wire technology.

Features

- Conforms to IEEE1394-1995 serial bus standard.
- Supports 100Mbps/200Mbps.

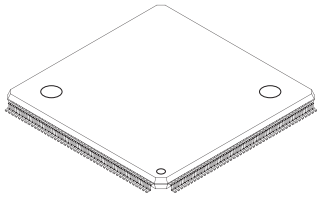
Link Layer

- Supports DVB transport streams.
- Supports IEC958 audio stream.
- Built-in PID filter function
- 2-channel isochronous simultaneous transmission/ synchronous transmission and reception
- Supports DMA (2 channels) transfer using host bus.
- Isochronous data inserted from asynchronous data port
- Built-in cipher circuit conforming to DTCP format
- Large capacity FIFO
  Isochronous Transmit/Receive FIFO: 960 × 32 bits × 2
  Asynchronous Transmit FIFO: 132 × 33 bits
  Asynchronous Receive FIFO: 133 × 33 bits
- CIP header automatic attachment/detection

Physical Layer

- Live wire detection function when port is connected to operation node
- Resynchronization for reception data local clock
- DS link encode/decode
- 196.603MHz PLL
- Supports of power class definition pin.
- Independent 3-port TpBias

176 pin LQFP (Plastic)



Applications

Digital interface for D-STB, D-VHS and DTV

Absolute Maximum Ratings

• Supply voltage	V_{DD}	Vss – 0.5 to +4.6	V
• Input voltage	V_I	Vss – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	Vss – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

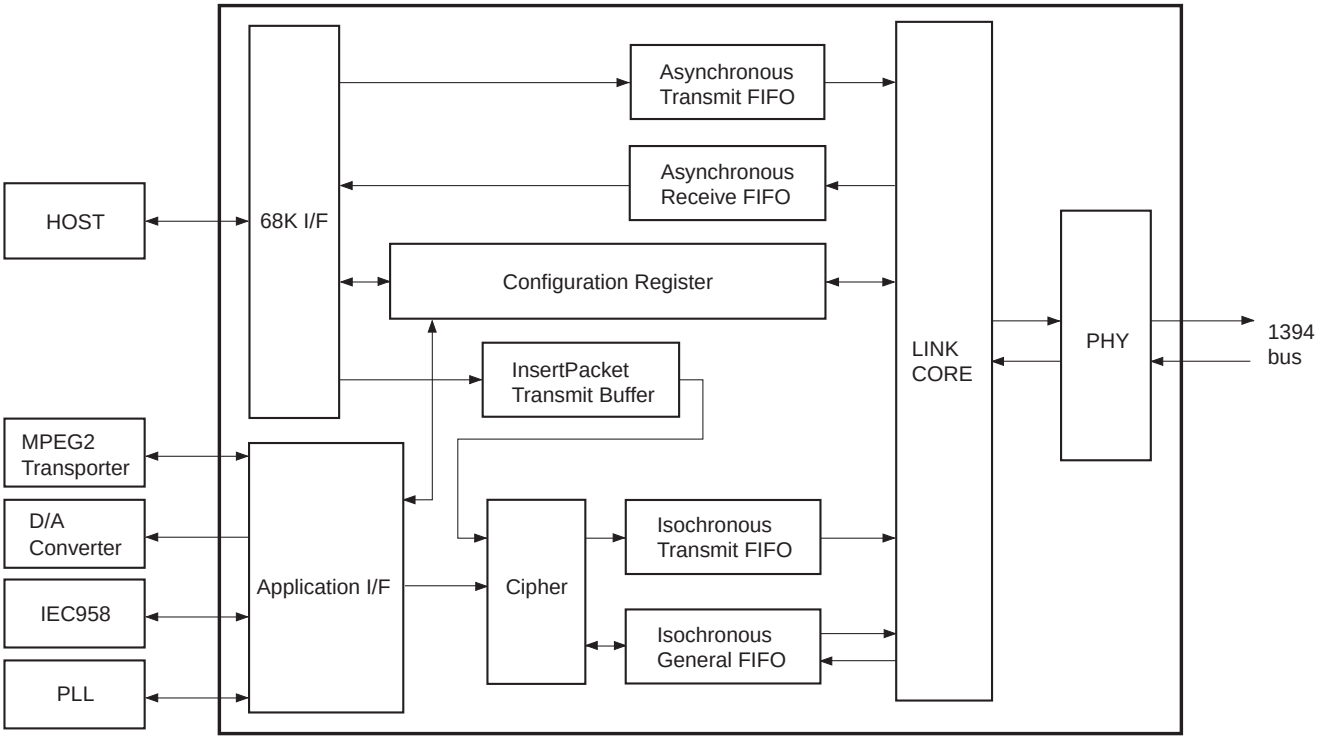
Recommended Operating Conditions

• Supply voltage	V_{DD}	3.0 to 3.6	V
• Operating temperature	Topr	–20 to +75	°C

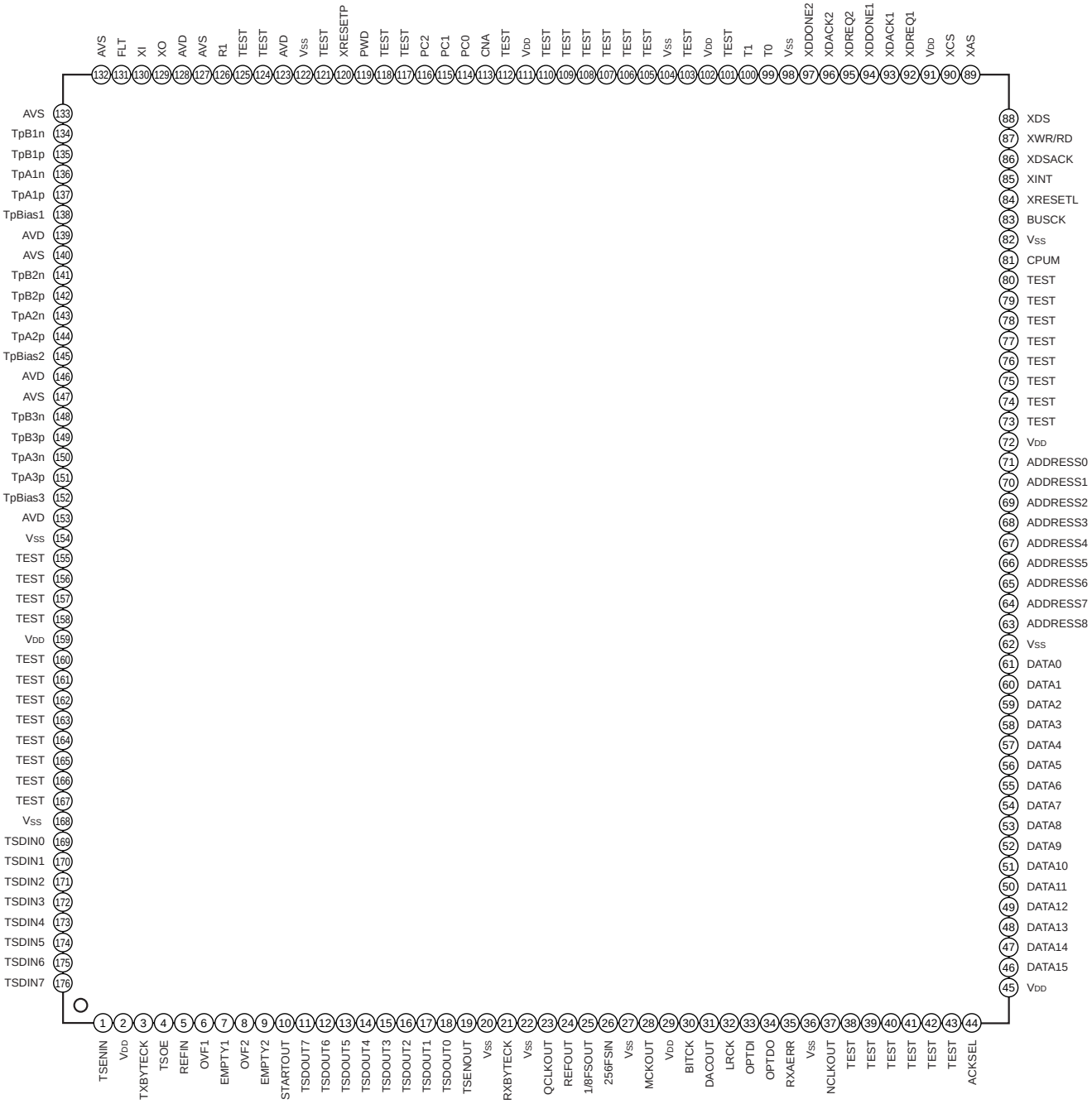
Fire Wire is a registered trademark of Apple Computer, Inc., USA.

E99745-PS

1. Block Diagram



2. Pin Configuration



3. Pin Description

Pin No.	Symbol	I/O	Description
1	TSENIN	I	Transport stream packet enable input. 0: non-active; 1: active. When not used, terminate to GND.
2	V_{DD}	—	Power supply
3	TXBYTECK	I	Transport stream packet transmit byte clock. Frequency specification 7.5MHz (Max.) – 200kHz (Min.) Stop is prohibited when the input signal is high level. When not used, terminate to GND.
4	TSOE	I (with pull-up)	Transport stream output enable control signal. 1: STARTOUT, TSENOUT, TSDOUT is Hi-Z. 0: STARTOUT, TSENOUT, TSDOUT is output mode.
5	REFIN	I	Isochronous transmit SyncTime reference signal. When not used, terminate to GND.
6	OVF1	O	Internal isochronous FIFO1 overflow status signal. 0: not overflow; 1: overflow
7	EMPTY1	O	Internal isochronous FIFO1 empty status signal. 0: not empty; 1: empty
8	OVF2	O	Internal isochronous FIFO2 overflow status signal. 0: not overflow; 1: overflow
9	EMPTY2	O	Internal isochronous FIFO2 empty status signal. 0: not empty; 1: empty
10	STARTOUT	O	Transport stream data output start byte signal. 0: not start byte; 1: start byte
11	TSDOUT7	O	Transport stream data output bit 7
12	TSDOUT6	O	Transport stream data output bit 6
13	TSDOUT5	O	Transport stream data output bit 5
14	TSDOUT4	O	Transport stream data output bit 4
15	TSDOUT3	O	Transport stream data output bit 3
16	TSDOUT2	O	Transport stream data output bit 2
17	TSDOUT1	O	Transport stream data output bit 1
18	TSDOUT0	O	Transport stream data output bit 0
19	TSENOUT	O	Transport stream packet enable output
20	V_{SS}	—	GND
21	RXBYTECK	I	Transport stream packet receive byte clock. Frequency specification 7.5MHz (Max.) – 200kHz (Min.) Stop is prohibited when the input signal is high level. When not used, terminate to GND.
22	V_{SS}	—	GND
23	QCLKOUT	O	6.144MHz clock output
24	REFOUT	O	Isochronous receive SyncTime reference signal
25	1/8FSOUT	O	Isochronous receive 1/8 frequency divided fs output for audio PLL

Pin No.	Symbol	I/O	Description
26	256FSIN	I	Isochronous receive ×256 fs input for audio PLL. When not used, terminate to GND.
27	V_{SS}	—	GND
28	MCKOUT	O	Isochronous receive DAC master clock output for audio (256fs output)
29	V_{DD}	—	Power supply
30	BITCK	O	Isochronous receive DAC bit clock output for audio (64fs output)
31	DACOUT	O	Isochronous receive DAC data output for audio
32	LRCK	O	Isochronous receive DAC LR clock output for audio
33	OPTDI	I	Isochronous transmit IEC958 data input. When not used, terminate to GND.
34	OPTDO	O	Isochronous receive IEC958 data output
35	RXAERR	O	Isochronous receive audio error output
36	V_{SS}	—	GND
37	NCLKOUT	O	24.576MHz clock output
38	TEST	—	Test pin*1
39	TEST	—	Test pin*1
40	TEST	—	Test pin*1
41	TEST	—	Test pin*1
42	TEST	—	Test pin*1
43	TEST	—	Test pin*1
44	ACKSEL	I (with pull-down)	Positive/negative logic selecting signal at XDSACK output 0: negative logic; 1: positive logic
45	V_{DD}	—	Power supply
46	DATA15	I/O	Host I/F I/O data bit 15
47	DATA14	I/O	Host I/F I/O data bit 14
48	DATA13	I/O	Host I/F I/O data bit 13
49	DATA12	I/O	Host I/F I/O data bit 12
50	DATA11	I/O	Host I/F I/O data bit 11
51	DATA10	I/O	Host I/F I/O data bit 10
52	DATA9	I/O	Host I/F I/O data bit 9
53	DATA8	I/O	Host I/F I/O data bit 8. Common with address input bit 8 when ADDRESS/DATA superimposed CPU is used (CPUM = 1).
54	DATA7	I/O	Host I/F I/O data bit 7. Common with address input bit 7 when ADDRESS/DATA superimposed CPU is used (CPUM = 1).

*1 The test pins should be used with open.

Pin No.	Symbol	I/O	Description
55	DATA6	I/O	Host I/F I/O data bit 6. Common with address input bit 6 when ADDRESS/DATA superimposed CPU is used (CPUM = 1).
56	DATA5	I/O	Host I/F I/O data bit 5. Common with address input bit 5 when ADDRESS/DATA superimposed CPU is used (CPUM = 1).
57	DATA4	I/O	Host I/F I/O data bit 4. Common with address input bit 4 when ADDRESS/DATA superimposed CPU is used (CPUM = 1).
58	DATA3	I/O	Host I/F I/O data bit 3. Common with address input bit 3 when ADDRESS/DATA superimposed CPU is used (CPUM = 1).
59	DATA2	I/O	Host I/F I/O data bit 2. Common with address input bit 2 when ADDRESS/DATA superimposed CPU is used (CPUM = 1).
60	DATA1	I/O	Host I/F I/O data bit 1. Common with address input bit 1 when ADDRESS/DATA superimposed CPU is used (CPUM = 1).
61	DATA0	I/O	Host I/F I/O data bit 0. Common with address input bit 0 when ADDRESS/DATA superimposed CPU is used (CPUM = 1).
62	V_{SS}	—	GND
63	ADDRESS8	I (with pull-down)	Host I/F address input bit 8. Not used when ADDRESS/DATA superimposed CPU is used (CPUM = 0).
64	ADDRESS7	I (with pull-down)	Host I/F address input bit 7. Not used when ADDRESS/DATA superimposed CPU is used (CPUM = 0).
65	ADDRESS6	I (with pull-down)	Host I/F address input bit 6. Not used when ADDRESS/DATA superimposed CPU is used (CPUM = 0).
66	ADDRESS5	I (with pull-down)	Host I/F address input bit 5. Not used when ADDRESS/DATA superimposed CPU is used (CPUM = 0).
67	ADDRESS4	I (with pull-down)	Host I/F address input bit 4. Not used when ADDRESS/DATA superimposed CPU is used (CPUM = 0).
68	ADDRESS3	I (with pull-down)	Host I/F address input bit 3. Not used when ADDRESS/DATA superimposed CPU is used (CPUM = 0).
69	ADDRESS2	I (with pull-down)	Host I/F address input bit 2. Not used when ADDRESS/DATA superimposed CPU is used (CPUM = 0).

*1 The test pins should be used with open.

Pin No.	Symbol	I/O	Description
70	ADDRESS1	I (with pull-down)	Host I/F address input bit 1. Not used when ADDRESS/DATA superimposed CPU is used (CPUM = 0).
71	ADDRESS0	I (with pull-down)	Host I/F address input bit 0. Not used when ADDRESS/DATA superimposed CPU is used (CPUM = 0).
72	V_{DD}	—	Power supply
73	TEST	—	Test pin*1
74	TEST	—	Test pin*1
75	TEST	—	Test pin*1
76	TEST	—	Test pin*1
77	TEST	—	Test pin*1
78	TEST	—	Test pin*1
79	TEST	—	Test pin*1
80	TEST	—	Test pin*1
81	CPUM	I (with pull-down)	Host I/F CPU mode select input 0: ADDRESS/DATA non-superimposed; 1: ADDRESS/DATA superimposed
82	V_{SS}	—	GND
83	BUSCK	I	Host I/F bus clock input. Frequency specification 27MHz (Max.) – 200kHz (Min.) Stop is prohibited when the input signal is high level.
84	XRESETL	I	Link Layer master reset input 0: active; 1: non-active
85	XINT	O	Host I/F interrupt signal 0: active; 1: non-active
86	XDSACK	O	Host I/F data acknowledge signal
87	XWR/RD	I	Host I/F write/read signal. Write EN signal when ADDRESS/DATA superimposed CPU is used (CPUM = 1).
88	XDS	I	Host I/F data strobe signal. Read EN signal when ADDRESS/DATA superimposed CPU is used (CPUM = 1).
89	XAS	I	Host I/F address strobe signal
90	XCS	I	Host I/F chip select signal 0: active; 1: non-active
91	V_{DD}	—	Power supply
92	XDREQ1	O	Asynchronous packet transmit DMA request signal 0: active; 1: non-active
93	XDACK1	I (with pull-up)	Asynchronous packet transmit DMA acknowledge signal 0: active; 1: non-active
94	XDDONE1	O	Asynchronous packet transmit DMA complete signal 0: active; 1: non-active
95	XDREQ2	O	Isochronous packet receive DMA request signal 0: active; 1: non-active

*1 The test pins should be used with open. However, connect to GND for Pin 74.

Pin No.	Symbol	I/O	Description
96	XDACK2	I (with pull-up)	Isochronous packet receive DMA acknowledge signal 0: active; 1: non-active
97	XDDONE2	O	Isochronous packet receive DMA complete signal 0: active; 1: non-active
98	V_{SS}	—	GND
99	T0	—	Test pin*1
100	T1	—	Test pin*1
101	TEST	—	Test pin*1
102	V_{DD}	—	Power supply
103	TEST	—	Test pin*1
104	V_{SS}	—	GND
105	TEST	—	Test pin*1
106	TEST	—	Test pin*1
107	TEST	—	Test pin*1
108	TEST	—	Test pin*1
109	TEST	—	Test pin*1
110	TEST	—	Test pin*1
111	V_{DD}	—	Power supply
112	TEST	—	Test pin*1
113	CNA	O	Cable connection information output 0: during no-connection; 1: during connection
114	PC0	I (with pull-down)	Power class bit 0
115	PC1	I (with pull-down)	Power class bit 1
116	PC2	I (with pull-down)	Power class bit 2
117	TEST	—	Test pin*1
118	TEST	—	Test pin*1
119	PWD	I	Power-down signal input 0: non-active; 1: active
120	XRESETP	I	Physical Layer master reset 0: active; 1: non-active
121	TEST	—	Test pin*1
122	V_{SS}	—	GND
123	AVD	—	Analog power supply

*1 The test pins should be used with open. However, connect Pin 121 to GND.

Pin No.	Symbol	I/O	Description
124	TEST	—	Test pin*1
125	TEST	—	Test pin*1
126	R1	O	Reference current setting pin
127	AVS	—	Analog GND
128	AVD	—	Analog power supply
129	XO	O	PLL output
130	XI	I	PLL input
131	FLT	I	Loop filter pin
132	AVS	—	Analog GND
133	AVS	—	Analog GND
134	TpB1n	I/O	Cable port B1 negative signal
135	TpB1p	I/O	Cable port B1 positive signal
136	TpA1n	I/O	Cable port A1 negative signal
137	TpA1p	I/O	Cable port A1 positive signal
138	TpBias1	O	Cable port 1 reference signal
139	AVD	—	Analog power supply
140	AVS	—	Analog GND
141	TpB2n	I/O	Cable port B2 negative signal
142	TpB2p	I/O	Cable port B2 positive signal
143	TpA2n	I/O	Cable port A2 negative signal
144	TpA2p	I/O	Cable port A2 positive signal
145	TpBias2	O	Cable port 2 reference signal
146	AVD	—	Analog power supply
147	AVS	—	Analog GND
148	TpB3n	I/O	Cable port B3 negative signal
149	TpB3p	I/O	Cable port B3 positive signal
150	TpA3n	I/O	Cable port A3 negative signal
151	TpA3p	I/O	Cable port A3 positive signal
152	TpBias3	O	Cable port 3 reference signal
153	AVD	—	Analog power supply
154	V_{SS}	—	GND
155	TEST	—	Test pin*1
156	TEST	—	Test pin*1
157	TEST	—	Test pin*1

*1 The test pins should be used with open. However, connect Pin 124 to analog power supply, and connect Pin 125 to GND.

Pin No.	Symbol	I/O	Description
158	TEST	—	Test pin*1
159	V_{DD}	—	Power supply
160	TEST	—	Test pin*1
161	TEST	—	Test pin*1
162	TEST	—	Test pin*1
163	TEST	—	Test pin*1
164	TEST	—	Test pin*1
165	TEST	—	Test pin*1
166	TEST	—	Test pin*1
167	TEST	—	Test pin*1
168	V_{SS}	—	GND
169	TSDIN0	I	Transport stream data input bit 0
170	TSDIN1	I	Transport stream data input bit 1
171	TSDIN2	I	Transport stream data input bit 2
172	TSDIN3	I	Transport stream data input bit 3
173	TSDIN4	I	Transport stream data input bit 4
174	TSDIN5	I	Transport stream data input bit 5
175	TSDIN6	I	Transport stream data input bit 6
176	TSDIN7	I	Transport stream data input bit 7

*1 The test pins should be used with open. However, connect Pin 158 to V_{DD}.

4. Electrical Characteristics

4-1. Link

4-1-1. DC Characteristics

(Ta = 25°C, Vss = 0V)

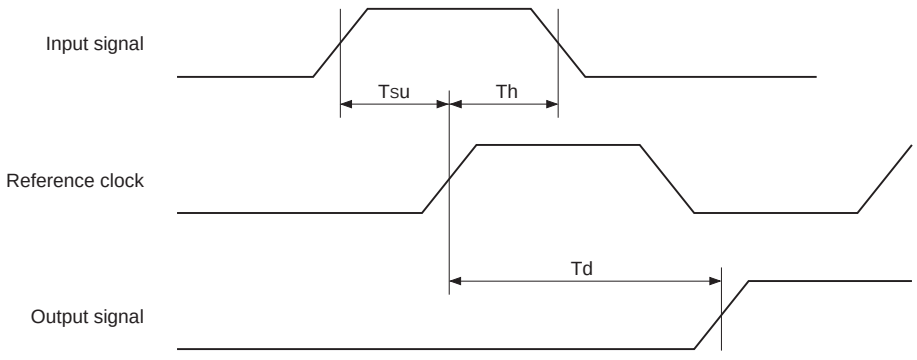
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}	CMOS input cell	0.7V_{DD}			V
Input voltage	V_{IL}	CMOS input cell			0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH} = –4.0mA	V_{DD} – 0.4			V
Output voltage	V_{OL}	I_{OL} = 4.0mA				V
Input leak current	I_{I1}	Bidirectional pin (input state)	–40			µA
Input leak current	I_{I2}	Normal input pin	–10			µA
Output leak current	I_{OZ}	Tri-state pin (for high impedance state) V_{IN} = V_{SS} or V_{DD}	–40			µA

4-1-2. AC Characteristics

(V_{DD} = 3.0 to 3.6V)

Item	Applicable pins	Symbol	Reference clock	Conditions	Min.	Typ.	Max.	Unit
Input setup	TSDIN[7:0], TSENIN	Tsu1	TXBYTECK	CL = 10pF	10			ns
Input hold		Th1			5			ns
Output delay	TSOUT[7:0], TSENOUT, STARTOUT	Td1	RXBYTECK		5		20	ns
Input setup	ADDRESS[8:0], XAS, DATA[15:0], XDS, XCS, XWR	Tsu2	ATF/CFR/IPF write timing and ARF/CFR read timing.					
Input hold		Th2						
Output delay	DATA[15:0], XDSACK	Td2						
Input setup	DATA[15:0], XDACK1, XDACK2	Tsu3	DMA write timing and DMA read timing.					
Input hold		Th3						
Output delay	DATA[15:0], XDREQ1, XDREQ2, XDDONE1, XDDONE2	Td3						

Timing Definition



4-2. PHY

Electrical Characteristics under the Recommended Operating Conditions (unless otherwise specified)

4-2-1. DC Characteristics

(V_{SS} = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		V_{DD} – 1.0			V
Low level input voltage	V_{IL}				1.0	V
High level input current	I_{IH}	$V_{IH} = V_{DD}$	–10			µA
Low level input current	I_{IL}	$V_{IL} = V_{SS}$			10.0	µA
High level output voltage	V_{OH}	I_{OH} = –6mA	V_{DD} – 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 6mA			0.5	V

4-2-2. AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Differential output amplitude	V_{OD}	Load 55Ω	175		265	mV
TpBias output voltage	V_{TPBIAS}	Source 3mA, Sync 1.3mA	1.72		1.92	V
Tp common mode current	I_{CM}	Driver disabled (Z state) Drivers other than the speed signal enabled	–25		5	µA
			–0.18		0.18	mA
TpB200Mbit speed signal	I_{SPD}		2.76		4.6	mA
Differential input impedance	Z_{DIFFZ}	Driver disabled (Z state)	21.0			kΩ
					6.9	pF
Differential input impedance	Z_{DIFFEN}	Driver enabled	3.4			kΩ
					6.9	pF
Common mode input capacitance	C_{CM}	Tp pins shorted Z state drivers			27.6	pF
Inactive line threshold voltage	V_T $_{NOCONN}$	TPB common mode voltage	0.64		0.96	V
CPS threshold voltage	V_T $_{CPWD}$	Vp pins (R = 220kΩ)	6.0		7.6	V

4-2-3. Interface Characteristics

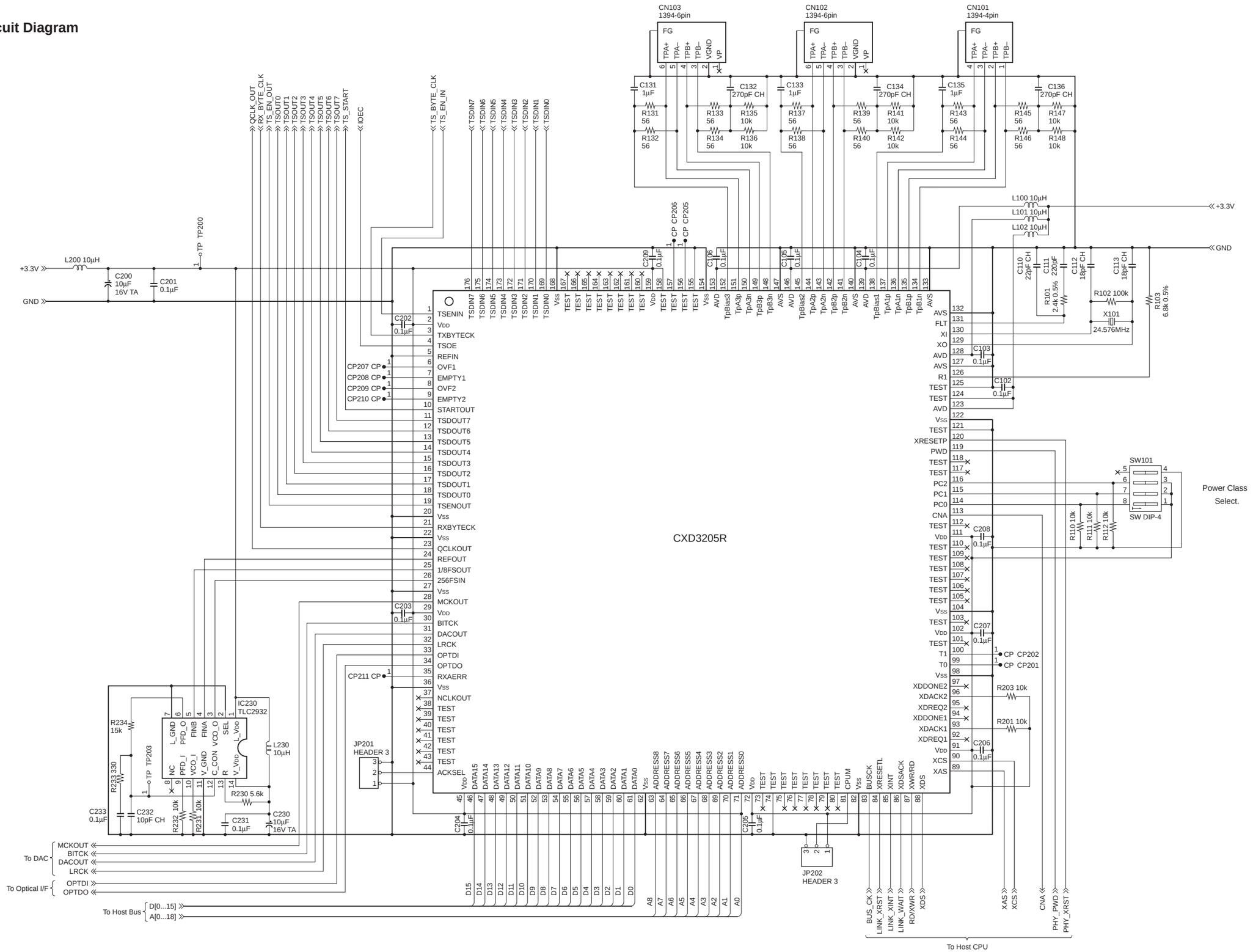
Link Interface

Item	Symbol	DC connection			Unit
		Min.	Typ.	Max.	
Link-On cycle time	T_{LINKON}	160			ns

Twisted Pair Interface

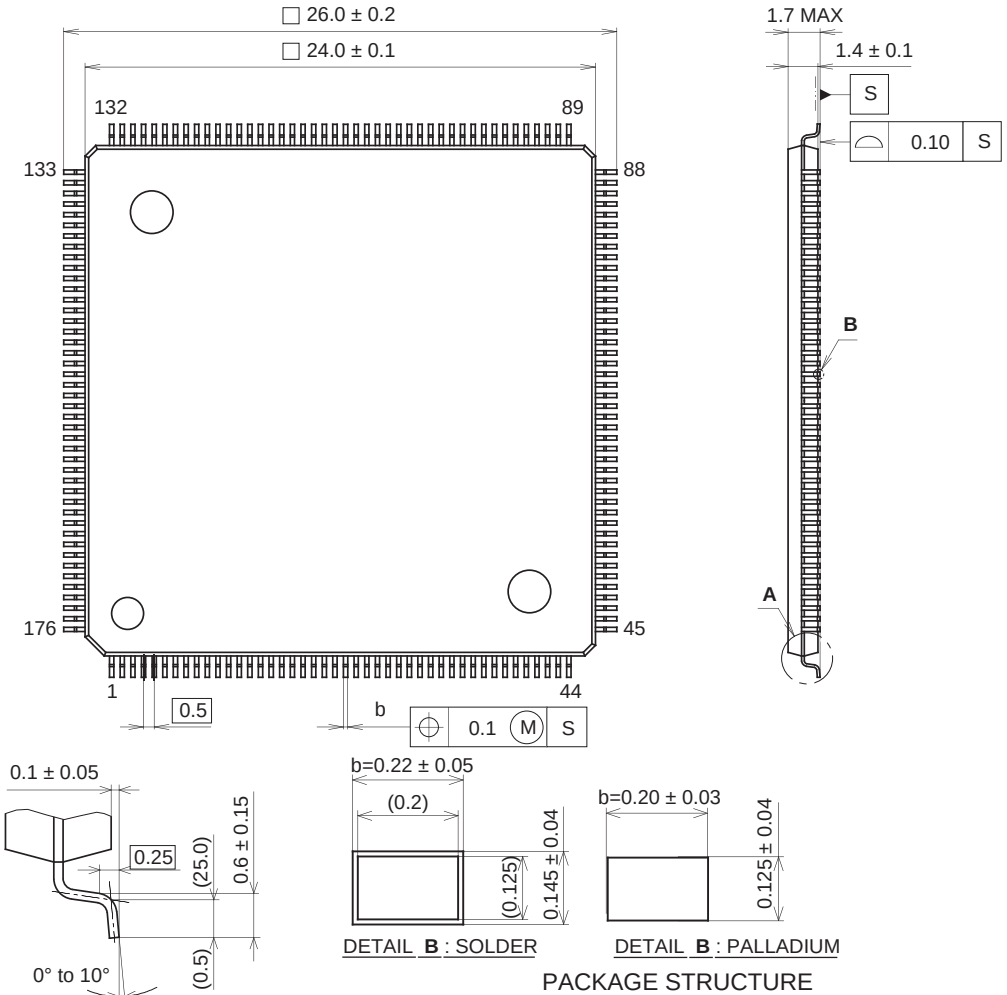
Item	Symbol	Conditions	Min.	Max.	Unit
TpA and TpB transfer jitter	$T_{TJITTER}$			±0.25	ns
Skew between TpA strobe and TpB data transfer	T_{TSKEW}			±0.15	ns
TpA and TpB transfer rise and fall	T_{TRF}	From 10% to 90%, via 55Ω and 10pF		2.2	ns

Reference Circuit Diagram



Package Outline Unit: mm

176PIN LQFP (PLASTIC)



SONY CODE	LQFP-176P-L01
EIAJ CODE	LQFP176-P-2424
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.8g