SONY

Dual SPDT Low Power Switch

CXG1404XR

Description

The CXG1404XR is a low power dual SPDT switch for Rx applications. It can be used as a differential signal switch.
The CXG1404XR has on-chip logic with single control reduces component counts and simplifies PCB layout by allowing direct connection of the switch to digital base band control lines with the CMOS logic levels.
The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity.

(Applications: CDMA/GSM/UMTS handsets, Differential signal switch)

Features

◆ Low insertion loss: 0.30 dB (Typ.) Rx (746 to 960 MHz)
0.35 dB (Typ.) Rx (1710 to 2170 MHz)
0.40 dB (Typ.) Rx (2500 to 2690 MHz)

◆ Low voltage operation: V_{DD} = 2.5 V

◆ On chip logic with single control

◆ Small package size: XQFN-12P (2.0 mm x 2.0 mm x 0.4 mm Max.)

◆ Lead-free and RoHS compliant

Structure

GaAs Junction Gate pHEMT (JPHEMT) MMIC Switch

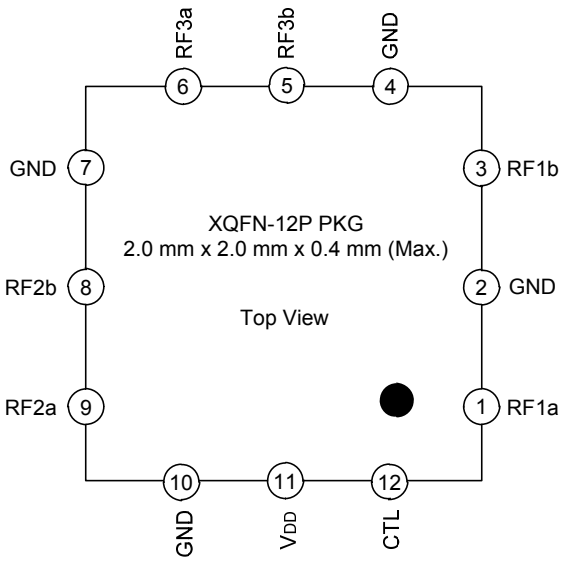
Absolute Maximum Ratings

(Ta = 25 ºC)

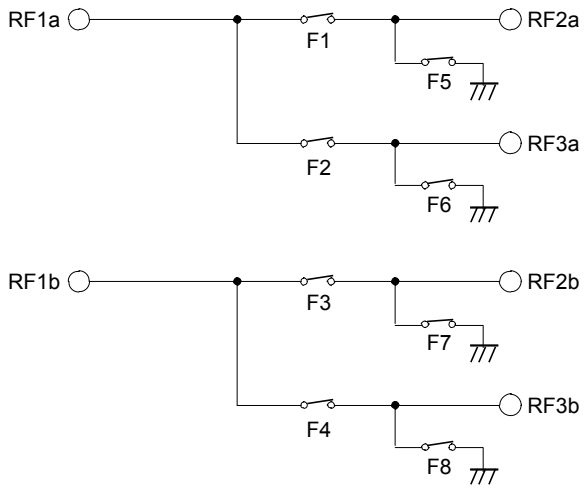
• Bias voltage	V_{DD}	4 V
• Control voltage	V_{CTL}	4 V
• Input power max.		18 dBm
• Operating temperature		–35 to +85 ºC
• Storage temperature		–65 to +150 ºC

GaAs MMIC's are ESD sensitive device. Special handling precautions are required.

Pin Configuration



Block Diagram



Truth Table

State	Active path	CTL state	Switch state							
			F1	F2	F3	F4	F5	F6	F7	F8
1	RF1a – RF2a, RF1b – RF2b	L	ON	OFF	ON	OFF	OFF	ON	OFF	ON
2	RF1a – RF3a, RF1b – RF3b	H	OFF	ON	OFF	ON	ON	OFF	ON	OFF

DC Bias Condition

Parameter	Min.	Typ.	Max.	Unit
V_{DD}	2.5	2.6	3.3	V
$V_{CTL(H)}$	1.5	1.8	3.3	V
$V_{CTL(L)}$	0	—	0.3	V

Target Specification

(V_{DD} = 2.6 V, Ta = 25 ºC)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	RF1a – RF2a, RF3a RF1b – RF2b, RF3b	*1	—	0.30	0.45	dB
			*2	—	0.35	0.50	
			*3	—	0.40	0.60	
Isolation	ISO	RF1a – RF2a, RF3a RF1b – RF2b, RF3b	746 to 960 MHz	25	28	—	dB
			1710 to 2170 MHz	21	24	—	
			2500 to 2690 MHz	19	22	—	
VSWR	VSWR	All ports in active paths	746 to 2690 MHz	—	—	1.40	—
Switching time	Ts		50 % Ctl to 90 % RF	—	3	5	µs
Control current	I_{CTL}		V_{CTL} = 1.80 V	—	7	20	µA
Supply current	I_{DD}		V_{DD} = 2.60 V	—	30	50	µA

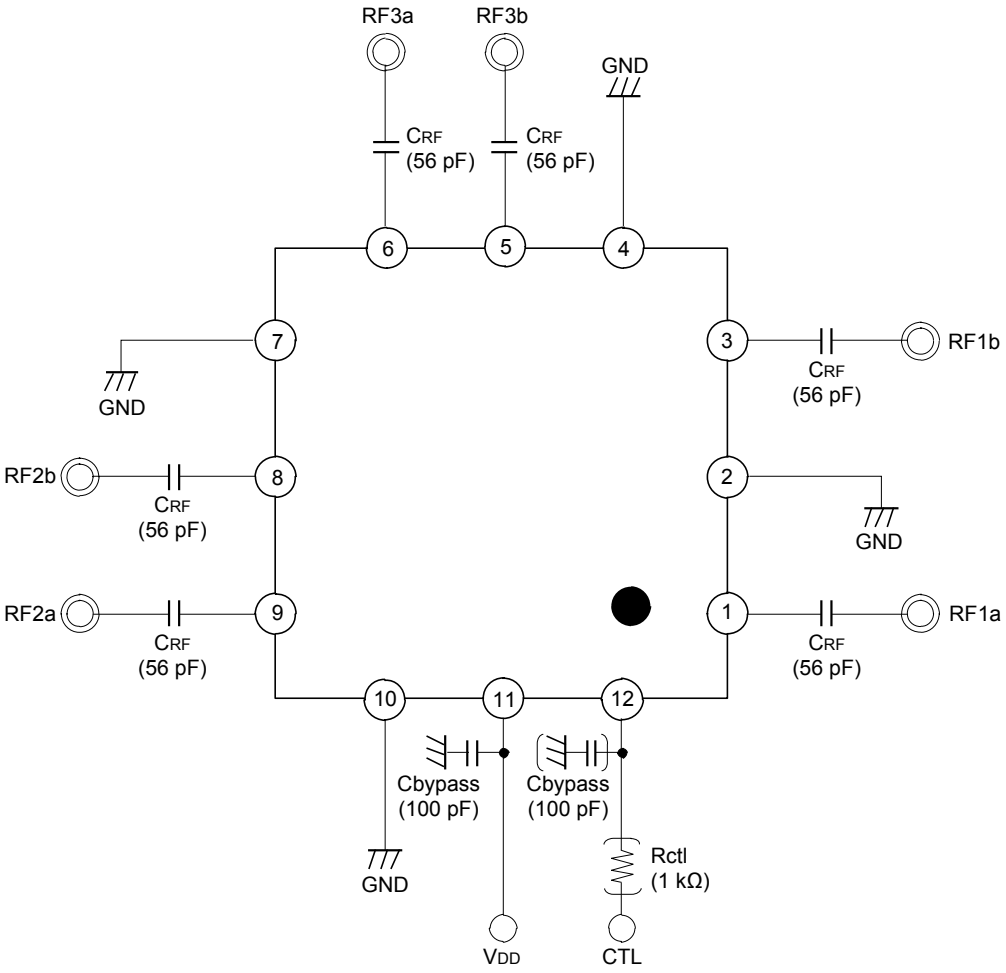
Electrical Characteristics are measured with all RF ports terminated in 50 Ω

*1 Pin = 10 dBm, 746 to 960 MHz

*2 Pin = 10 dBm, 1710 to 2170 MHz

*3 Pin = 10 dBm, 2500 to 2690 MHz

Recommended Circuit



When using this IC, the following external components should be used:

Rctl: This resistor is used to improved ESD performance. 1 kΩ is recommended.
CRF: This capacitor is used for RF De-coupling and must be used all application.
Cbypass: This capacitor is used for DC line filtering. 100 pF is recommended.

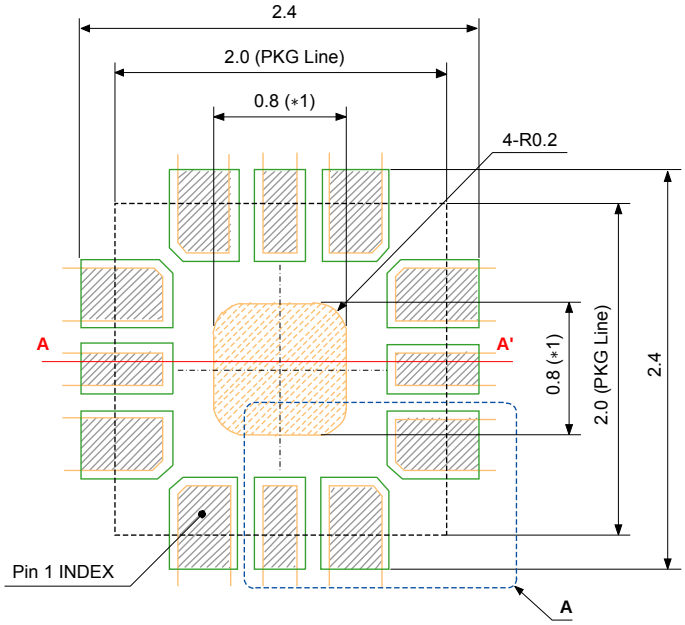
PCB Layout Template

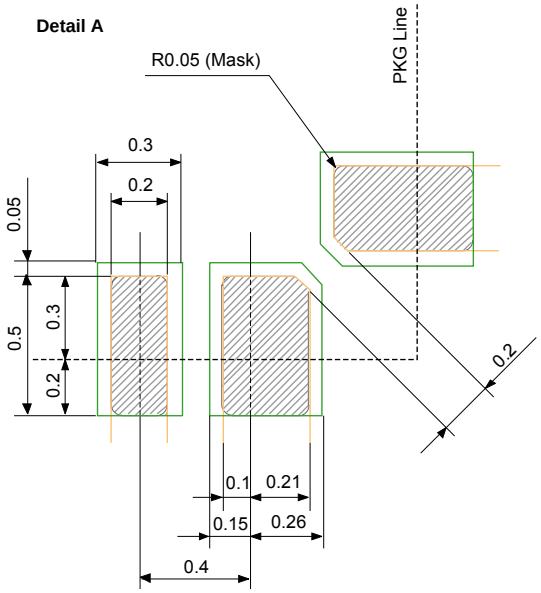
XQFN-12P-02 Macro drawing (Reference)

* Metal mask thickness: 110 µm
- PKG: 2.0 mm x 2.0 mm
- Pin pitch: 0.4 mm

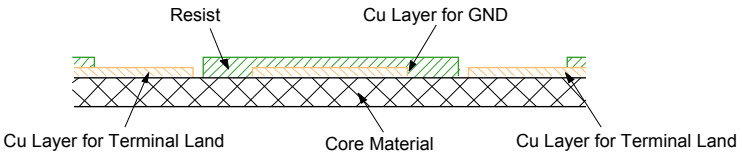
: Land
: Mask (Open area)
: Resist (Open area)
: Metal area in board (∗1)

∗1: GND plane is recommended.
A metallic layer (GND) is necessary
for this area to keep the performance.





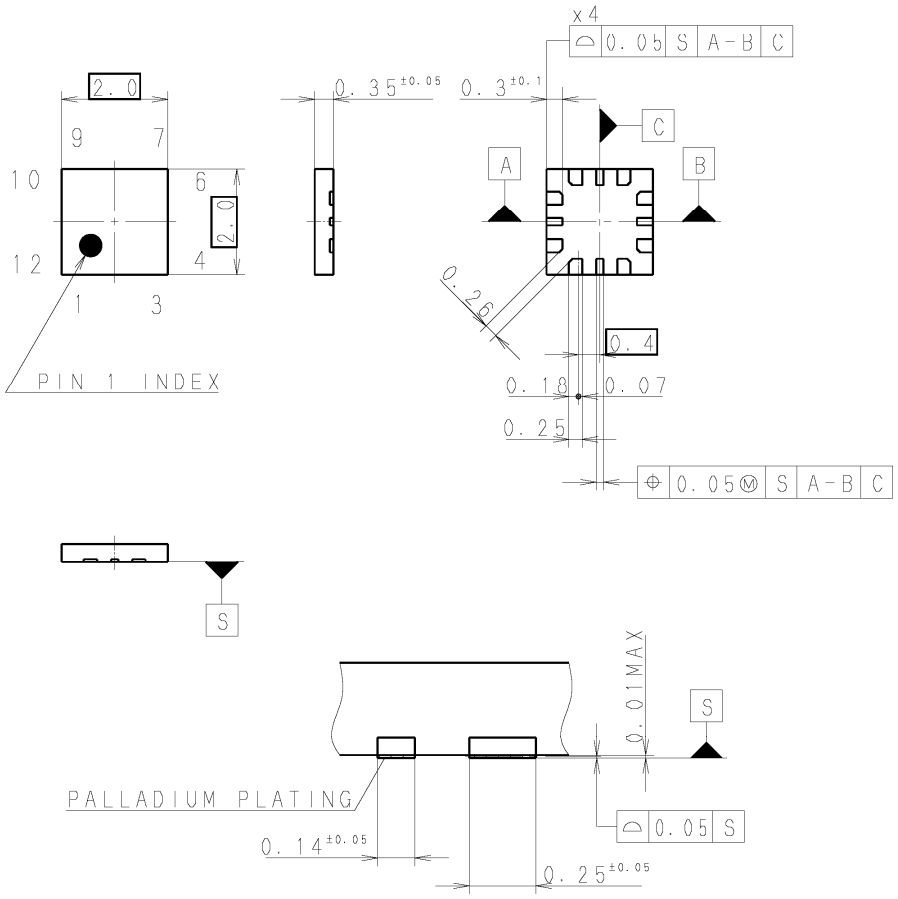
A-A' Cross section view



Package Outline

(Unit: mm)

12PIN XQFN (PLASTIC)



TERMINAL SECTION

Note:Terminal burr height 0.05mm MAX.

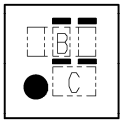
SONY CODE	XQFN-12P-02
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.004g

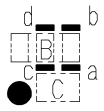
PART No. AP-4000-12013S	Rev. 0
ISSUED '11.08.30	REVISED
PRODUCTION LINE	COMPILING DIV. SDT ENGINEERING DIVISION
REMARKS PKG CODE:XR-012-D	

Marking



MARKING C: GC

注1） B部はロット番号（Ｍａｘ３文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記２進法ビット方式により表示する。）
ａ部年コード（２進法ビット方式の１ビット目を表示）を配置する。
ｂ部年コード（２進法ビット方式の２ビット目を表示）を配置する。
ｃ部年コード（２進法ビット方式の３ビット目を表示）を配置する。
ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注2） C部は製品名（Ｍａｘ２文字）を配置する。
（２文字を超える場合は製品名省略標示規定に従う。）
注3） マーク深さは，Ｍａｘ０．０５ｍｍの事。



DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION d.
2) TYPE NO. (MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.05 mm.

Note

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.