SONY

DP8T Antenna Switch Module for GSM/UMTS/CDMA Multi-mode Handsets

CXM3570ER

Description

The CXM3570ER is a DP8T antenna switch module for GSM/UMTS/CDMA multi-mode handset.
This IC has a built-in dual low pass filter and a +1.8 V CMOS compatible decoder.
The Sony JPHEMT MMIC process is used for low insertion loss and high linearity.
The device has low BOM with no DC blocking capacitor.
(Application: GSM/UMTS/CDMA multi-mode handset)

Features

- ◆ Low insertion loss: 0.52 dB (Typ.) TRx (Cellular band)
  0.72 dB (Typ.) TRx (IMT Tx band)
- ◆ Low-voltage operation: V_{DD} = 2.5 V
- ◆ No DC blocking capacitor
- ◆ Small packing (size): VQFN-26P (3.0 mm × 3.8 mm × 0.85 mm Max.)
- ◆ Lead-free and RoHS compliant

Structure

- ◆ GaAs JPHEMT MMIC switch, CMOS decoder

This IC is ESD sensitive device. Special handling precautions are required.

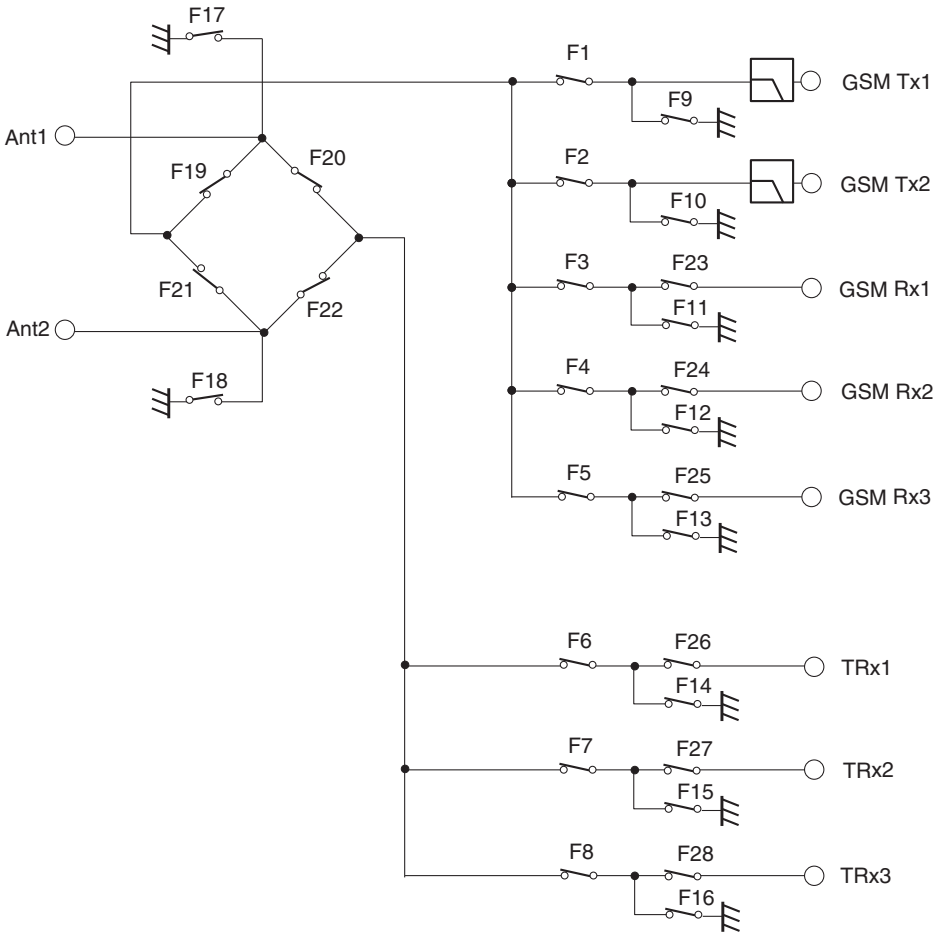
E10923A21

Absolute Maximum Ratings

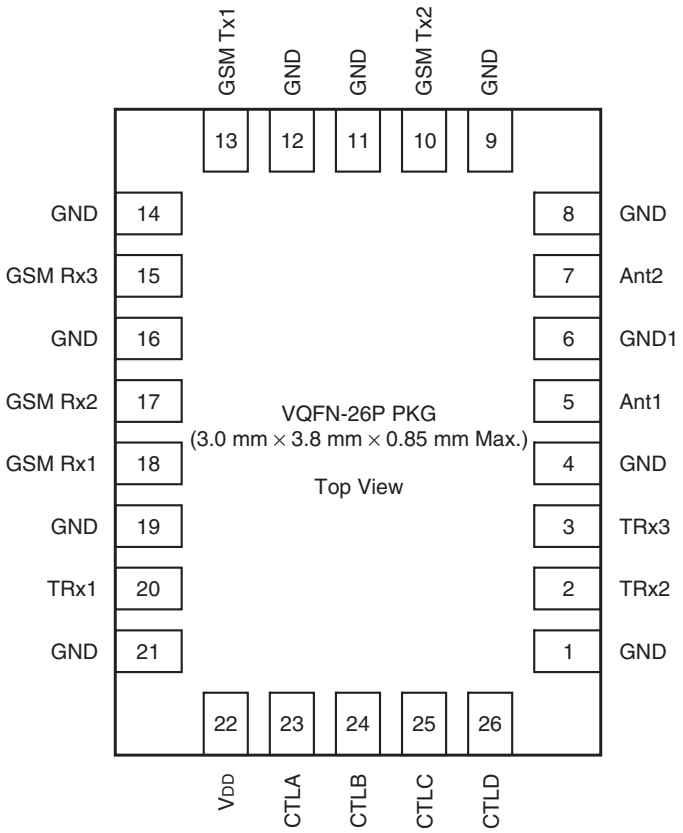
(Ta = 25 ℃)

Bias voltage	V_{DD}	4	V
Control voltage	Vctl	4	V
Input power max. (Tx1)		36	dBm (Duty cycle = 12.5 % to 50 %)
Input power max. (Tx2)		34	dBm (Duty cycle = 12.5 % to 50 %)
Input power max. (TRx1, 2, 3)		32	dBm
Input power max. (Rx1, 2, 3)		13	dBm
Operating temperature range		–20 to +90	℃
Storage temperature range		–65 to +150	℃

Block Diagram



Pin Configuration



Truth Table

State	CTL A	CTL B	CTLC	CTL D	Active Port	Active Ant	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18
1	L	H	L	H	TRx1	ANT1	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	ON	ON	OFF	ON
2	H	H	L	H	TRx2	ANT1	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	OFF	ON	OFF	ON
3	L	H	H	H	TRx3	ANT1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	ON
4	L	L	H	H	GSM Rx1	ANT1	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON	ON	ON	OFF	ON
5	H	L	H	H	GSM Rx2	ANT1	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON	ON	ON	ON	OFF	ON
6	H	H	H	H	GSM Rx3	ANT1	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	OFF	ON
7	H	L	L	H	GSM Tx1	ANT1	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	OFF	ON
8	L	L	L	H	GSM Tx2	ANT1	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	OFF	ON
9	L	H	L	L	TRx1	ANT2	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	ON	ON	ON	OFF
10	H	H	L	L	TRx2	ANT2	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	OFF	ON	ON	OFF
11	L	H	H	L	TRx3	ANT2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	ON	OFF	ON	OFF
12	L	L	H	L	GSM Rx1	ANT2	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON	ON	ON	ON	OFF
13	H	L	H	L	GSM Rx2	ANT2	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON	ON	ON	ON	ON	OFF
14	H	H	H	L	GSM Rx3	ANT2	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	ON	OFF
15	H	L	L	L	GSM Tx1	ANT2	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	ON	OFF
16	L	L	L	L	GSM Tx2	ANT2	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON	ON	ON	OFF

State	CTL A	CTL B	CTLC	CTL D	Active Port	Active Ant	F19	F20	F21	F22	F23	F24	F25	F26	F27	F28
1	L	H	L	H	TRx1	ANT1	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
2	H	H	L	H	TRx2	ANT1	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
3	L	H	H	H	TRx3	ANT1	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
4	L	L	H	H	GSM Rx1	ANT1	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
5	H	L	H	H	GSM Rx2	ANT1	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
6	H	H	H	H	GSM Rx3	ANT1	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
7	H	L	L	H	GSM Tx1	ANT1	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
8	L	L	L	H	GSM Tx2	ANT1	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
9	L	H	L	L	TRx1	ANT2	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
10	H	H	L	L	TRx2	ANT2	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF
11	L	H	H	L	TRx3	ANT2	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON
12	L	L	H	L	GSM Rx1	ANT2	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF
13	H	L	H	L	GSM Rx2	ANT2	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF
14	H	H	H	L	GSM Rx3	ANT2	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
15	H	L	L	L	GSM Tx1	ANT2	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
16	L	L	L	L	GSM Tx2	ANT2	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF

DC Bias Conditions

(Ta = 25 ℃)

Item	Min.	Typ.	Max.	Unit
V_{DD}	2.5	2.8	3.3	V
Vctl (H)	1.35	1.8	3.3	V
Vctl (L)	0	—	0.45	V

Electrical Characteristics

(Ta = 25 ℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Switching speed	Tsw		—	3	5	μs
Startup time	Tst	V_{DD} = 0 to 2.8 V	—	6	50	μs
Control current	Ictl	Vctl = 1.8 V per line	—	0.01	1	μA
Supply current	I_{DD}	V_{DD} = 2.8 V	—	240	500	μA

Item	Symbol	Path	Condition	Ant1 Active			Ant2 Active			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Insertion loss	IL	Ant1/Ant2 – Tx1	*1	—	1.30	1.45	—	1.32	1.47	dB
		Ant1/Ant2 – Tx2	*2	—	1.15	1.30	—	1.16	1.31	dB
		Ant1/Ant2 – Rx1/2/3	*3	—	0.90	1.05	—	0.90	1.05	dB
		Ant1/Ant2 – Rx1/2/3	*4	—	1.15	1.30	—	1.11	1.26	dB
		Ant1/Ant2 – TRx1/2/3	*5	—	0.52	0.67	—	0.52	0.67	dB
		Ant1/Ant2 – TRx1/2	*6	—	0.68	0.83	—	0.67	0.82	dB
		Ant1/Ant2 – TRx3	*6	—	0.77	0.92	—	0.73	0.88	dB
		Ant1/Ant2 – TRx1/2	*7	—	0.75	0.90	—	0.72	0.87	dB
		Ant1/Ant2 – TRx3	*7	—	0.86	1.01	—	0.80	0.95	dB
VSWR	VSWR	All ports in Active paths	824 to 2170 MHz	—	1.3	—	—	1.3	—	—
Rx in-band spurious	SPR	Ant1/Ant2 – Rx1, 2, 3	*3, *4		—	–125		—	–125	dBm
Attenuation	ATT	Tx1 – Ant/Ent	1648 to 1830 MHz	25	30	—	25	30	—	dB
			2472 to 2745 MHz	25	31	—	25	30	—	dB
			3296 to 12750 MHz	20	30	—	20	33	—	dB
		Tx2 – Ant/Ent	3420 to 3820 MHz	25	30	—	25	28	—	dB
			5130 to 5730 MHz	25	40	—	25	28	—	dB
			6840 to 7000 MHz	15	21	—	15	21	—	dB
			7000 to 12750 MHz	20	23	—	20	27	—	dB

Electrical characteristics are measured with all RF ports terminated in 50 Ω.

*1 Pin on Tx1: 35 dBm, 824 to 915 MHz, V_{DD} = 2.8 V, Tx1 enable

*2 Pin on Tx2: 32 dBm, 1710 to 1910 MHz, V_{DD} = 2.8 V, Tx2 enable

*3 Pin on Ant: 10 dBm, 869 to 960 MHz, V_{DD} = 2.8 V, Rx1 or Rx2 or Rx3 enable

*4 Pin on Ant: 10 dBm, 1805 to 1990 MHz, V_{DD} = 2.8 V, Rx1 or Rx2 or Rx3 enable

*5 Pin on TRx1 or TRx2 or TRx3: 26 dBm, 824 to 894 MHz, V_{DD} = 2.8 V, TRx1 or TRx2 or TRx3 enable

*6 Pin on TRx1 or TRx2 or TRx3: 26 dBm, 1750 to 1880 MHz, V_{DD} = 2.8 V, TRx1 or TRx2 or TRx3 enable

*7 Pin on TRx1 or TRx2 or TRx3: 26 dBm, 1920 to 2170 MHz, V_{DD} = 2.8 V, TRx1 or TRx2 or TRx3 enable

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO1	Tx1 - Rx1, 2	Tx1 - Ant1/Ant2 Active Freq. = Tx1_Band	30	53	—	dB
		Tx1 - Rx3	Tx1 - Ant1/Ant2 Active Freq. = Tx1_Band	30	45	—	dB
		Tx1 - TRx1, 2, 3	Tx1 - Ant1/Ant2 Active Freq. = Tx1_Band	30	50	—	dB
		Tx2 - Rx1, 2, 3	Tx2 - Ant1/Ant2 Active Freq. = Tx2_Band	30	55	—	dB
		Tx2 - TRx1, 2	Tx2 - Ant1/Ant2 Active Freq. = Tx2_Band	30	50	—	dB
		Tx2 - TRx3	Tx2 - Ant1/Ant2 Active Freq .= Tx2_Band	30	42	—	dB
	ISO2	TRx1 - TRx2	TRx1/2/3 Active Freq. = TRx_Band	30	44	—	dB
		TRx1 - TRx3	TRx1/2/3 Active Freq. = TRx_Band	30	45	—	dB
		TRx2 - TRx3	TRx1/2/3 Active Freq. = TRx_Band	21	26	—	dB
	ISO3	Tx1- Ant1/Ant2	Rx1/2/3 Active Freq. = Tx1_Band	25	35	—	dB
		Tx2- Ant1/Ant2	Rx1/2/3 Active Freq. = Tx2_Band	21	27	—	dB
	ISO4	Tx1 - Tx2	Tx1 Active Freq. = Tx1_Band	17	21	—	dB
			Tx2 Active Freq. = Tx2_Band	20	27	—	dB

Item	Symbol	Path	Condition	Ant1 Active			Ant2 Active			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Harmonics	2fo	Tx1 –Ant1/Ant2	*1	—	–45	–36	—	–43	–36	dBm
	3fo			—	–50	–36	—	–50	–36	dBm
	2fo	Tx2 –Ant1/Ant2	*2	—	–58	–39	—	–52	–39	dBm
	3fo			—	–52	–39	—	–53	–39	dBm
	2fo	TRx1 –Ant1/Ant2	*3	—	–65	–39	—	–65	–39	dBm
	3fo			—	–65	–39	—	–65	–39	dBm
	2fo	TRx2 –Ant1/Ant2	*4	—	–65	–39	—	–65	–39	dBm
	3fo			—	–65	–39	—	–65	–39	dBm
	2fo	TRx3 –Ant1/Ant2	*5	—	–65	–39	—	–65	–39	dBm
	3fo			—	–65	–39	—	–65	–39	dBm
ACLR***	±5 MHz	TRx1–Ant1/Ant2	*3	—	—	–50	—	—	–50	dBc
	±10 MHz			—	—	–55	—	—	–55	dBc
	±5 MHz	Rx2–Ant1/Ant2	*4	—	—	–50	—	—	–50	dBc
	±10 MHz			—	—	–55	—	—	–55	dBc
	±5 MHz	Rx3–Ant1/Ant2	*5	—	—	–50	—	—	–50	dBc
	±10 MHz			—	—	–55	—	—	–55	dBc

Electrical characteristics are measured with all RF ports terminated in 50 Ω.

*1 Pin on Tx1: 35 dBm, 824 to 915 MHz, V_{DD} = 2.8 V, Tx1 enable

*2 Pin on Tx2: 32 dBm, 1710 to 1910 MHz, V_{DD} = 2.8 V, Tx2 enable

*3 Pin on TRx1 or TRx2 or TRx3: 26 dBm, 824 to 894 MHz, V_{DD} = 2.8 V, TRx1 or TRx2 or TRx3 enable

*4 Pin on TRx1 or TRx2 or TRx3: 26 dBm, 1750 to 1880 MHz, V_{DD} = 2.8 V, TRx1 or TRx2 or TRx3 enable

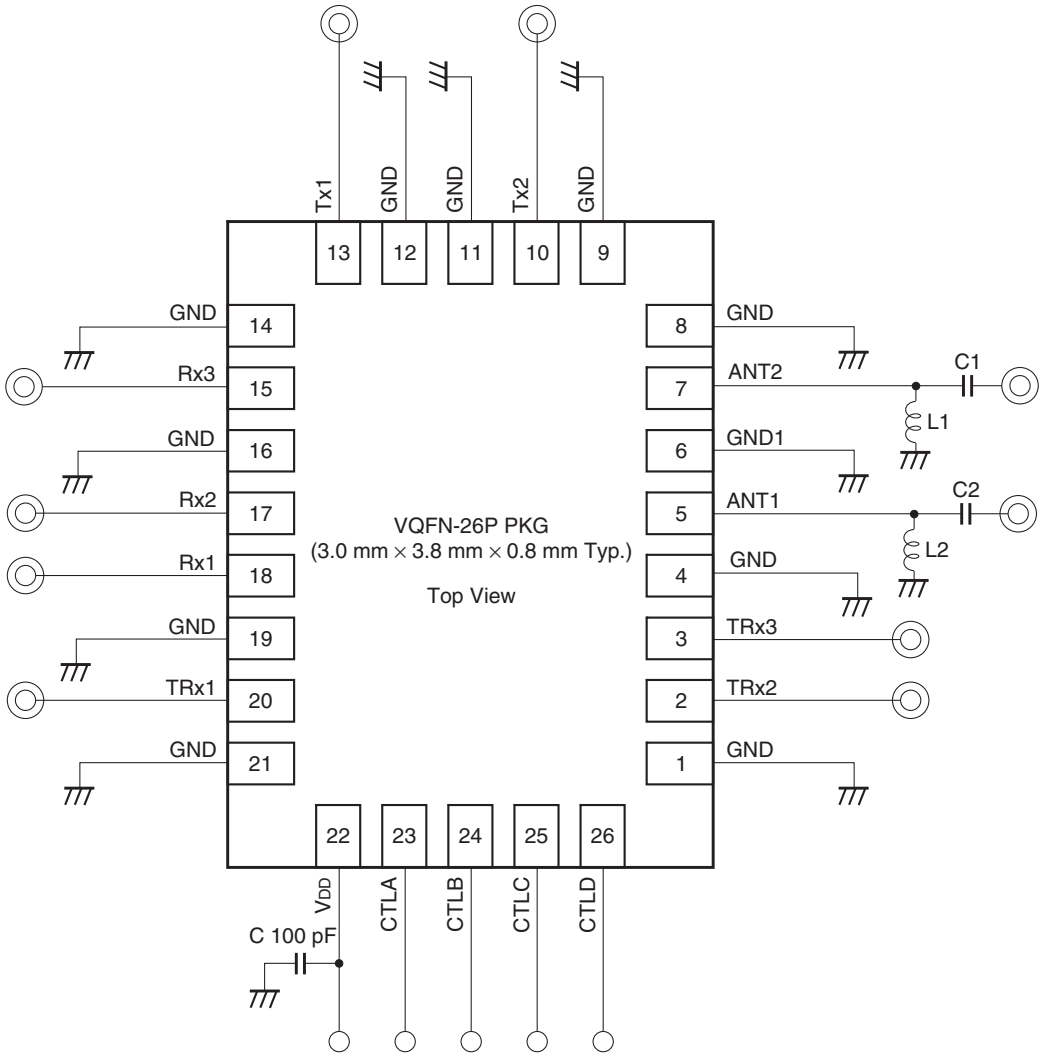
*5 Pin on TRx1 or TRx2 or TRx3: 26 dBm, 1920 to 2170 MHz, V_{DD} = 2.8 V, Rx1 or TRx2 or TRx3 enable

Item	Symbol	Path	Condition	Ant1 Active			Ant2 Active			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Intermodulation distortion	IMD2	TRx1 –Ant1/Ant2	*1, *13	—	–125	–110	—	–125	–110	dBm
			*2, *13	—	–123	–110	—	–126	–110	dBm
		TRx2 –Ant1/Ant2	*3, *13	—	–115	–105	—	–115	–105	dBm
			*4, *13	—	–110	–105	—	–111	–105	dBm
		TRx3 –Ant1/Ant2	*5, *13	—	–113	–105	—	–110	–105	dBm
			*6, *13	—	–111	–105	—	–116	–105	dBm
	IMD3	TRx1 –Ant1/Ant2	*7, *13	—	–112	–105	—	–112	–105	dBm
			*8, *13	—	–113	–105	—	–114	–105	dBm
		TRx2 –Ant1/Ant2	*9, *13	—	–108	–103	—	–108	–103	dBm
			*10, *13	—	–110	–105	—	–110	–105	dBm
		TRx3 –Ant1/Ant2	*11, *13	—	–108	–103	—	–110	–105	dBm
			*12, *13	—	–110	–105	—	–112	–105	dBm

Electrical characteristics are measured with all RF ports terminated in 50 Ω.

*1 TRx port: +21.5 dBm, 835 MHz Ant port: –15 dBm, 45 MHz, V_{DD} = 2.8 V
*2 TRx port: +21.5 dBm, 835 MHz Ant port: –15 dBm, 1715 MHz, V_{DD} = 2.8 V
*3 TRx port: +21.5 dBm, 1765 MHz Ant port: –15 dBm, 95 MHz, V_{DD} = 2.8 V
*4 TRx port: +21.5 dBm, 1765 MHz Ant port: –15 dBm, 3625 MHz, V_{DD} = 2.8 V
*5 TRx port: +21.5 dBm, 1950 MHz Ant port: –15 dBm, 190 MHz, V_{DD} = 2.8 V
*6 TRx port: +21.5 dBm, 1950 MHz Ant port: –15 dBm, 4090 MHz, V_{DD} = 2.8 V
*7 TRx port: +21.5 dBm, 835 MHz Ant port: –15 dBm, 790 MHz, V_{DD} = 2.8 V
*8 TRx port: +21.5 dBm, 835 MHz Ant port: –15 dBm, 2550 MHz, V_{DD} = 2.8 V
*9 TRx port: +21.5 dBm, 1765 MHz Ant port: –15 dBm, 1670 MHz, V_{DD} = 2.8 V
*10 TRx port: +21.5 dBm, 1765 MHz Ant port: –15 dBm, 5390 MHz, V_{DD} = 2.8 V
*11 TRx port: +21.5 dBm, 1950 MHz Ant port: –15 dBm, 1760 MHz, V_{DD} = 2.8 V
*12 TRx port: +21.5 dBm, 1950 MHz Ant port: –15 dBm, 6040 MHz, V_{DD} = 2.8 V
*13 Measured with the recommended circuit

Recommended Circuit

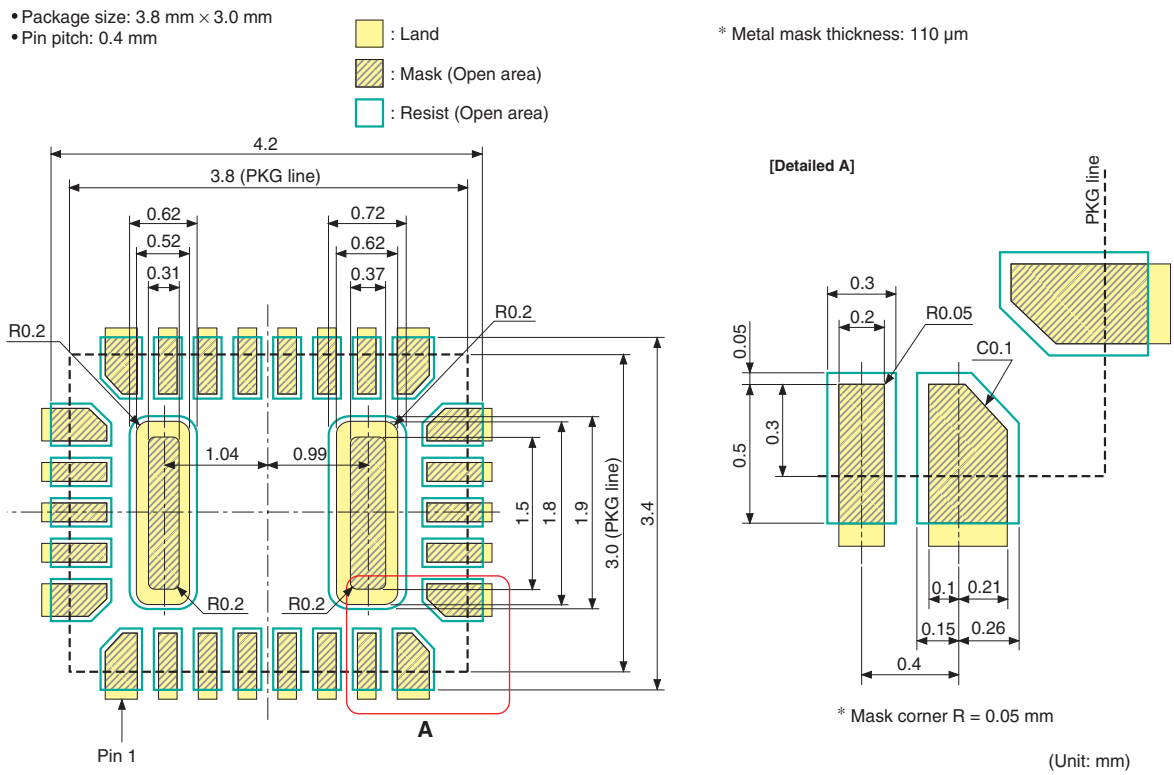


∗ L1 = 22 nH, C1 = 12 pF, L2 = 22 nH, C2 = 12 pF

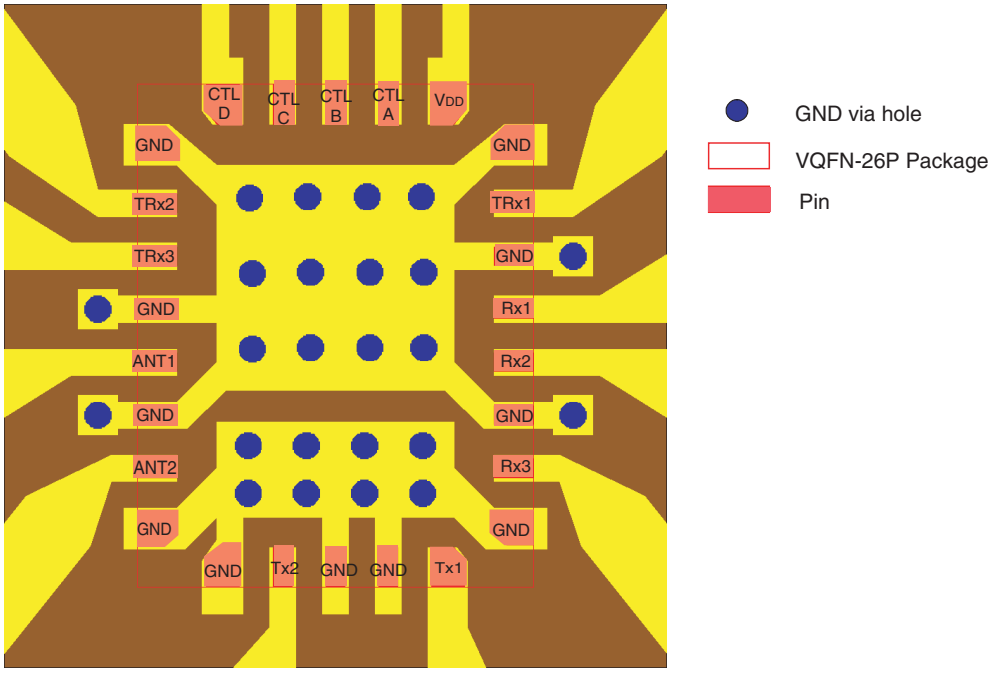
Note) 1. No DC block capacitors are required on each RF port.
2. DC levels of all RF ports are GND.
3. L1/L2 inductor and C1/C2 capacitor are recommended on Ant port for IMD2 and ESD protection.

PCB Layout Template

Recommended land pattern



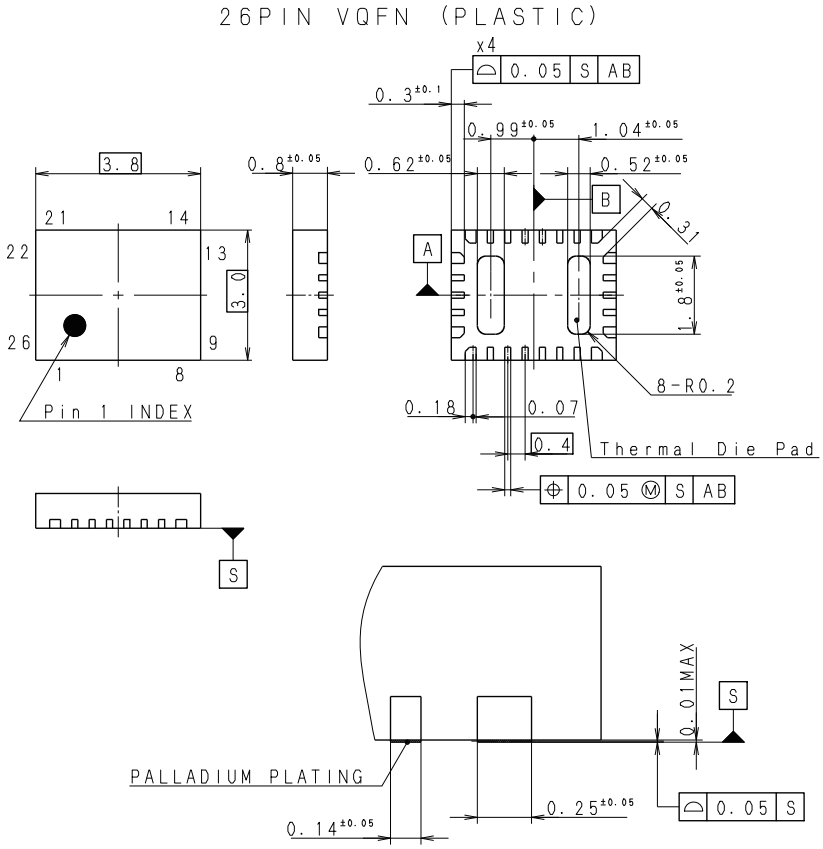
Recommended PCB Design



Package Outline

(Unit: mm)

Product Code: 875340957



Note:Cutting burr of lead are 0.05mm MAX.

TERMINAL SECTION

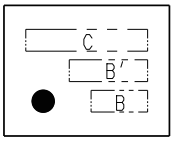
PACKAGE STRUCTURE

SONY CODE	VQFN-26P-541
JEITA CODE	————
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.03g

PART No. AP-2000-26QNBE2	Rev. 0
ISSUED '11.11.24	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:ER-26-EBE	

Marking



MARKING C: M3570

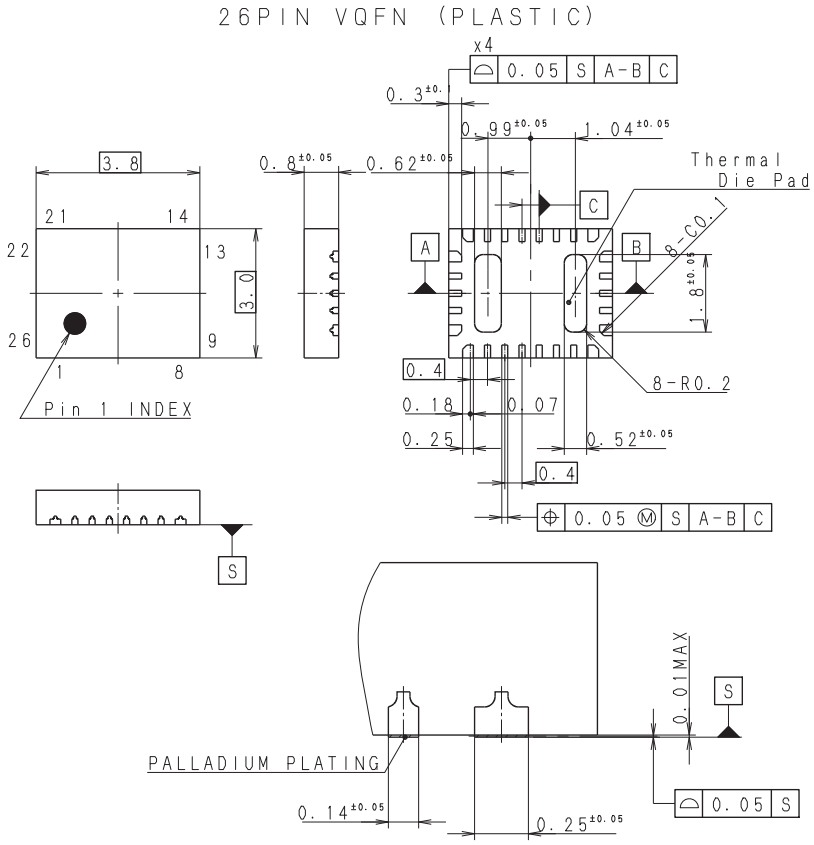
注1) C部は製品名(Max6文字)を配置する。
(6文字を超える場合は製品名省略標示規定に従う。)
2) B, B' 部はロット番号(Max7文字)を配置する。
(但し B部Max3文字, B'部Max4文字とする。規定文字数未満につき省略は省略規定に従う。)
3) 文字位置は、右詰めとする。

< INSTRUCTIONS >
1) TYPE NO. (MAX 6 CHARACTERS) IN SECTION C.
(FOR MORE THAN 6 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) LOT NO. (MAX 7 CHARACTERS) IN SECTION B, B'.
(B: 3 CHARACTERS , B': 4 CHARACTERS. FOLL RULES FOR ABBREVIATIONS.)
3) PUT THE POSITION OF A CHARACTER REFERENCE FROM THE RIGHT SIDE.

Package outline

(Unit: mm)

Product Code: 875337503

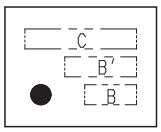


SONY CODE	VQFN-26P-01
JEITA CODE	————
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.03g

PART No. AP-4000-26009S	Rev. 0
ISSUED 10.09.24	REVISED
PRODUCTION LINE	COMPILING DIV. SDT ENGINEERING DIVISION
REMARKS PKG CODE:ER-026-AB	

Marking



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