SONY

SP12T Antenna Switch Module for 7TRx/2Tx/3Rx

CXM3583AUR

Description

The CXM3583AUR is a SP12T antenna switch module for GSM/UMTS/CDMA/LTE multi-mode handset.
The CXM3583AUR has a built-in dual low pass filter and a +1.8 V CMOS compatible decoder.
The Sony GaAs junction gate PHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity.
The device has low BOM with no DC blocking Capacitor.

Features

- Low Insertion Loss: 0.50 dB (Typ.) TRx (Cellular Band)
  0.60 dB (Typ.) TRx (IMT Tx Band)
- High Linearity: IIP3 = 68 dBm
- Low Voltage Operation: V_{DD} = 2.5 V
- No DC Blocking Capacitors except sourcing DC bias.
- Small Package Size: UQFN-30P (3.0 mm × 3.8 mm × 0.625 mm Max.)
- Lead-Free and RoHS Compliant.

Structure

GaAs Junction Gate PHEMT (JPHEMT) MMIC Switch, CMOS Decoder.

Moisture Sensitivity

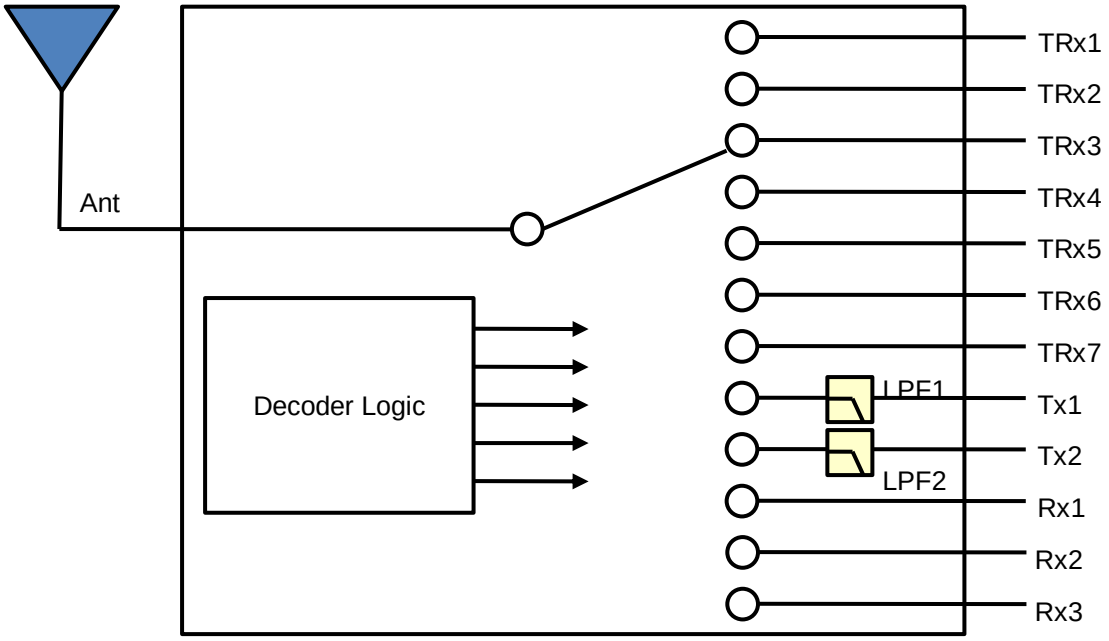
Moisture Sensitivity Level for this part is MSL = 2

This IC is ESD sensitive device. Special handling precautions are required.

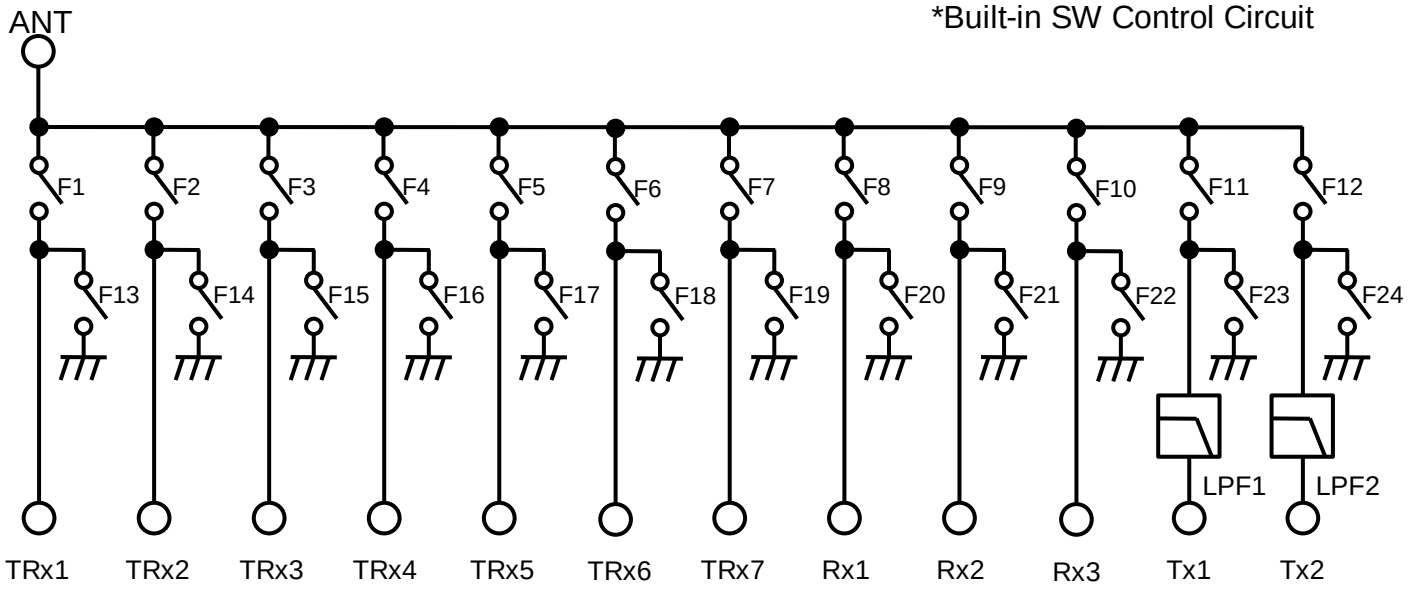
E12702A2Z

Block Diagram

SP12T Antenna Switch Module



SP12T 7TRx/2Tx/3Rx

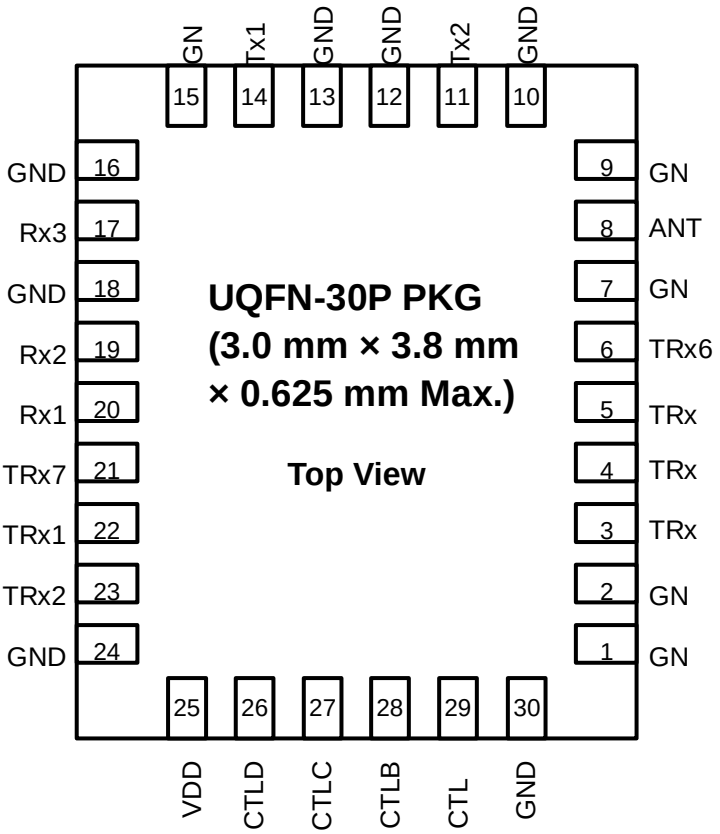


Truth Table

State	Active Path	CTL State				Switch State (*1)																							
		A	B	C	D	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20	F21	F22	F23	F24
1	TRx1	H	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H
2	TRx2	H	H	H	L	L	H	L	L	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H
3	TRx3	H	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H
4	TRx4	H	H	H	H	L	L	L	H	L	L	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H
5	TRx5	H	L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H
6	TRx6	H	H	L	H	L	L	L	L	L	H	L	L	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H
7	TRx7	L	L	L	H	L	L	L	L	L	L	H	L	L	L	L	L	H	H	H	H	H	H	L	H	H	H	H	H
8	Rx1	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H
9	Rx2	L	H	H	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H
10	Rx3	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H
11	Tx1	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H
12	Tx2	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

(*1) State ”L” means a switch “OFF”, State ”H” means a switch “ON”

Pin Configuration



Pin No.	Name	Pin No.	Name
1	GND	16	GND
2	GND	17	Rx3
3	TRx3	18	GND
4	TRx4	19	Rx2
5	TRx5	20	Rx1
6	TRx6	21	TRx7
7	GND	22	TRx1
8	ANT	23	TRx2
9	GND	24	GND
10	GND	25	VDD
11	Tx2(DCS/PCS)	26	CTLD
12	GND	27	CTLC
13	GND	28	CTLB
14	Tx1(GSM850/900M)	29	CTLA
15	GND	30	GND

DC Bias Conditions

Ta=25 ℃

Parameter	Min.	Typ.	Max.	Unit
V_{DD}	2.5	2.8	3.3	V
Vctl(H)	1.35	1.8	3.1	V
Vctl(L)	0	-	0.45	V

Absolute Maximum Ratings

◆Supply voltage	V_{DD}	4	V	(Ta = 25 °C)
◆Control voltage	Vctl	4	V	(Ta = 25 °C)
◆Maximum input	[Tx1]	36	dBm	(Duty cycle = 12.5 % to 50 %) (Ta = 25 °C)
	[Tx2]	34	dBm	(Duty cycle = 12.5 % to 50 %) (Ta = 25 °C)
	[TRx]	32	dBm	(Ta = 25 °C)
	[Rx]	13	dBm	(Ta = 25 °C)
◆Operating temperature	Topr	–35 to +90	°C	
◆Storage temperature	Tstg	–65 to +150	°C	

Electrical Characteristics

V_{DD} = 2.5 V, Vctl = 1.80 V, Ta = 25 °C

Item	Symbol	Path	Condition	Min	Typ	Max	Unit
Insertion Loss	IL	Ant - TRx1	*1, *2, *3	-	0.44	0.54	dB
			*4	-	0.71	0.86	
			*5	-	0.78	0.93	
			*6	-	0.86	1.06	
			*7	-	1.02	1.22	
		Ant - TRx2	*1, *2, *3	-	0.48	0.58	
			*4	-	0.72	0.87	
			*5	-	0.78	0.93	
			*6	-	0.87	1.07	
			*7	-	1.00	1.20	
		Ant - TRx3	*1, *2, *3	-	0.44	0.54	
			*4	-	0.71	0.86	
			*5	-	0.77	0.92	
			*6	-	0.85	1.05	
			*7	-	0.98	1.18	
		Ant - TRx4	*1, *2, *3	-	0.50	0.60	
			*4	-	0.87	1.02	
			*5	-	0.95	1.10	
			*6	-	1.08	1.28	
			*7	-	1.29	1.49	
		Ant - TRx5	*1, *2, *3	-	0.52	0.62	
			*4	-	0.99	1.14	
			*5	-	1.09	1.24	
			*6	-	1.22	1.42	
			*7	-	1.44	1.64	
		Ant - TRx6	*1, *2, *3	-	0.53	0.63	
			*4	-	0.98	1.13	
			*5	-	1.09	1.24	
			*6	-	1.24	1.44	
			*7	-	1.49	1.69	
		Ant - TRx7	*1, *2, *3	-	0.45	0.55	
			*4	-	0.71	0.86	
			*5	-	0.78	0.93	
			*6	-	0.86	1.01	
			*7	-	1.00	1.20	
		Ant - Tx1	*8	-	1.02	1.17	
		Ant - Tx2	*9	-	1.05	1.25	
		Ant - Rx1	*10	-	0.75	0.85	
			*11	-	1.11	1.26	
		Ant - Rx2	*10	-	0.75	0.85	
			*11	-	1.09	1.24	
		Ant - Rx3	*10	-	0.74	0.84	
			*11	-	1.00	1.15	

(*)Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

Electrical Characteristics

V_{DD} = 2.5 V, Vctl = 1.80 V, Ta = 25 °C

Item	Symbol	Path	Condition	Min	Typ	Max	Unit
Isolation	ISO	Tx1 - TRx1,2,3,4,5,6,7 Tx1 - Rx1,2,3	*8	45	-	-	dB
		Tx2 - TRx1,2,3,4,5,6,7	*9	35	-	-	
		Tx2 - Rx1,2,3		45	-	-	
		TRx1 - TRx2,7 TRx4 - TRx3,5 TRx5 - TRx6	452 MHz to 1990 MHz	17	-	-	
		TRx1,2,7 - TRx3,4,5,6	452 MHz to 1990 MHz	35	-	-	
		TRx7 - TRx2 TRx3 - TRx5,6 TRx4 - TRx6	452 MHz to 1990 MHz	23	-	-	
		Rx1 - Ant (Rx3: Active)	1805 MHz to 1990 MHz	45	-	-	
		Rx3 - Ant (Rx1: Active)		42	-	-	
		Rx2 - Ant (Rx3: Active)		33	-	-	
		Rx3 - Ant (Rx2: Active)		33	-	-	
Attenuation	ATT	Tx1 - Ant	1648 MHz to 1805 MHz	25	-	-	dB
			1805 MHz to 1830 MHz	30	-	-	
			2472 MHz to 2745 MHz	25	-	-	
			3296 MHz to 12750 MHz	20	-	-	
		Tx2 - Ant	3420 MHz to 3820 MHz	25	-	-	
			5130 MHz to 5730 MHz	25	-	-	
			6840 MHz to 12750 MHz	20	-	-	
Harmonics	2fo	Ant - TRx1,2,3,4,5,6,7	*3, *4	-	-	-40	dBm
	3fo			-	-	-40	
	2fo	Ant - TRx1,3,7	*2,*12B	-	-	-78	
	2fo	Ant - Tx1	*8	-	-	-36	
	3fo			-	-	-36	
	2fo	Ant - Tx2	*9	-	-	-36	
	3fo			-	-	-36	
V.S.W.R.	V.S.W.R.	All Ports in Active Paths	452 MHz to 2170 MHz	-	-	1.5	-
Switching Time	Ts	Ant - TRx2,4,5,6 Ant - Tx1,2 Ant - Rx1,2,3	50 % Ctl – 90 % RF	-	-	5	µs
		Ant -TRx1,3,7				7	µs
Control Current	Ictl	-	Vctl = 1.8 V	-	-	10	µA
Supply Current	Idd	-	Vdd = 2.8 V	-	0.19	0.30	mA
Inter Modulation Distortion Level in Rx band	IMD2	Ant - TRx1,2,3,4,5,6,7	*12A,13,14,17,18,21,22	-	-	-105	dBm
	IMD3		*12A,15,16,19,20,23,24	-	-	-105	
Input IP2	IIP2	Ant - TRx1,2,3,4,5,6,7	*12A,25,26,27,28,30	95.5	-	-	dBm
			*29	113.5	-	-	
Input IP3	IIP3	Ant - TRx1,2,3,4,5,6,7	*12A,31,32	-	68	-	dBm
Triple Beat Ratio	TBR	Ant - TRx1,2,3,4,5,6,7	*12A,33,34	81	-	-	dBc

(*)Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

Electrical Characteristics

Corresponding Band of TRx (UMTS/CDMA)

*1: Pin = 26 dBm, 452 MHz to 468 MHz(Band Class 5)

*2: Pin = 25 dBm, 704 MHz to 787 MHz(Band 13, Band 17)

*3: Pin = 26 dBm, 824 MHz to 960 MHz(Band 5, Band 8)

*4: Pin = 26 dBm, 1710 MHz to 1990 MHz (Band 1 Tx, Band 2 Tx, Band 3 Tx, Band4 Tx)

*5: Pin = 10 dBm, 2110 MHz to 2170 MHz (Band 1 Rx, Band 4 Rx)

*6: Pin = 26 dBm, 2300 MHz to 2400 MHz (Band 40)

*7: Pin = 26 dBm, 2500 MHz to 2690 MHz (Band 7)

*8: Pin = 35 dBm, 824 MHz to 915 MHz (GSM850/900 Tx)

*9: Pin = 32 dBm, 1710 MHz to 1910 MHz (GSM1800/1900 Tx)

*10: Pin = 10 dBm, 869 MHz to 960 MHz (GSM850/900 Rx)

*11: Pin = 10 dBm, 1805 MHz to 1990 MHz (GSM1800/1900 Rx)

*12A: Measured with the recommended Circuit1, Circuit2

*12B: Measured with the recommended Circuit3

(*)Electrical characteristics are measured with all RF ports terminated in 50 Ω.

IMD Condition

Band	fRx on TRx	fRx +20 dBm on TRx	fBlocker –15 dBm on Ant		IMD Condition
Band I	2140 MHz	1950 MHz	IMD2 (fRx-fTx)	190 MHz	*13
			IMD2 (fRx-fTx)	4090 MHz	*14
			IMD3 (2fTx-fRx)	1760 MHz	*15
			IMD3 (2fTx-fRx)	6040 MHz	*16
Band II	1960 MHz	1880 MHz	IMD2 (fRx-fTx)	80 MHz	*17
			IMD2 (fRx-fTx)	3840 MHz	*18
			IMD3 (2fTx-fRx)	1800 MHz	*19
			IMD3 (2fTx-fRx)	5720 MHz	*20
Band V	880 MHz	835 MHz	IMD2 (fRx-fTx)	45 MHz	*21
			IMD2 (fRx-fTx)	1715 MHz	*22
			IMD3 (2fTx-fRx)	790 MHz	*23
			IMD3 (2fTx-fRx)	2550 MHz	*24

IIP3 Condition

Band	f1 +27 dBm on TRx	f2 +27 dBm on TRx	IIP3 Condition IIP3 = (3 × Pout – IM3)/2
Band I	1950 MHz	1951 MHz	*25
Band V	835 MHz	836 MHz	*26

Triple Beat Ratio

V_{DD} = 2.5 V, Vctl = 1.80 V, Ta = 25 °C

Item	Symbol	Path	Condition				Min.	Typ.	Max.	Unit
Triple Beat Ratio	TBR	-	Tx1 at TRx*1 21.5 dBm [MHz]	Tx2 at TRx*1 21.5 dBm [MHz]	Jammer at Ant –30 dBm [MHz]	Triple Beat Product at TRx*1 [MHz]	-	-	-	dBc
		Ant-TRx 1, 2, 3, 4, 5, 6, 7	835.5	836.5	881.5	881.5 ± 1	81	-	-	
			1880	1881	1960	1960 ± 1	81	-	-	

(*)Electrical characteristics are measured with all RF ports terminated in 50 Ω.
*12A:Measured with the recommended Circuit1, Circuit2

IIP2

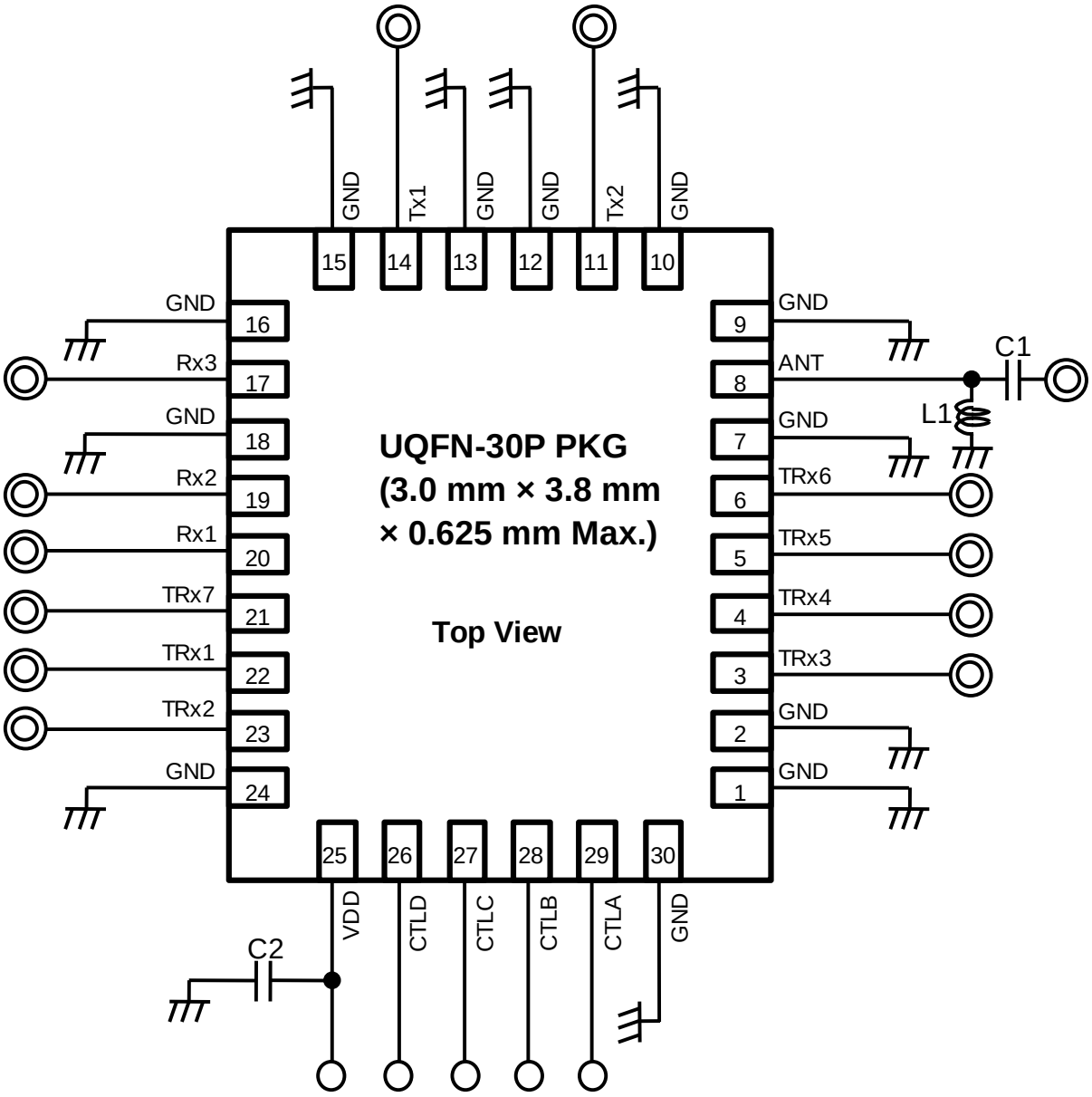
V_{DD} = 2.5 V, Vctl = 1.80 V, Ta = 25 °C

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
Input IP2	IIP2	-	Tx at TRx*1 24 dBm [MHz]	Jammer at Ant -20 dBm [MHz]	IM2 Product at TRx*1 [MHz]	-	-	-	dBm
		Ant - TRx 1, 2, 3, 4, 5, 6, 7	836.61	1718.61	881.61	113.5	-	-	
			836.61	45	881.61	95.5	-	-	
			1885	3850	1965	95.5	-	-	
			1885	80	1965	95.5	-	-	
			1732.5	3865	2132.5	95.5	-	-	
			1732.5	400	2132.5	95.5	-	-	

(*)Electrical characteristics are measured with all RF ports terminated in 50 Ω.
*12A:Measured with the recommended Circuit1, Circuit2

Recommended Circuit 1

Operation Frequency Range : 0.7 GHz to 2.7 GHz



*1: No DC blocking capacitors are required on all RF ports. (Except sourcing DC bias)

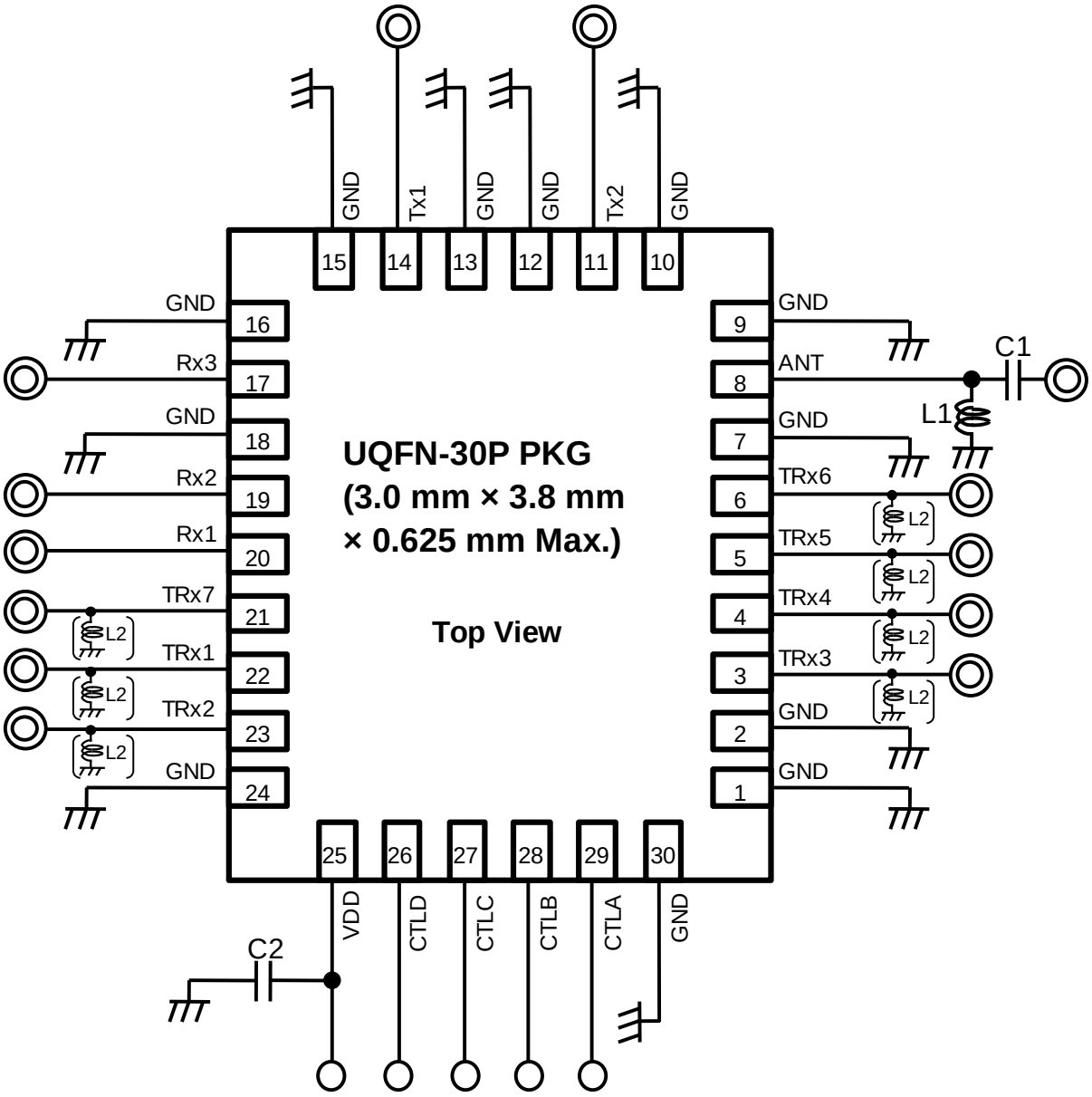
*2: DC levels of all RF ports are GND.

*3: L1 Inductor(22 nH) and C1 Capacitor(12 pF) are recommended on Ant port for ESD protection.

*4: C2 Capacitor(100 pF) is recommended.

Recommended Circuit 2

Operation Frequency Range : 0.45 GHz to 2.7 GHz



*1: No DC blocking capacitors are required on all RF ports. (Except sourcing DC bias)

*2: DC levels of all RF ports are GND.

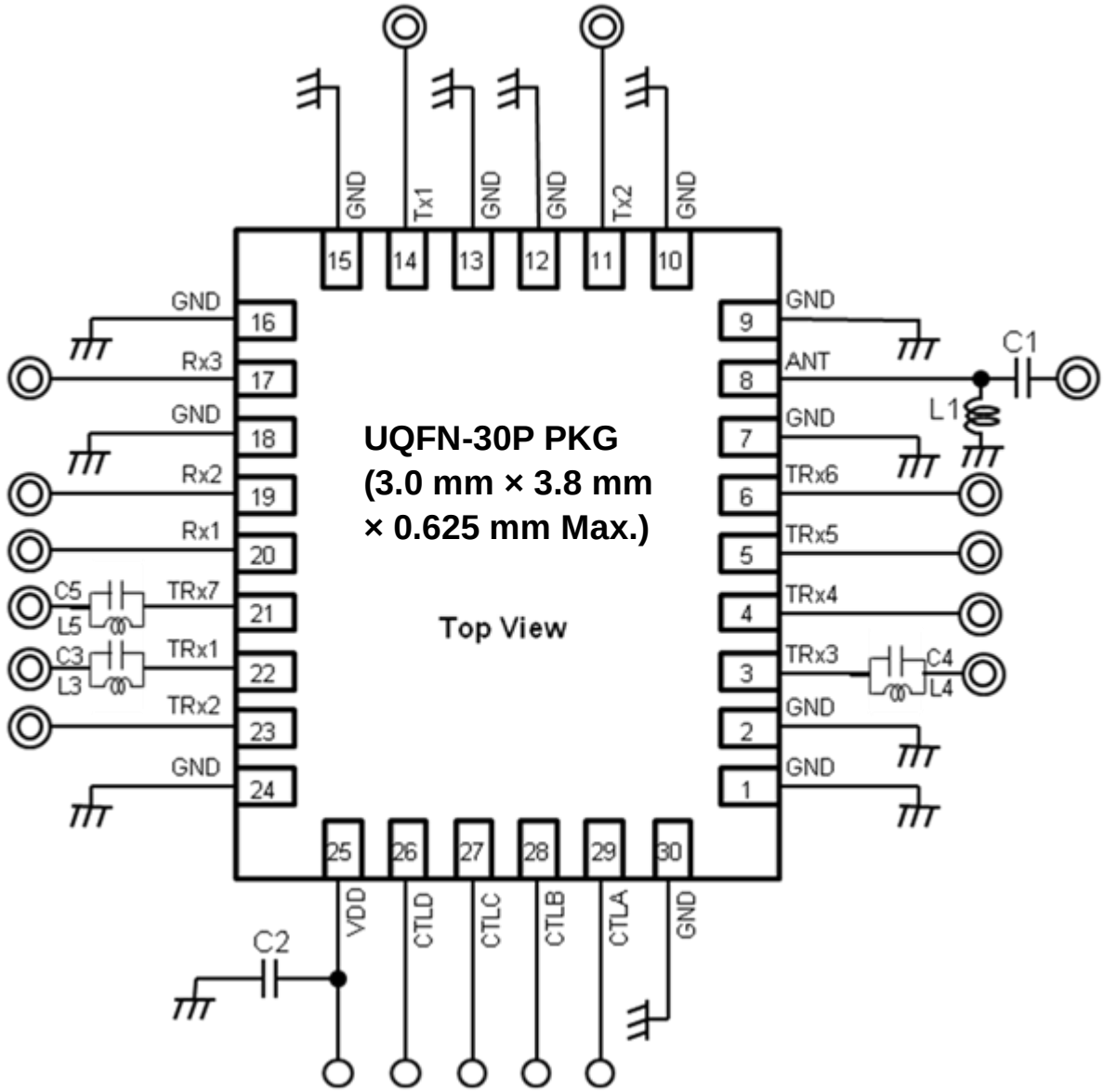
*3: L1 Inductor(47 nH) and C1 Capacitor(22 pF) are recommended on Ant port for ESD protection.

*4: L2 Inductor(12 nH) is recommended on a TRx port assigned for Band I to improve IMD2 performance(Rx-Tx(190 MHz)).

*5: C2 Capacitor(100 pF) is recommended.

Recommended Circuit 3

2nd Harmonic Improvement at LTE : Band13



*1: No DC blocking capacitors are required on all RF ports. (Except sourcing DC bias)

*2: DC levels of all RF ports are GND.

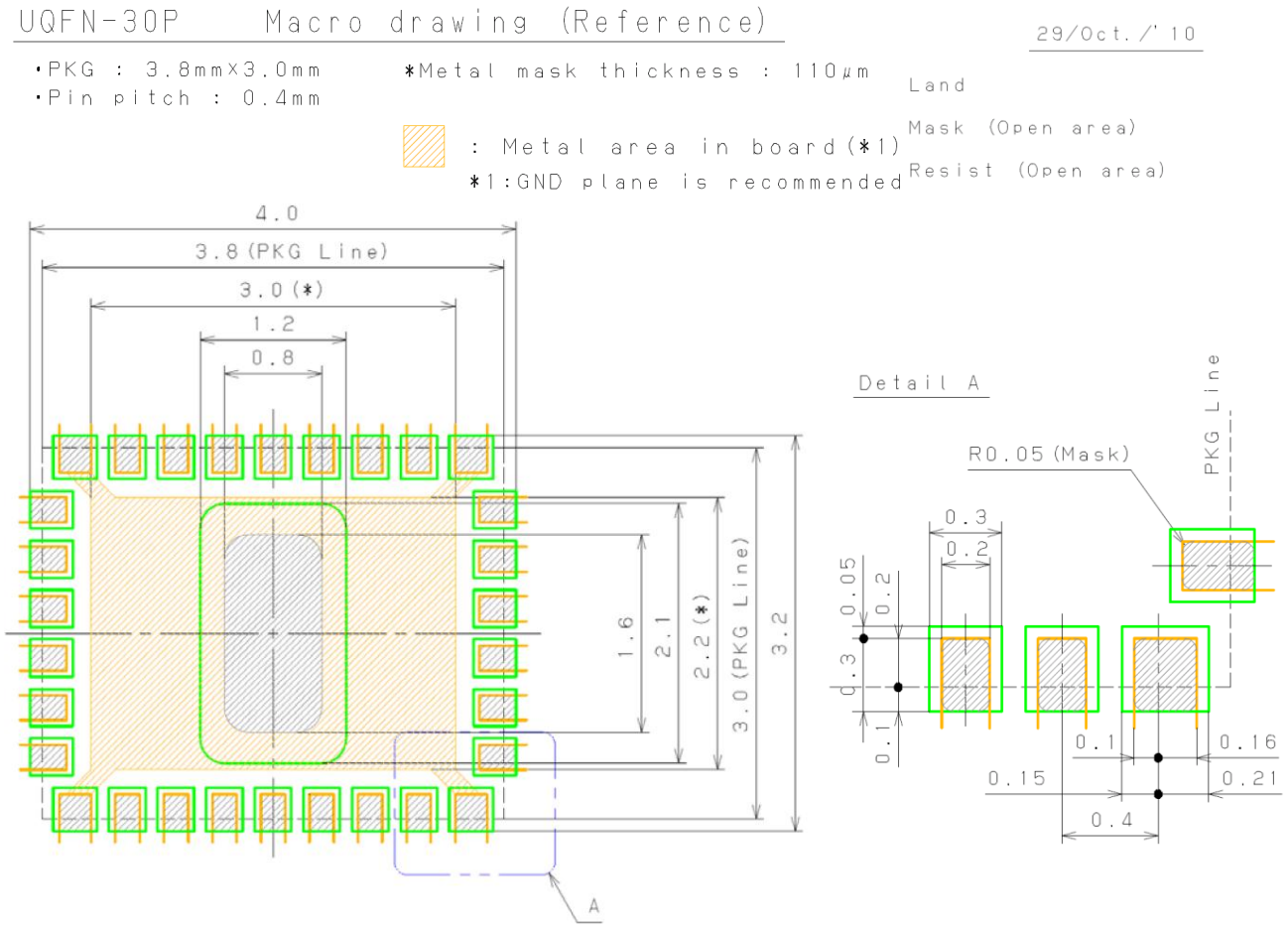
*3: L1 Inductor(22 nH) and C1 Capactor(12 pF) are recommended on Ant port for ESD protection.

*4: C2 Capacitor(100 pF) is recommended.

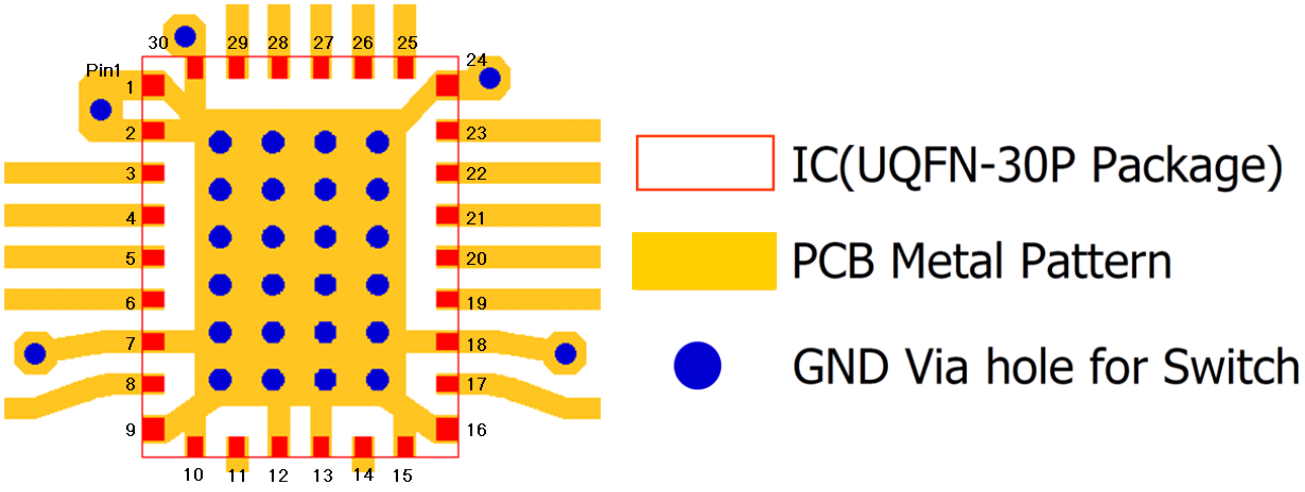
*5: L3 Inductor(1.8 nH) and C3 Capacitor(6.6 pF) are recommended when TRx1 is assigned for Band 13.
L4 Inductor(1.8 nH) and C4 Capacitor(7.8 pF) are recommended when TRx3 is assigned for Band 13.
L5 Inductor(1.8 nH) and C5 Capacitor(6.6 pF) are recommended when TRx7 is assigned for Band 13.

PCB Layout

Foot Pattern



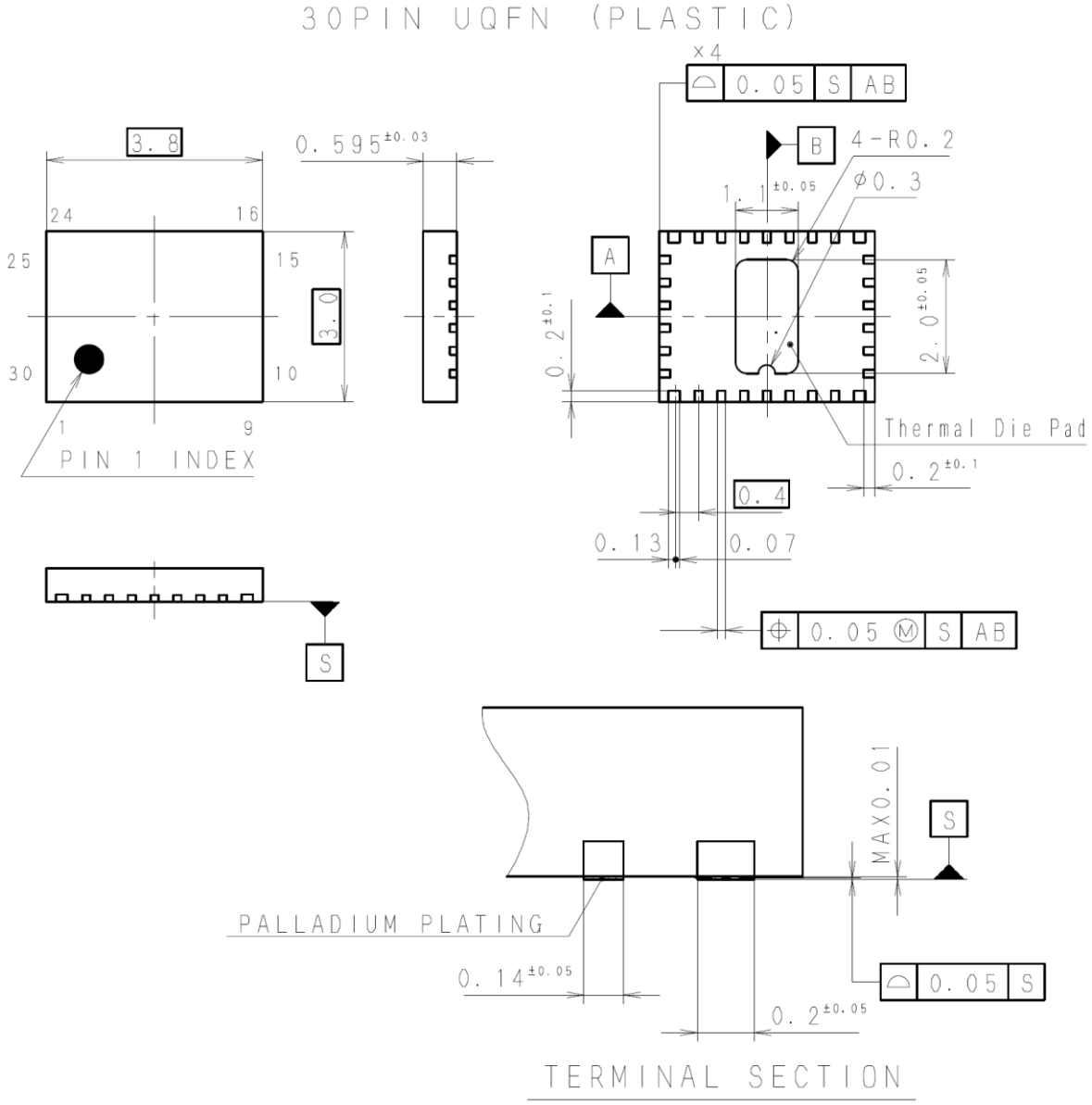
Recommended PCB Design



Package Outline

(Unit: mm)

Product Code : 875341512



Note:Terminal burr height 0.05mm MAX.

SONY CODE	UQFN-30P-541
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

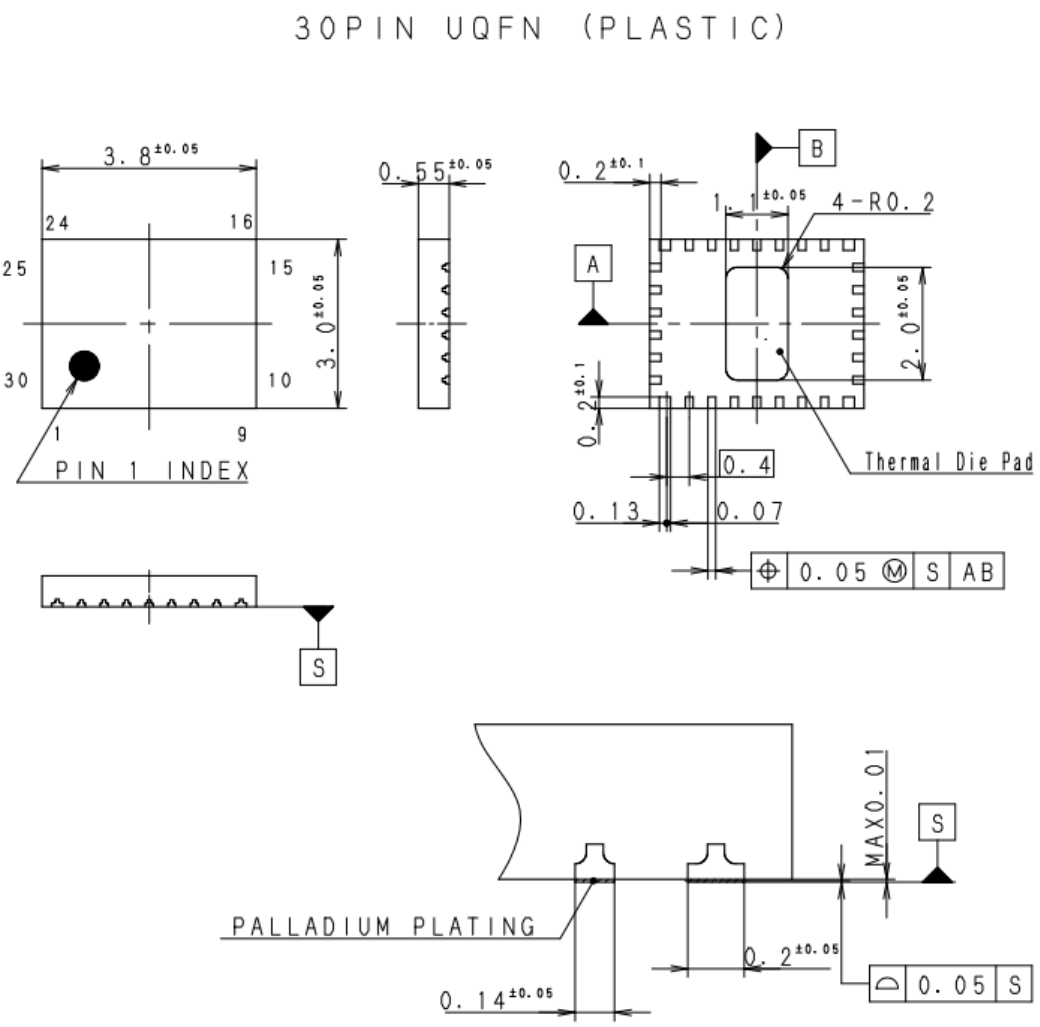
PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.017g

PART No. AP-2000-30QNBE2	Rev. 0
ISSUED '11.12.21	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR
REMARKS PKG CODE:UR-30-DBE	

Package Outline

(Unit: mm)

Product Code : 875342694



Note:Terminal burr height 0.05mm MAX.

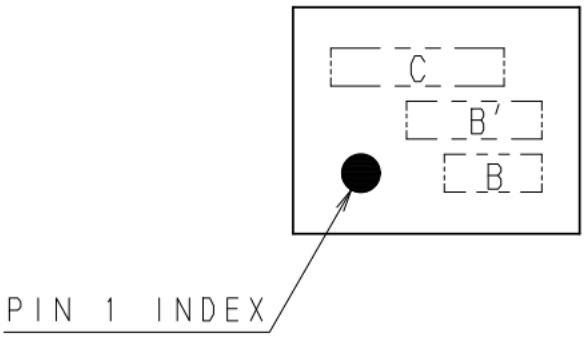
SONY CODE	UQFN-30P-01
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.017g

PART No. AP-4000-30015S	Rev. 0
ISSUED ' 12.08.31	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR
REMARKS PKG CODE:UR-30-J	

Marking



MARKING C: 3583A

注1) C部は製品名（Max5文字）を配置する。
（5文字を超える場合は製品名省略標示規定に従う。）
2) B, B' 部はロット番号（Max7文字）を配置する。
（但し B部Max3文字, B' 部Max4文字とする。規定文字数未満につき省略は省略規定に従う。）
3) 文字位置は、右詰めとする。

< INSTRUCTIONS >
1) TYPE NO. (MAX 5 CHARACTERS) IN SECTION C.
(FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) LOT NO. (MAX 7 CHARACTERS) IN SECTION B, B'.
(B: 3 CHARACTERS , B': 4 CHARACTERS. FOLL RULES FOR ABBREVIATIONS.)
3) PUT THE POSITION OF A CHARACTER REFERENCE FROM THE RIGHT SIDE.

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.