CY2CC810

1:10 Clock Fanout Buffer

Features

- Low-voltage operation
- V_{DD} range from 2.5 V to 3.3 V
- 1:10 fanout
- Over voltage tolerant input hot swappable
- Drives either a 50-Ohm or 75-Ohm transmission line
- Low-input capacitance
- 250 ps typical output-to-output skew
- 19 ps typical DJ jitter
- Typical propagation delay < 3.5 ns
- High-speed operation > 500 MHz
- Industrial temperature range
- Available packages include: SSOP

Description

The Cypress series of network circuits are produced using advanced 0.35-micron CMOS technology, achieving the industry's fastest logic and buffers.

The Cypress CY2CC810 fanout buffer features one input and ten outputs. Designed for data communications clock management applications, the large fanout from a single input reduces loading on the input clock.

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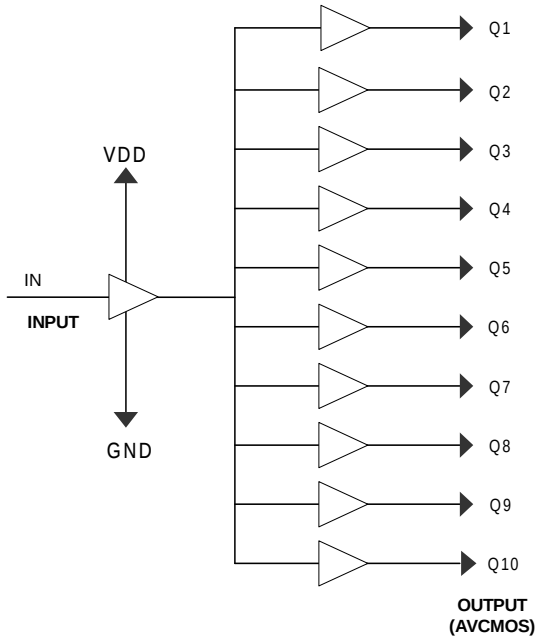
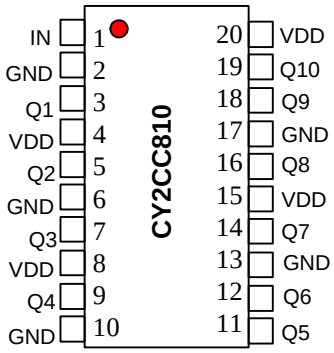
Block Diagram



Pin Configuration



20 pin SOIC/SSOP

Contents

Pin Description

Pin Number	Pin Name	Description	
1	IN	Input	LVCMOS
2, 6, 10, 13, 17	GND	Ground	Power
4, 8, 15, 20	V_{DD}	Power Supply	Power
3, 5, 7, 9, 11, 12, 14, 16, 18, 19	Q1... Q10	Output	AVCMOS

Absolute Maximum Conditions[1, 2]

Parameter	Description	Min	Max	Unit
V_{DD}	V_{DD} ground supply voltage	–0.5	4.6	V
V_{IN}	Input supply voltage to ground potential	–0.5	5.8	V
V_{OUT}	Output supply voltage to ground potential	–0.5	V_{DD} +1	V
T_S	Temperature, storage	–65	150	°C
T_A	Temperature, operating ambient	–40	85	°C
	Power dissipation	0.75		W

DC Electrical Characteristics @ 3.3 V (see Figure 5)

Parameter	Description	Conditions		Min	Typ.	Max	Unit
V_{OH}	Output high voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12 mA	2.3	3.3		V
V_{OL}	Output low voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA	–	0.2	0.5	V
V_{IH}	Input high voltage	Guaranteed Logic High Level	–	2	–	5.8	V
V_{IL}	Input low voltage	Guaranteed Logic Low Level	–	–	–	0.8	V
I_{IH}	Input high current	V_{DD} = Max	V_{IN} = 2.7 V	–	–	1	µA
I_{IL}	Input low current	V_{DD} = Max	V_{IN} = 0.5 V	–	–	–1	µA
I_I	Input high current	V_{DD} = Max, V_{IN} = V_{DD}(Max)	–	–	–	20	µA
V_{IK}	Clamp diode voltage	V_{DD} = Min, I_{IN} = –18 mA	–	–	–0.7	–1.2	V
I_{OK}	Continuous clamp current	V_{DD} = Max, V_{OUT} = GND	–	–	–	–50	mA
O_{OFF}	Power down disable	V_{DD} = GND, V_{OUT} = < 4.5 V	–	–	–	100	µA
V_H	Input hysteresis	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	–	–	80		mV

DC Electrical Characteristics @ 2.5 V (see Figure 1)

Parameter	Description	Conditions		Min	Typ.	Max	Unit
V_{OH}	Output high voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –7 mA	1.8	–	–	V
			I_{OH} = 12 mA	1.6	–	–	V
V_{OL}	Output low voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA		–	0.65	V
V_{IH}	Input high voltage	Guaranteed Logic High Level	–	1.6	–	5.0	V
V_{IL}	Input low voltage	Guaranteed Logic Low Level	–	–	–	0.8	V
I_{IH}	Input high current	V_{DD} = Max	V_{IN} = 2.4 bV	–	–	1	µA
I_{IL}	Input low current	V_{DD} = Max	V_{IN} = 0.5 V	–	–	–1	µA
I_I	Input high current	V_{DD} = Max, V_{IN} = V_{DD}(Max)	–	–	–	20	µA
V_{IK}	Clamp diode voltage	V_{DD} = Min, I_{IN} = –18 mA	–	–	–0.7	–1.2	V
I_{OK}	Continuous clamp current	V_{DD} = Max, V_{OUT} = GND	–	–	–	–50	mA
O_{OFF}	Power-down disable	V_{DD} = GND, V_{OUT} = < 4.5 V	–	–	–	100	µA
V_H	Input hysteresis	–	–	–	80	–	mV

Capacitance

Parameter	Description	Test Conditions	Min	Typ.	Max	Unit
Cin	Input capacitance	V_{IN} = 0 V	–	2.5	–	pF
Cout	Output capacitance	V_{OUT} = 0 V	–	6.5	–	pF

Power Supply Characteristics (see Figure 5)

Parameter	Description	Test Conditions	Min	Typ.	Max	Unit
Δ_{ICC}	Delta I_{CC} quiescent power supply current	(I_{DD} @ V_{DD} = Max and V_{IN} = V_{DD}) – (I_{DD} @ V_{DD} = Max and V_{IN} = V_{DD} – 0.6 V)	–	–	50	µA
I_{CCD}	Dynamic power supply current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open	–		0.63	mA/ MHz
I_C	Total power supply current	V_{DD} = Max Input toggling 50% Duty Cycle, Outputs Open fL = 40 MHZ	–	–	25	mA
t_{PU}	Power-up time for all V_{DD}s	Power-up to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms

High-frequency Parametrics

Parameter	Description	Test Conditions		Min	Typ.	Max	Unit
D_J	Jitter, Deterministic	50% duty cycle t_W(50–50) The “point to point load circuit” Output Jitter – Input Jitter	2.5 V	–	23	35	ps
			3.3 V	–	19	30	ps
$F_{max(3.3\ V)}$	Maximum frequency V_{DD} = 3.3 V	50% duty cycle t_W(50–50) Standard Load Circuit.	See Figure 5	–	–	160	MHz
		50% duty cycle t_W(50–50) The “point to point load circuit”	See Figure 7	–	–	650	
$F_{max(2.5\ V}$	Maximum frequency V_{DD} = 2.5 V	The “point to point load circuit” V_{IN} = 2.4 bV/0.0 V V_{OUT} = 1.7 V/0.7 V	See Figure 7	–	–	200	MHz
$F_{max(20)}$	Maximum frequency V_{DD} = 3.3 V	20% duty cycle t_W(20–80) The “point to point load circuit” V_{IN} = 3.0 V/0.0 V V_{OUT} = 2.3 V/0.4 bV	See Figure 7	–	–	250	MHz
	Maximum frequency V_{DD} = 2.5 V	The “point to point load circuit” V_{IN} = 2.4 bV/0.0 V V_{OUT} = 1.7 V/0.7 V	See Figure 3	–	–	200	MHz
t_W	Minimum pulse V_{DD} = 3.3 V	The “point to point load circuit” V_{IN} = 3.0 V/0.0 V F = 100 MHz V_{OUT} = 2.0 V/0.8 V	See Figure 7	1	–	–	ns
	Minimum pulse V_{DD} = 2.5 V	The “point to point load circuit” V_{IN} = 2.4 bV/0.0 V F = 100 MHz V_{OUT} = 1.7 V/0.7 V	See Figure 3	1	–	–	

Note

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

AC Switching Characteristics @ 3.3 V, V_{DD} = 3.3 V ±5%, Temperature = –40 °C to +85°C

Parameter	Description		Min	Typ.	Max	Unit
t_{PLH}	Propagation delay – Low to High	See Figure 4	1.5	2.7	3.5	ns
t_{PHL}	Propagation delay – High to Low		1.5	2.7	3.5	ns
t_R	Output rise time	–	–	0.8		V/ns
t_F	Output fall time	–	–	0.8		V/ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)	See Figure 10	–	0.25	0.38	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} – t_{PLH}$).	See Figure 9	–	–	0.2	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See Figure 11	–	–	0.42	ns

AC Switching Characteristics @ 2.5 V, V_{DD} = 2.5 V ±5%, Temperature = –40 °C to +85 °C

Parameter	Description		Min	Typ.	Max	Unit
t_{PLH}	Propagation delay – Low to High	See Figure 4	1.5	2.0	3.5	ns
t_{PHL}	Propagation delay – High to Low		1.5	2.0	3.5	ns
t_R	Output rise time	–	–	0.8		V/ns
t_F	Output fall time	–	–	0.8		V/ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)	See Figure 10	–	0.25	0.38	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} – t_{PLH}$).	See Figure 9	–	–	0.4	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See Figure 11	–		0.65	ns

Parameter Measurement Information: V_{DD} @ 2.5 V

Figure 1. Load Circuit [3,4,5]

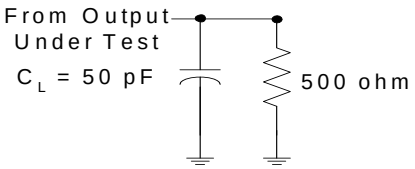
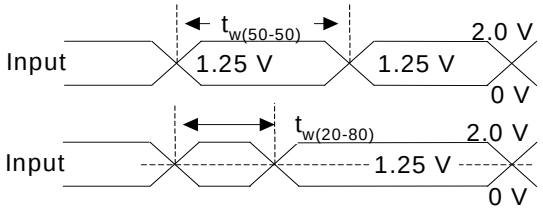


Figure 2. Voltage Waveforms Pulse Duration[6]



Notes
3. C_L includes probe and jig capacitance.
4. All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz, Z_0 = 50W, t_R < 2.5 nS, t_F < 2.5 nS.
5. The outputs are measured one at a time with one transition per measurement.
6. T_{PLH} and T_{PHL} are the same as t_{pd}..

Figure 3. Point to Point Load Circuit[3,4,5]

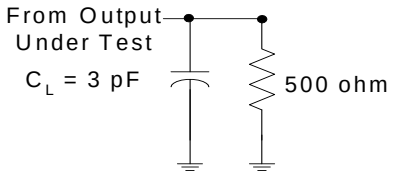
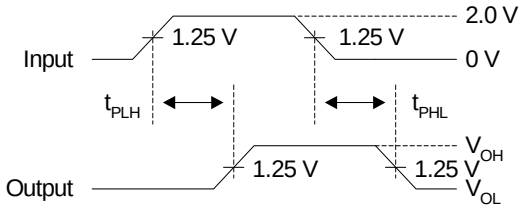


Figure 4. Voltage WaveformsPropagation Delay Times[4]



Parameter Measurement Information: V_{DD} @ 3.3 V

Figure 5. Load Circuit [3,4,5]

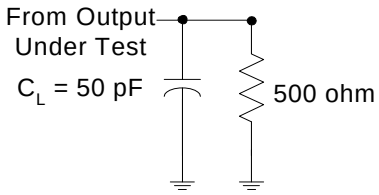


Figure 6. Voltage Waveforms–Pulse Duration[6]

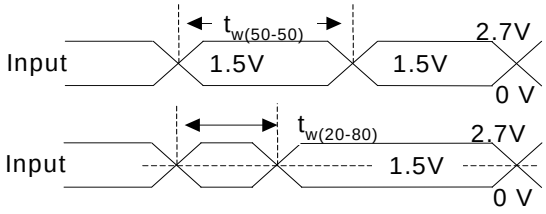


Figure 7. Point to Point Load Circuit[3,4,5]

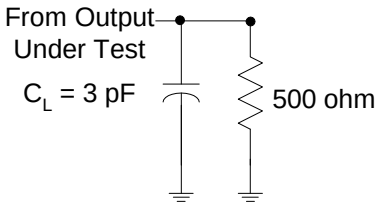


Figure 8. Voltage Waveforms Propagation Delay Times[4]

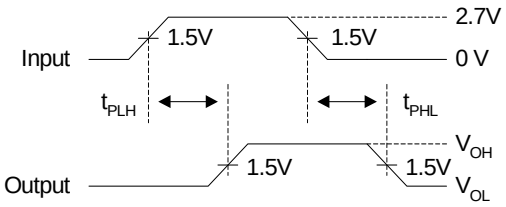
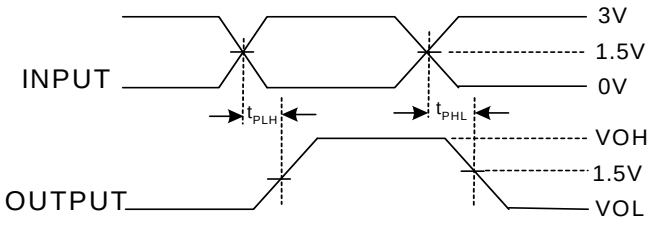
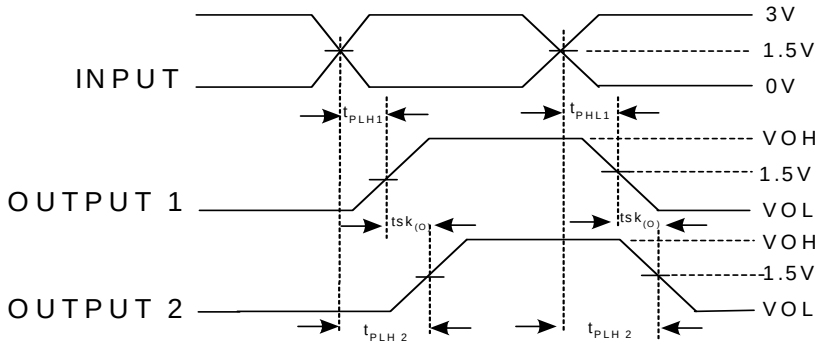


Figure 9. Pulse Skew–$tsk_{(p)}$



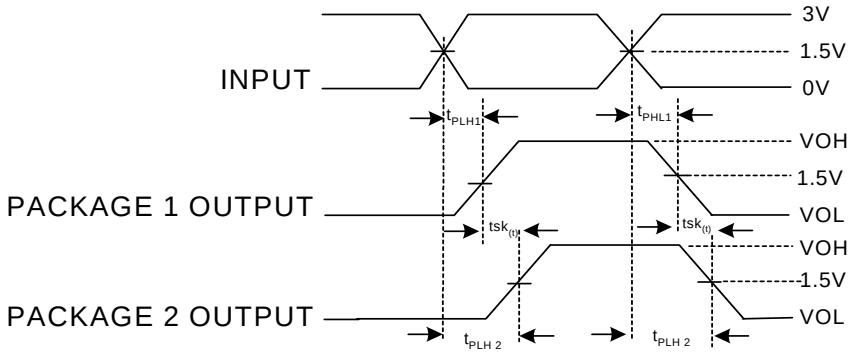
$$tsk_{(P)} = | t_{PHL} - t_{PLH} |$$

Figure 10. Output Skew–$tsk_{(0)}$



$$tsk_{(P)} = | t_{PLH2} - t_{PLH1} | \text{ or } t_{PHL2} - t_{PHL1} |$$

Figure 11. Package Skew–$tsk_{(t)}$

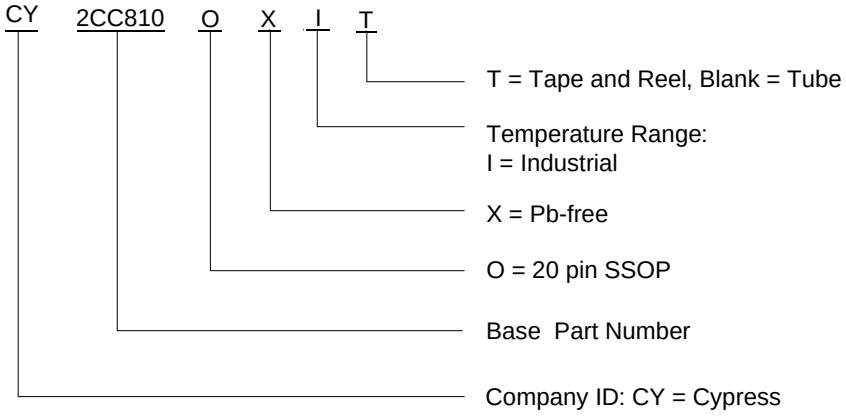


$$tsk_{(t)} = | t_{PLH2} - t_{PLH1} | \text{ or } t_{PHL2} - t_{PHL1} |$$

Ordering Information

Part Number[7]	Package Type	Product Flow
Pb-free		
CY2CC810OXI	20-pin SSOP	Industrial, –40 °C to 85 °C
CY2CC810OXIT	20-pin SSOP–Tape and Reel	Industrial, –40 °C to 85 °C
CY2CC810OXI-1	20-pin SSOP	Industrial, –40 °C to 85 °C
CY2CC810OXI-1T	20-pin SSOP–Tape and Reel	Industrial, –40 °C to 85 °C

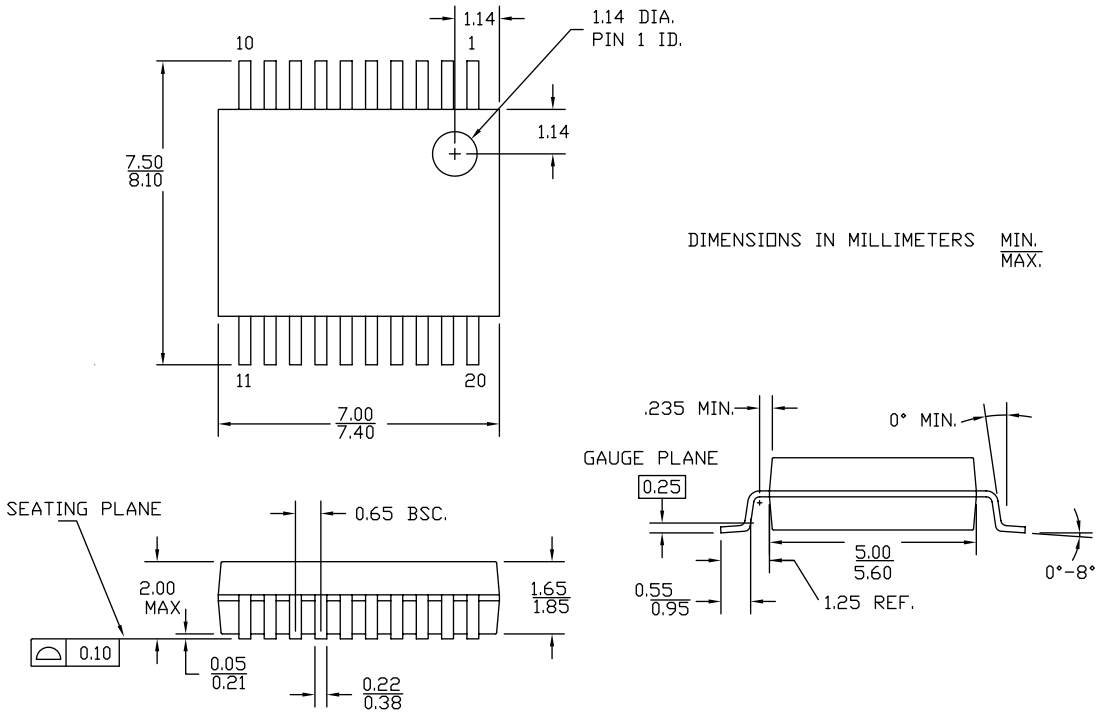
Ordering Code Definitions



Note
7. Devices with part numbers ending with -1 are identical to devices without the -1 suffix. There are no differences in specification.

Package Drawing and Dimensions

Figure 12. 20-Pin (5.3-mm) Shrunk Small Outline Package O20



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Acronym

Acronym	Description
CMOS	complementary metal oxide semiconductor
DJ	Deterministic Jitter
SSOP	shrunk small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHZ	megahertz
uA	microamperes
mA	milliamperes
ms	milliseconds
ns	nanoseconds
%	percent
pF	picofarads
ps	picoseconds
V	volt

Document History Page

Document Title: CY2CC810 1:10 Clock Fanout Buffer Document #: 38-07056				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	107081	06/07/01	IKA	Convert from IMI to Cypress
*A	114315	05/09/02	TSM	ΔI_{DD} Validation
*B	119117	10/07/02	RGL	Added 5.8 as the Max value of V_{IH} in the DC Electrical Characteristics @3.3 V table. Changed the Max value of V_{IH} from 1.8 to 5.0 in the DC Electrical Characteristics @2.5 V table.
*C	122743	12/14/02	RBI	Added power up requirements to maximum ratings information.
*D	387761	See ECN	RGL	Added typical values Updated jitter and skew specs. Removed devices with SOIC package Added Lead-free SSOP package
*E	499991	See ECN	RGL	Added tpu parameter in the Power Supply Characteristics table
*F	2896073	03/19/10	CXQ	Updated package diagram Removed obsolete parts from ordering information table and added CY2CC810OXI-1, CY2CC810OXI-1T Removed reference to SOIC packages
*G	3056154	10/08/2010	CXQ	Removed CY2CC810OXC and CY2CC810OXCT parts from Ordering Information.
*H	3396159	10/10/2011	PURU	Added Contents Updated Description Updated Package Drawing and Dimensions Added Ordering Code Definitions, Acronym, and Units of Measure. The statement related to Variable impedance "AVCMOS-type outputs dynamically adjust for variable impedance matching and reduce noise overall" was removed.

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