CY2DL1504

1:4 Differential LVDS Fanout Buffer with Selectable Clock Input

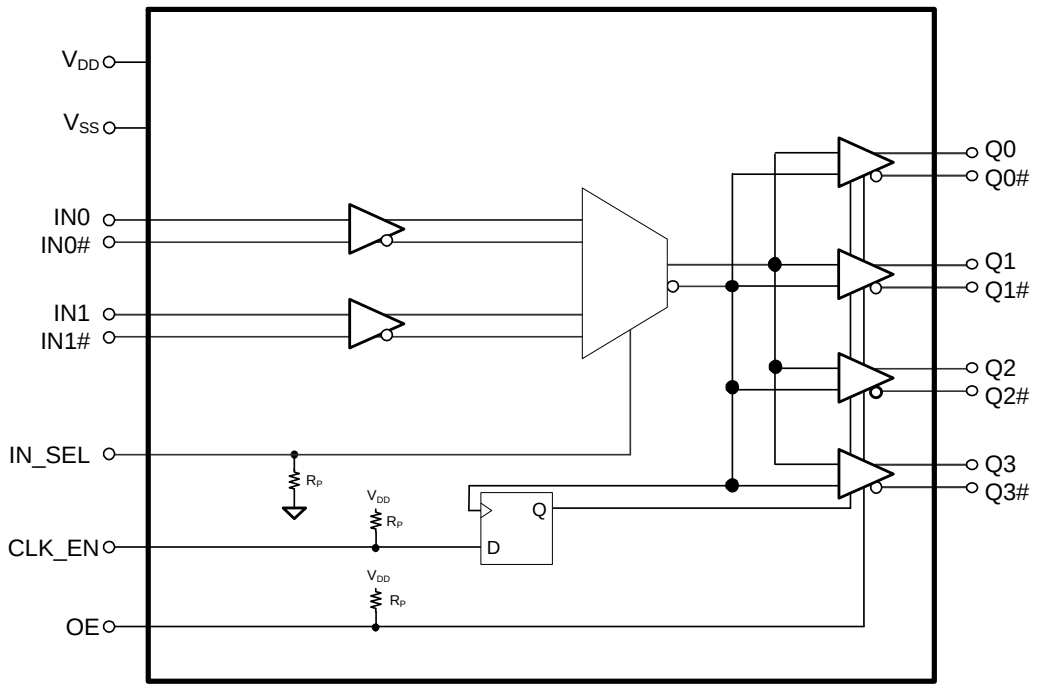
Features

- Select one of two differential (LVPECL, LVDS, HCSL, or CML) input pairs to distribute to four LVDS output pairs
- 30-ps maximum output-to-output skew
- 480-ps maximum propagation delay
- 0.11-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 1.5-GHz operation
- Output enable and synchronous clock enable functions
- 20-pin TSSOP
- 2.5-V or 3.3-V operating voltage[1]
- Commercial and industrial operating temperature range

Functional Description

The CY2DL1504 is an ultra-low noise, low-skew, low-propagation delay 1:4 differential LVDS fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The CY2DL1504 can select between two separate differential (LVPECL, LVDS, HCSL, or CML) input clock pairs using the IN_SEL pin. The synchronous clock enable function ensures glitch-free output transitions during enable and disable periods. The output enable function allows the outputs to be asynchronously driven to a high-impedance state. The device has a fully differential internal architecture that is optimized to achieve low-additive jitter and low-skew at operating frequencies of up to 1.5 GHz.

Logic Block Diagram



Note
1. Input AC-coupling capacitors are required for voltage-translation applications.

Contents

Pinouts

Figure 1. Pin Diagram – CY2DL1504 20-Pin TSSOP Package

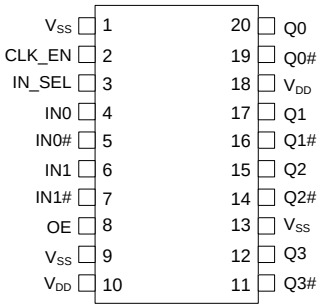


Table 1. Pin Definitions

Pin No.	Pin Name	Pin Type	Description
1,9,13	V_{SS}	Power	Ground
2	CLK_EN	Input	Synchronous clock enable. LVCMOS/LVTTL; When CLK_EN = Low, Q(0:3) outputs are held low and Q(0:3)# outputs are held high
3	IN_SEL	Input	Input clock select pin. LVCMOS/LVTTL; When IN_SEL = Low, the IN0/IN0# differential input pair is active When IN_SEL = High, the IN1/IN1# differential input pair is active
4	IN0	Input	Differential (LVPECL, HCSL, LVDS, or CML) input clock. Active when IN_SEL = Low
5	IN0#	Input	Differential (LVPECL, HCSL, LVDS, or CML) complementary input clock. Active when IN_SEL = Low
6	IN1	Input	Differential (LVPECL, HCSL, LVDS, or CML) input clock. Active when IN_SEL = High
7	IN1#	Input	Differential (LVPECL, HCSL, LVDS, or CML) complementary input clock. Active when IN_SEL = High
8	OE	Input	Output enable. LVCMOS/LVTTL; When OE = Low, Q(0:3) and Q(0:3)# outputs are disabled (see I_{OZ})
10,18	V_{DD}	Power	Power supply
11,14,16,19	Q(0:3)#	Output	LVDS complementary output clocks
12,15,17,20	Q(0:3)	Output	LVDS output clocks

Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	Nonfunctional	–0.5	4.6	V
V_{IN}[2]	Input voltage, relative to V_{SS}	Nonfunctional	–0.5	Lesser of 4.0 or V_{DD} + 0.4	V
V_{OUT}[2]	DC output or I/O voltage, relative to V_{SS}	Nonfunctional	–0.5	Lesser of 4.0 or V_{DD} + 0.4	V
T_S	Storage temperature	Nonfunctional	–55	150	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	–	V
L_U	Latch up		Meets or exceeds JEDEC Spec JESD78B IC latch up test		
UL–94	Flammability rating	At 1/8 in.	V–0		
MSL	Moisture sensitivity level		3		

Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.5-V supply	2.375	2.625	V
		3.3-V supply	3.135	3.465	V
T_A	Ambient operating temperature	Commercial	0	70	°C
		Industrial	–40	85	°C
t_{PU}	Power ramp time	Power-up time for V_{DD} to reach minimum specified voltage. (Power ramp must be monotonic)	0.05	500	ms

Note
2. The voltage on any I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

DC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Max	Unit
I_{DD}	Operating supply current	All LVDS outputs terminated with a load of 100 Ω[3, 4]	–	61	mA
V_{IH1}	Input high voltage, differential input clocks, IN0, IN0#, IN1, and IN1#		–	V_{DD} + 0.3	V
V_{IL1}	Input low voltage, differential input clocks, IN0, IN0#, IN1, and IN1#		–0.3	–	V
V_{IH2}	Input high voltage, CLK_EN, IN_SEL, and OE	V_{DD} = 3.3 V	2.0	V_{DD} + 0.3	V
V_{IL2}	Input low voltage, CLK_EN, IN_SEL, and OE	V_{DD} = 3.3 V	–0.3	0.8	V
V_{IH3}	Input high voltage, CLK_EN, IN_SEL, and OE	V_{DD} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL3}	Input low voltage, CLK_EN, IN_SEL, and OE	V_{DD} = 2.5 V	–0.3	0.7	V
V_{ID_LVDS}[5]	LVDS input differential amplitude	See Figure 3 on page 7	0.4	0.8	V
V_{ID_LVPECL}[5]	LVPECL/CML/HCSL input differential amplitude	See Figure 3 on page 7	0.4	1.0	V
V_{ICM}	Input common mode voltage	See Figure 3 on page 7	0.2	V_{DD} – 0.2	V
I_{IH}	Input high current, All inputs	Input = V_{DD}[6]	–	150	µA
I_{IL}	Input low current, All inputs	Input = V_{SS}[6]	–150	–	µA
V_{PP}	LVDS differential output voltage peak to Peak, Single-ended	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between Q and Q# pairs[3, 7]	250	470	mV
V_{OCM}	LVDS differential output common mode voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between Q and Q# pairs[3, 7]	1.125	1.375	V
ΔV_{OCM}	Change in V_{OCM} between complementary output states	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between Q and Q# pairs[3, 7]	–	50	mV
I_{OZ}	Output leakage current	OE = V_{SS}, V_{OUT} = 0.75V – 1.75V	–15	15	µA
R_P	Internal pull-up/pull-down resistance, LVCMOS logic inputs	CLK_EN has pull-up only IN_SEL has pull-down only OE has pull-up only	60	165	kΩ
C_{IN}	Input capacitance	Measured at 10 MHz; per pin	–	3	pF

Notes
3. Refer to Figure 2 on page 7.
4. I_{DD} includes current that is dissipated externally in the output termination resistors.
5. V_{ID} minimum of 400 mV is required to meet all output AC Electrical Specifications. The device is functional with V_{ID} minimum of greater than 200 mV.
6. Positive current flows into the input pin, negative current flows out of the input pin.
7. Refer to Figure 4 on page 7.

AC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{IN}	Input frequency		DC	–	1.5	GHz
F_{OUT}	Output frequency	$F_{OUT} = F_{IN}$	DC	–	1.5	GHz
t_{PD}[8]	Propagation delay input pair to output pair	Input rise/fall time < 1.5 ns (20% to 80%)	–	–	480	ps
t_{ODC}[9]	Output duty cycle	Diff input at 50% duty cycle Frequency range up to 1 GHz	48	–	52	%
t_{SK1}[10]	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	30	ps
$t_{SK1\ D}$[10]	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
PN_{ADD}	Additive RMS phase noise 156.25 MHz Input Rise/fall time < 150 ps (20% to 80%) V_{ID} > 400 mV	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–135	dBc/Hz
		Offset = 100 kHz	–	–	–135	dBc/Hz
		Offset = 1 MHz	–	–	–150	dBc/Hz
		Offset = 10 MHz	–	–	–154	dBc/Hz
		Offset = 20 MHz	–	–	–155	dBc/Hz
t_{JIT}[11]	Additive RMS phase jitter (Random)	156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV	–	–	0.11	ps
t_R, t_F[12]	Output rise/fall time, single-ended	50% duty cycle at input, 20% to 80% of full swing (V_{OL} to V_{OH}) Input rise/fall time < 1.5 ns (20% to 80%) Measured at 1 GHz.	–	–	300	ps
t_{SOD}	Time from clock edge to outputs disabled	Synchronous clock enable (CLK_EN) switched low	–	–	700	ps
t_{SOE}	Time from clock edge to outputs enabled	Synchronous clock enable (CLK_EN) switched high	–	–	700	ps

Notes
8. Refer to Figure 5 on page 7.
9. Refer to Figure 6 on page 7.
10. Refer to Figure 7 on page 8.
11. Refer to Figure 8 on page 8.
12. Refer to Figure 9 on page 8.

Figure 2. LVDS Output Termination

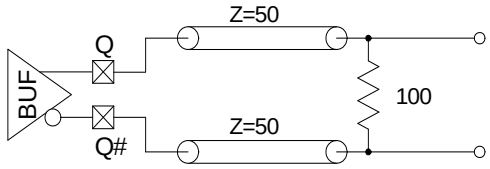


Figure 3. Input Differential and Common Mode Voltages

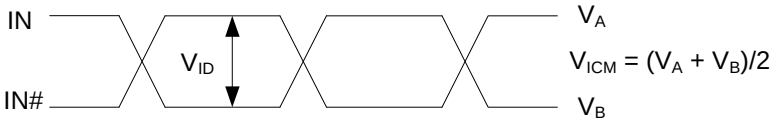


Figure 4. Output Differential and Common Mode Voltages

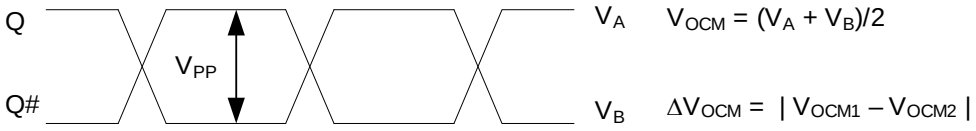


Figure 5. Input to Any Output Pair Propagation Delay

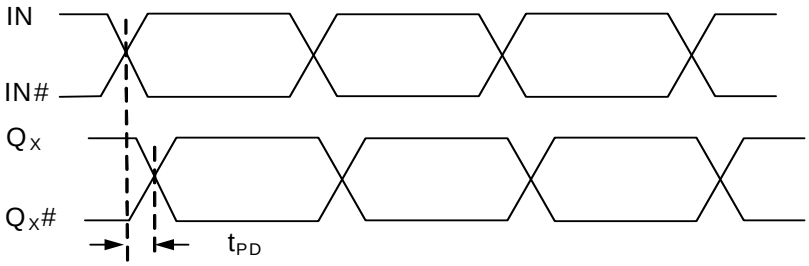


Figure 6. Output Duty Cycle

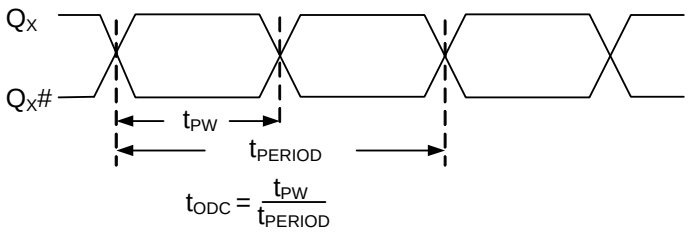


Figure 7. Output-to-output and Device-to-device Skew

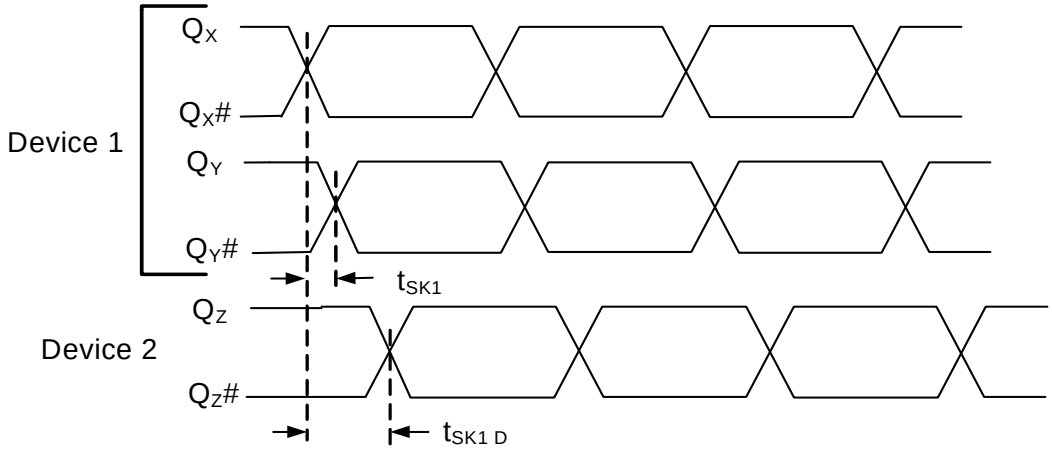


Figure 8. RMS Phase Jitter

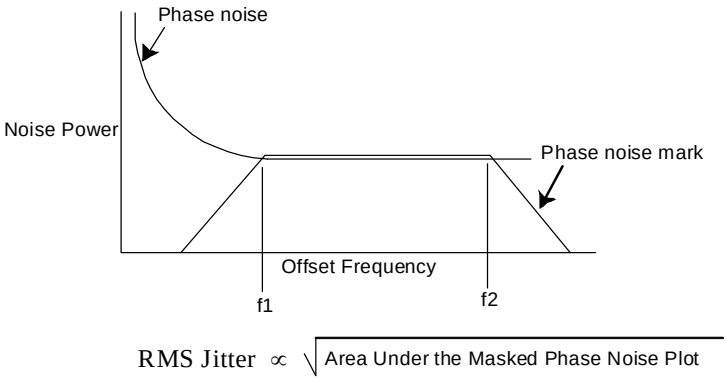


Figure 9. Output Rise/Fall Time

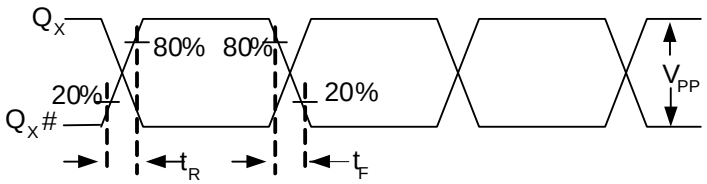
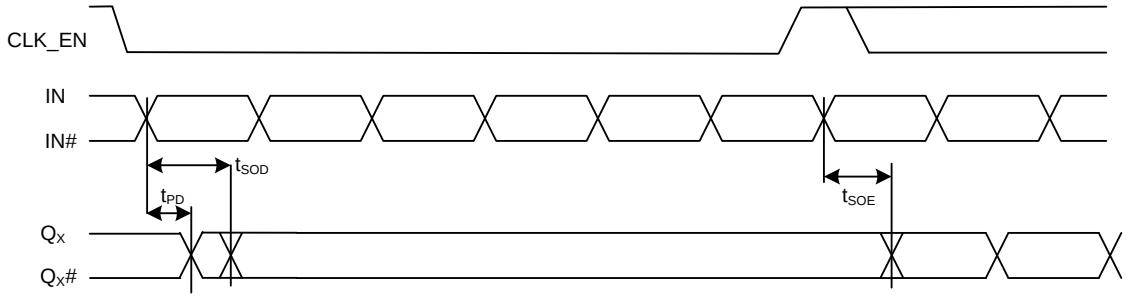


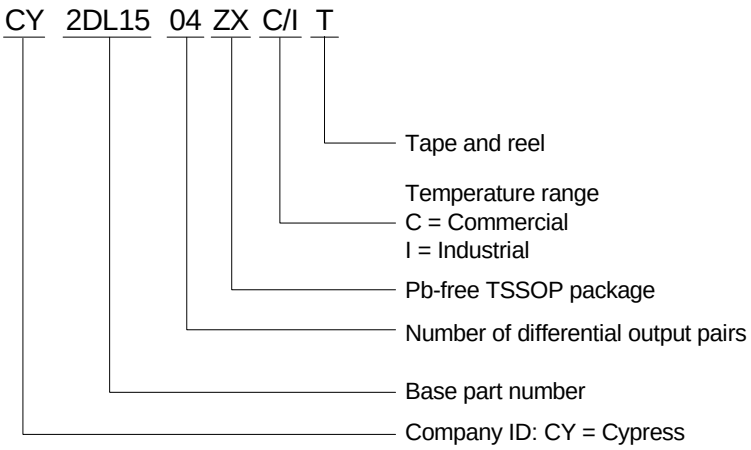
Figure 10. Synchronous Clock Enable Timing



Ordering Information

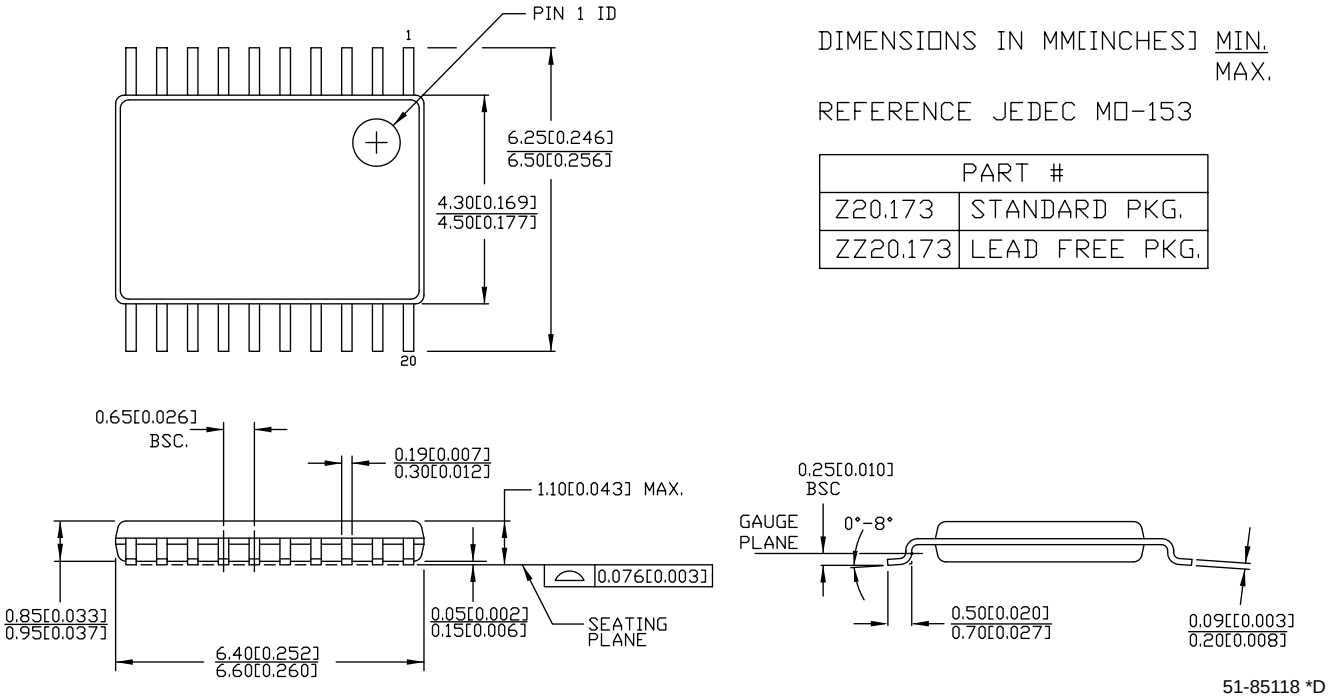
Part Number	Type	Production Flow
Pb-free		
CY2DL1504ZXC	20-Pin TSSOP	Commercial, 0 °C to 70 °C
CY2DL1504ZXCT	20-Pin TSSOP	Commercial, 0 °C to 70 °C
CY2DL1504ZXI	20-Pin TSSOP	Industrial, –40 °C to 85 °C
CY2DL1504ZXIT	20-Pin TSSOP	Industrial, –40 °C to 85 °C

Ordering Code Definitions



Package Diagram

Figure 11. 20-Pin Thin Shrunk Small Outline Package (4.40 mm Body) ZZ20



Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
ESD	Electrostatic discharge
HBM	Human body model
HCSL	high-speed current steering logic
JEDEC	Joint electron devices engineering council
LVDS	Low-voltage differential signal
LVCMOS	Low-voltage complementary metal oxide semiconductor
LVPECL	Low-voltage positive emitter-coupled logic
LVTTL	Low-voltage transistor-transistor logic
OE	Output enable
RMS	Root mean square
TSSOP	Thin shrunk small outline package

Document Conventions

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	giga hertz
Hz	hertz
kΩ	kilo ohm
µA	micro ampere
µF	micro Farad
µs	micro second
mA	milliamperes
ms	millisecond
mV	millivolt
MHz	megahertz
ns	nano second
Ω	ohm
pF	pico Farad
ps	pico second
V	volt
W	watt

Document History Page

Document Title: CY2DL1504 1:4 Differential LVDS Fanout Buffer with Selectable Clock Input Document Number: 001-56312				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2782891	CXQ	10/09/09	New Datasheet.
*A	2838613	CXQ	01/05/2010	Changed status from “ADVANCE” to “PRELIMINARY”. Changed from 0.34 ps to 0.25 ps maximum additive jitter in “Features” on page 1 and in t_{JIT} in the AC Electrical Specs table on page 5. Added t_{PU} spec to the Operating Conditions table on page 3. Changed max I_{DD} spec in the DC Electrical Specs table on page 4 from 60 mA to 61 mA. Removed V_{OD} and ΔV_{OD} specs from the DC Electrical Specs table on page 4. Changed I_{OZ} in the DC Electrical Specs table on page 4 from min of -10 uA to -15 uA and from max of 10 uA to 15 uA. Added R_P spec in the DC Electrical Specs table on page 4. Min = 60 kΩ, Max = 140 kΩ. Added a measurement definition for C_{IN} in the DC Electrical Specs table on page 4. Added V_{PP} and ΔV_{PP} specs to the AC Electrical Specs table on page 5. V_{PP} min = 250 mV and max = 470 mV; ΔV_{PP} max = 50 mV. Changed letter case and some names of all the timing parameters in the AC Electrical Specs table on page 5 to be consistent with EROS. Lowered all additive phase noise mask specs by 3 dB in the AC Electrical Specs table on page 5. Added condition to t_R and t_F specs in the AC Electrical specs table on page 5 that input rise/fall time must be less than 1.5 ns (20% to 80%). Changed letter case and some names of all the timing parameters in Figures 4, 5, 6, 7 and 9, to be consistent with EROS. Updated Figure 4 with definition for V_{PP} and ΔV_{PP}.
*B	3010332	CXQ	08/18/2010	Changed from 0.25 ps to 0.11 ps maximum additive jitter in “Features” on page 1 and in t_{JIT} in the AC Electrical Specs table on page 5. Added “Functional equivalent to ICS8543i” to the “Features” section. Changed pin 13 in Figure 1 and Table 1 from V_{DD} to V_{SS}. Changed pin 8 description in Table 1 from “high impedance” to “disabled”. Added note 6 to describe I_{IH} and I_{IL} specs. Removed reference to data distribution from “Functional Description”. Changed R_P for diff inputs from 100 kΩ to 150 kΩ in the Logic Block Diagram and from 60 kΩ min / 140 kΩ max to 90 kΩ min / 210 kΩ max in the DC Electrical Specs table. Split V_{ID} into separate specs in DC Electrical Specs table: 0.4 V min and 0.8 V max for LVDS, 0.4 V min and 1.0 V max for LVPECL. Updated phase noise specs for 1 k/10 k/100 k/1 M/10 M/20 MHz offset to -120/-130/-135/-150/-150/-150dBc/Hz, respectively, in the AC Electrical Specs table. Added “Frequency range up to 1 GHz” condition to t_{ODC} spec. Changed t_{OD} in the AC Electrical Specs table from 3 ns max to 5 ns max. Added Acronyms and Ordering Code Definition.
*C	3090644	CXQ	11/19/2010	Changed V_{IN} and V_{OUT} specs from 4.0V to “lesser of 4.0 or V_{DD} + 0.4” Removed 200mA min LU spec, replaced with “Meets or exceeds JEDEC Spec JESD78B IC Latchup Test” Added “V_{OUT} = 0.75V - 1.75V” to I_{OZ} comments. Moved V_{PP} from AC spec table to DC spec table, removed ΔV_{PP}. Removed R_P spec for differential input clock pins IN_X and IN_X#. Changed C_{IN} condition to “Measured at 10 MHz”. Changed PN_{ADD} specs for 10kHz, 10MHz, and 20MHz offsets. Added “Measured at 1 GHz” to t_R, t_F spec condition. Removed specs t_S, t_H, t_{OD}, and t_{OE} from AC spec table. Removed ΔV_{PP} reference from Figure 4.

Document Title: CY2DL1504 1:4 Differential LVDS Fanout Buffer with Selectable Clock Input Document Number: 001-56312				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*D	3135189	CXQ	01/12/2011	Removed “Preliminary” status heading. Removed “Functional equivalent” bullet on page 1. Added “(see I_{OZ})” note to pin 8 description in Pin Definitions. Fixed typo and removed resistors from IN_X/IN_X# in Logic Block Diagram. Added Figure 10 to describe T_{SOE} and T_{SOD}.
*E	3090938	CXQ	02/25/11	Post to external web.
*F	3208968	CXQ	03/29/2011	Changed R_P max from 140 kΩ to 165 kΩ and updated R_P in Logic Block Diagram.
*G	3308039	CXQ	07/11/2011	Updated supported differential input clock types to include CML in Features, Functional Description, Pin Definitions, and DC specs table sections.
*H	3395868	PURU	10/05/11	Updated supported differential input clock types to include HCSL in Features, Pinouts, and DC Electrical Specifications table. Changed Min value of V_{ICM}.

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