# ComLink™ Series
# CY2DL814
# 1:4 Clock Fanout Buffer

## Features

- Low-voltage operation
- $V_{DD}$ = 3.3 V
- 1:4 fanout
- Single-input configurable for
  - LVDS, LVPECL, or LVTTL
  - Four differential pairs of LVDS outputs
- Drives 50 or 100 Ω load (selectable)
- Low input capacitance
- 85 ps typical output-to-output skew
- < 4 ns typical propagation delay
- Does not exceed Bellcore 802.3 standards
- Operation at ⇒ 350 MHz – 700 Mbps
- Industrial versions available
- Packages available include TSSOP

## Functional Description

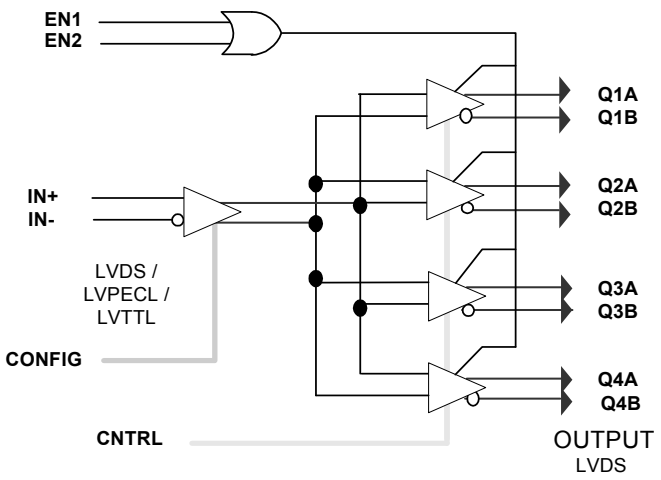
The Cypress CY2 series of network circuits is produced using advanced 0.35 micron CMOS technology, achieving the industry's fastest logic.

The Cypress CY2DL814 fanout buffer features a single LVDS, LVPECL, or LVTTL compatible input and four LVDS output pairs.

Designed for data-communication clock management applications, the fanout from a single input reduces loading on the input clock.

The CY2DL814 is ideal for both level translations from single ended to LVDS and/or for the distribution of LVDS-based clock signals. The Cypress CY2DL814 has configurable input and output functions. The input can be selectable for LVPECL/LVTTL or LVDS signals while the output driver's support standard and high drive LVDS. Drive either a 50 Ω or 100 Ω line with a single part number/device.

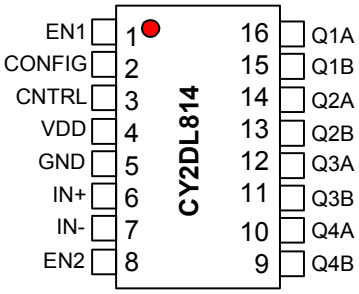
## Block Diagram



## Contents

## Pin Configuration

**Figure 1. 16-pin TSSOP Pinout**




## Pin Description

| Pin Number | Pin Name | Pin Standard Interface | Description |
|---|---|---|---|
| 6,7 | IN+, IN– | Configurable | Differential input pair or single line.<br>LVPECL default. See config below. |
| 3 | CNTRL | LVTTL/LVCMOS | Converts into a High drive driver from a standard LVDS.<br>Standard drive (logic = 0)<br>B/High drive/Bus (logic = 1) |
| 2 | CONFIG | LVTTL/LVCMOS | Converts inputs (IN+/IN–), (EN, EN#) from the default LVPECL/LVDS (logic = 0)<br>To LVTTL/LVCMOS (logic = 1) |
| 1,8 | EN1, EN2 | LVTTL/LVCMOS | Enable/disable logic. See Table 1 below for details. |
| 16,15,14,13,12, 11,10,9 | Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B | LVDS | Differential outputs. |
| 4 | $V_{DD}$ | POWER | Positive supply voltage |
| 5 | $G_{ND}$ | POWER | Ground |

## Maximum Ratings[1, 2]

Storage temperature: ..... –65 °C to +150 °C
Ambient temperature: ..... –40 °C to +85 °C
Supply voltage to ground potential (Inputs and $V_{CC}$ only) .....–0.3 V to 4.6 V
Supply voltage to ground potential (Outputs only) ..... –0.3 V to $V_{DD}$ + 0.3 V
DC input voltage ..... –0.3 V to $V_{DD}$ + 0.3 V
DC output voltage ..... –0.3 V to $V_{DD}$ + 0.9 V
Power dissipation ..... 0.75 W

**Table 1. EN1 EN2 Function Table – Differential Input Mode**

| Enable Logic | | Input | | Outputs | |
|---|---|---|---|---|---|
| **EN1** | **EN2** | **IN+** | **IN–** | **QnA** | **QnB** |
| H | X | H | L | H | L |
| H | X | L | H | L | H |
| X | L | H | L | H | L |
| X | L | L | H | L | H |
| L | H | X | X | Z | Z |

**Table 2. Output Drive Control for Standard and Bus/B/High Drive B**

| CNTRL Pin 3 Binary Value | Drive STD | Impedance | Output Voltage Value |
|---|---|---|---|
| 0 | Standard | 100 Ω | V0 = Voutput |
| | | 50 Ω | V = 1/2 × V0 |
| 1 | High Drive/Bus/B | 100 Ω | V = 2 × V0 |
| | | 50 Ω | V = V0 |

**Table 3. Input Receiver Configuration for Differential or LVTTL/LVCMOS**

| CONFIG Pin 2 Binary Value | Input Receiver Family | Input Receiver Type |
|---|---|---|
| 1 | LVTTL in LVCMOS | Single-ended, non-inverting, inverting, void of bias resistors |
| 0 | LVDS | Low-voltage differential signaling |
| | LVPECL | Low-voltage Pseudo (Positive) emitter coupled logic |

**Table 4. Function Control of the TTL Input Logic Used to Accept or Invert the Input Signal**

| LVTTL/LVCMOS Input Logic | | | |
|---|---|---|---|
| **Input Condition** | | **Input Logic** | **Output Logic Q Pins, Q1A or Q1** |
| Ground | IN– Pin 7 | | |
| | IN+ Pin 6 | Input | True |
| $V_{CC}$ | IN– Pin 7 | | |
| | IN+ Pin 6 | Input | Invert |
| Ground | IN+ Pin 6 | | |
| | IN– Pin 7 | Input | True |
| $V_{CC}$ | IN+ Pin 6 | | |
| | IN– Pin 7 | Input | Invert |

**Notes**
1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**Table 5. Power Supply Characteristics**

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CCD}$ | Dynamic power supply current | $V_{DD}$ = Max<br>Input toggling 50% duty cycle,<br>Outputs open | – | 1.5 | 2.0 | mA/MHz |
| $I_C$ | Total power supply current | $V_{DD}$ = Max<br>Input toggling 50% duty cycle,<br>Outputs open<br>fL = 100 MHz | – | 90 | 100 | mA |

**Table 6. DC Electrical Characteristics: 3.3 V – LVDS Input**

| Parameter | Description | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{ID}$ | Magnitude of differential input voltage | | | 100 | – | 600 | mV |
| $V_{IC}$ | Common-mode of differential input voltage $\|V_{ID}\|$ (min and max) | | | $\|VIDI/2$ | 2.4 – ($\|VIDI/2$) | | V |
| $V_{IH}$ | Input high voltage | Guaranteed logic high level | Config/Control pins | 2 | – | – | V |
| $V_{IL}$ | Input low voltage | Guaranteed logic low level | | – | – | 0.8 | V |
| $I_{IH}$ | Input high current | $V_{DD}$ = Max | $V_{IN} = V_{DD}$ | – | ±10 | ±20 | µA |
| $I_{IL}$ | Input low current | $V_{DD}$ = Max | $V_{IN} = V_{SS}$ | – | ±10 | ±20 | µA |
| $I_I$ | Input high current | $V_{DD}$ = Max, $V_{IN} = V_{DD}$(max) | | – | – | ±20 | µA |

**Table 7. DC Electrical Characteristics: 3.3 V – LVPECL Input**

| Parameter | Description | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{ID}$ | Differential input voltage p-p | Guaranteed logic high level | | 400 | – | 2600 | mV |
| $V_{CM}$ | Common-mode voltage | | | 1.65 | – | 2.25 | V |
| $I_{IH}$ | Input high current | $V_{DD}$ = Max | $V_{IN} = V_{DD}$ | – | ±10 | ±20 | µA |
| $I_{IL}$ | Input low current | $V_{DD}$ = Max | $V_{IN} = V_{SS}$ | – | ±10 | ±20 | µA |
| $I_I$ | Input high current | $V_{DD}$ = Max, $V_{IN} = V_{DD}$(Max) | | – | – | ±20 | µA |

**Table 8. DC Electrical Characteristics: 3.3 V – LVTTL/LVCMOS Input**

| Parameter | Description | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | Guaranteed logic high level | | 2 | – | – | V |
| $V_{IL}$ | Input low voltage | Guaranteed logic low level | | – | – | 0.8 | V |
| $I_{IH}$ | Input high current | $V_{DD}$= Max | $V_{IN}$ = 2.7 V | – | – | 1 | µA |
| $I_{IL}$ | Input low current | $V_{DD}$= Max | $V_{IN}$ = 0.5 V | – | – | –1 | µA |
| $I_I$ | Input high current | $V_{DD}$ = Max, $V_{IN} = V_{DD}$(Max) | | – | – | 20 | µA |
| $V_{IK}$ | Clamp diode voltage | $V_{DD}$ = Min, IIN = –18 mA | | – | –0.7 | –1.2 | V |
| $V_H$ | Input hysteresis | | | – | 80 | | mV |

**Table 9. D.C Electrical Characteristics: 3.3 V – LVDS Output**

| Parameter | Description | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **I** $V_{OD}$ **I** | Differential output voltage p-p | $V_{DD}$ = 3.3 V, $V_{IN}$ = $V_{IH}$, or $V_{IL}$ | RL = 100 ohm | 0.25 | – | 0.45 | V |
| VOC(SS) | Steady-state common-mode output voltage | | | – | – | 226 | mV |
| Delta VOC(SS) | Change in VOC(SS) between logic states | | | –50 | 3 | 50 | mV |
| VOC(PP) | Peak to peak common mode output voltage | | | – | – | 150 | mV |
| $I_{OS}$ | Output short circuit | QA = 0 V or QB = 0 V | | – | – | –20 | mA |
| Voh | Output voltage high | | RL = 100 ohm | – | – | 1475 | mV |
| Vol | Output voltage low | | | 925 | – | – | mV |

**Table 10. AC Parameters**

| Parameter | Description | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Rise time | Pin control (pin 3) logic is “FALSE” defaulting to 100 ohm output drivers. Differential 20% to 80% | CL–10 pF RL and CL to GND 3 CL = $C_{intrinsic}$ and $C_{external}$ | RL = 100 ohm | – | – | 1.4 | ns |
| Fall time | | | | – | – | 1.4 | ns |
| Rise time | Pin control (pin 3) logic is “True” defaulting to 50 ohm output drivers. Differential 20% to 80% | CL–10 pF RL and CL to GND 3 CL = $C_{intrinsic}$ and $C_{external}$ | RL = 50 ohm Output boost | – | 350 | 600 | ps |
| Fall time | | | | – | 350 | 600 | ps |

**Table 11. AC Switching Characteristics @ 3.3 V**

($V_{DD}$ = 3.3 V ± 5%, Temperature = –40 °C to +85 °C)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **IN [+,–] to Q[A,B] Data and Clock Speed** | | | | | | |
| $t_{PLH}$ | Propagation delay – Low to High | $V_{OD}$ = 100 mV | 3 | 4 | 5 | ns |
| $t_{PHL}$ | Propagation delay – High to Low | | 3 | 4 | 5 | ns |
| $T_{pd}$ | Propagation delay | | 3 | 4 | 5 | ns |
| **IN [1,2] to Q[A,B] Control Speed** | | | | | | |
| $T_{Pe}$ | Enable (EN) to functional operation | | – | – | 6 | ns |
| $T_{pd}$ | Functional operation to disable | | – | – | 5 | ns |
| **Q[A,B] Output Skews** | | | | | | |
| $t_{SK(0)}$ | Output Skew: Skew between outputs of the same package (in phase) | | – | 0.085 | 0.2 | ns |
| $t_{SK(p)}$ | Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL}$–$t_{PLH}$) | | – | 0.2 | – | ns |
| $t_{SK(t)}$ | Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. Same input signal level and output load. | $V_{ID}$ = 100 mV | – | – | 1 | ns |

**Table 12. High Frequency Parametrics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Fmax | Maximum frequency<br>$V_{DD}$ = 3.3 V | 50% duty cycle tW(50–50)<br>Standard load circuit. | – | – | 400 | MHz |
| Fmax(20) | Maximum frequency<br>$V_{DD}$ = 3.3 V | 20% duty cycle tW(50–50)<br>LVPECL input<br>$V_{IN} = V_{IH}(Max)/V_{IL}(Min)$<br>$V_{OUT} = V_{OH}(Min)/V_{OL}$ (Max) (Limit) | – | – | 200 | MHz |
| TW | Minimum pulse<br>$V_{DD}$ = 3.3 V | LVPECL Input<br>$V_{IN} = V_{IH}(Max)/V_{IL}(Min)$ F= 100 MHz<br>$V_{OUT} = V_{OH}(Min)/V_{OL}(Max)$(Limit) | 1 | – | – | ns |

**Figure 2. Differential Receiver to Driver Propagation Delay and Driver Transition Time**[3, 4, 5, 6]

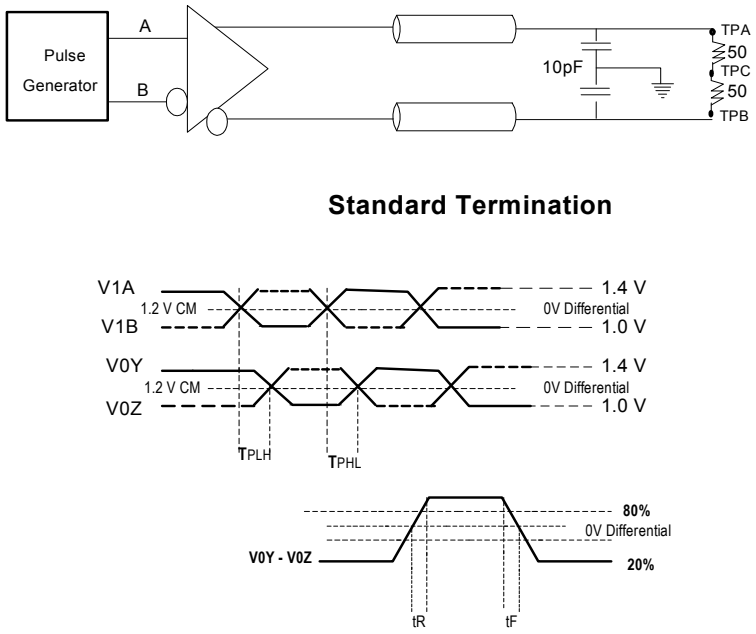
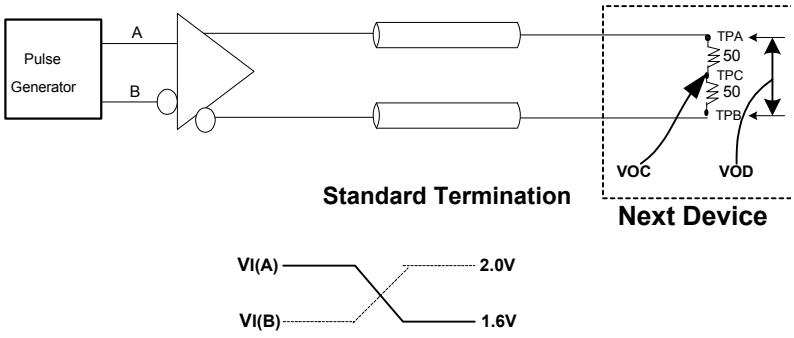
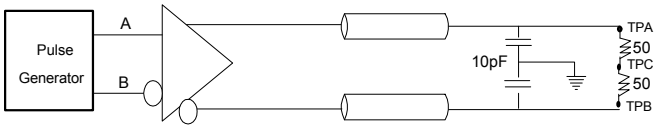



**Figure 3. Test Circuit and Voltage Definitions for the Driver Common-mode Output Voltage**[3, 4, 5, 6]




**Notes**
3. All input pulses are supplied by a frequency generator with the following characteristics: $t_R$ and $t_F \leq 1$ ns; pulse rerate = 50 Mpps; pulse width = 10 ± 0.2 ns.
4. RL= 50 ohm ± 1% Zline = 50 ohm 6”.
5. CL includes instrumentation and fixture capacitance within 6 mm of the UT.
6. TPA and B are used for prop delay and Rise/Fall measurements. TPC is used for VOC measurements only and is otherwise connected to $V_{DD-2}$.

**Figure 4. Test Circuit and Voltage Definitions for the Differential Output Signal**[7, 8, 9, 10]




**Standard Termination**

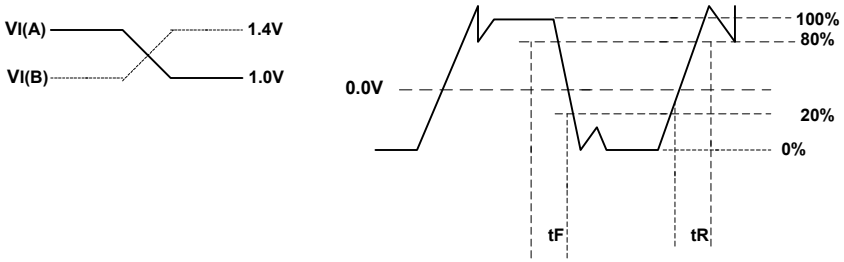



**Figure 5. LVCMOS/LVTTL Single-ended Input Value**[11]

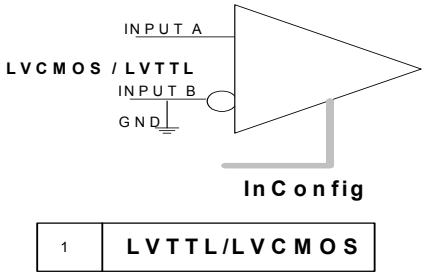
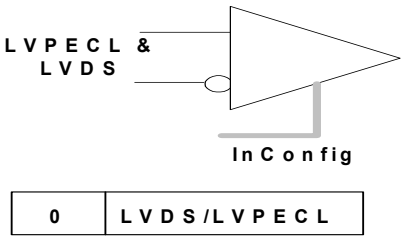



**Figure 6. LVPECL or LVDS Differential Input Value**[12]

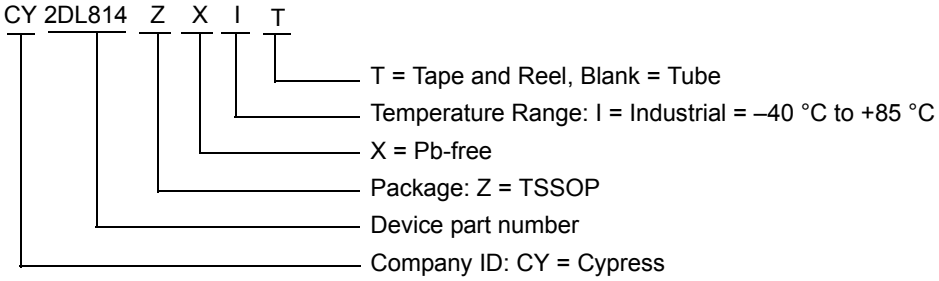



**Notes**
7. All input pulses are supplied by a frequency generator with the following characteristics: $t_R$ and $t_F \leq 1$ ns; pulse rerate = 50 Mpps; pulse width = 10 ± 0.2 ns.
8. RL= 50 ohm ± 1% Zline = 50 ohm 6".
9. CL includes instrumentation and fixture capacitance within 6 mm of the UT.
10. TPA and B are used for prop delay and Rise/Fall measurements. TPC is used for VOC measurements only and is otherwise connected to $V_{DD-2}$.
11. LVCMOS/LVTTL single ended input value. Ground either input: when on the B side then non-inversion takes place. If A side is grounded, the signal becomes the complement of the input on B side. See Table 4.
12. LVPECL or LVDS differential input value.

## Ordering Information

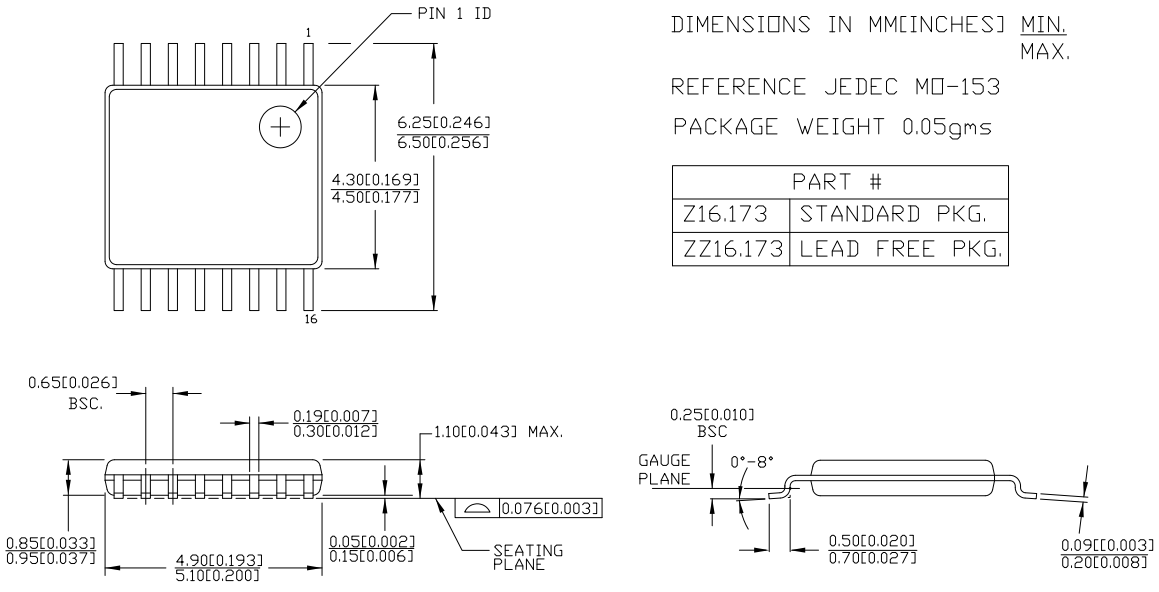
| Part Number | Package Type | Product Flow |
|---|---|---|
| Pb-free | | |
| CY2DL814ZXI | 16-pin TSSOP | Industrial, –40 °C to 85 °C |
| CY2DL814ZXIT | 16-pin TSSOP – Tape and Reel | Industrial, –40 °C to 85 °C |

### Ordering Code Definitions




## Package Drawing and Dimensions

**Figure 7. 16-pin TSSOP 4.40 mm Body Z16.173**




51-85091 *C

## Acronyms

| Acronym | Description |
|---|---|
| CMOS | Complementary metal oxide semiconductor |
| LVDS | Low voltage differential signaling |
| LVPECL | Low voltage positive emitter coupled logic |
| LVTTL | Low voltage transistor transistor logic |
| TSSOP | thin-shrink small outline package |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| Ω | ohms |
| kΩ | kilo ohms |
| MHz | Mega Hertz |
| µA | micro Amperes |
| mA | milli Amperes |
| % | percent |
| pF | pico Farads |
| ppm | parts per million |
| ps | pico seconds |
| ns | nano seconds |
| ms | milli seconds |
| mV | milli Volts |
| V | Volts |
| mW | milli Watts |
| W | Watts |

## Document History Page

| Document Title: ComLink™ Series CY2DL814 1:4 Clock Fanout Buffer<br>Document Number: 38-07057 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 115362 | 07/10/02 | EHX | New Data Sheet |
| *A | 122744 | 12/14/02 | RBI | Added power up requirements to maximum ratings information. |
| *B | 384077 | See ECN | RGL | Added Lead-free devices<br>Added typical values |
| *C | 2899846 | 03/26/10 | KVM | Removed inactive parts in ordering information table<br>Updated package diagram<br>Removed SOIC package |
| *D | 3085165 | 11/12/2010 | BASH | Added Ordering Code Definitions.<br>Updated Package Drawing and Dimensions.<br>Minor edits and updated in new template. |

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