CY2DP1510

1:10 LVPECL Fanout Buffer with Selectable Clock Input

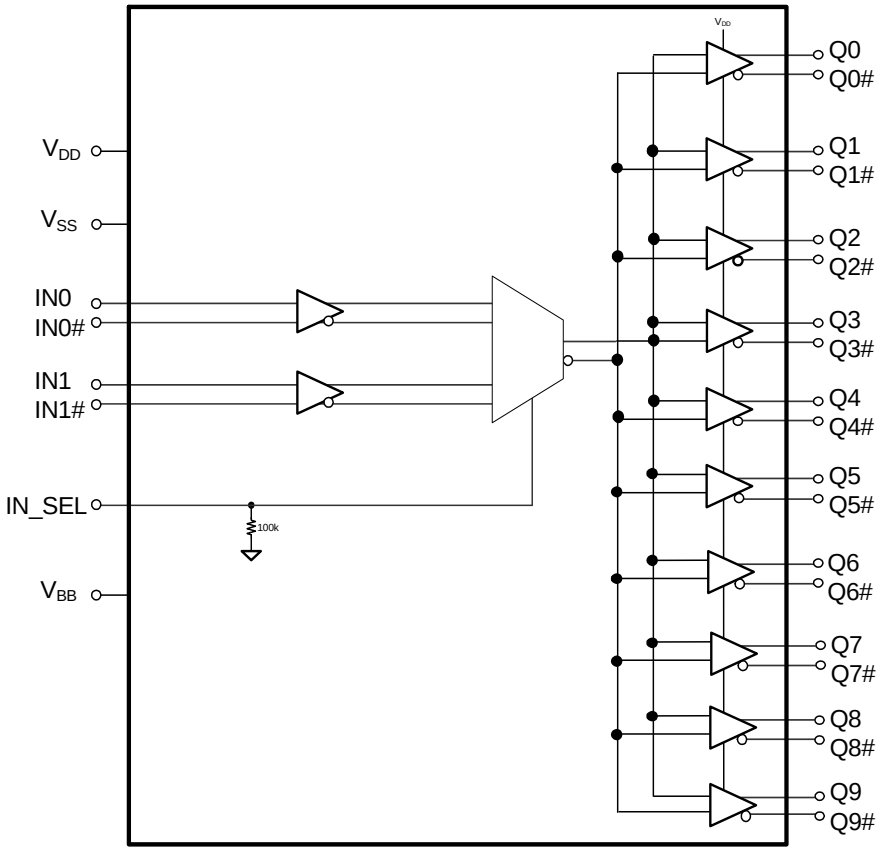
Features

- Select one of two low-voltage positive emitter-coupled logic (LVPECL) input pairs to distribute to 10 LVPECL output pairs
- 40-ps maximum output-to-output skew
- 600-ps maximum propagation delay
- 0.11-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 1.5-GHz operation
- 32-Pin thin quad flat pack (TQFP) package
- 2.5-V or 3.3-V operating voltage[1]
- Commercial and industrial operating temperature range

Functional Description

The CY2DP1510 is an ultra-low noise, low skew, low-propagation delay 1:10 LVPECL fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The CY2DP1510 can select between two separate LVPECL input clock pairs using the IN_SEL pin. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 1.5 GHz.

Logic Block Diagram



Note
1. Input AC-coupling capacitors are required for voltage-translation applications.

Contents

Pinouts

Figure 1. Pin Diagram – 32-Pin TQFP Package

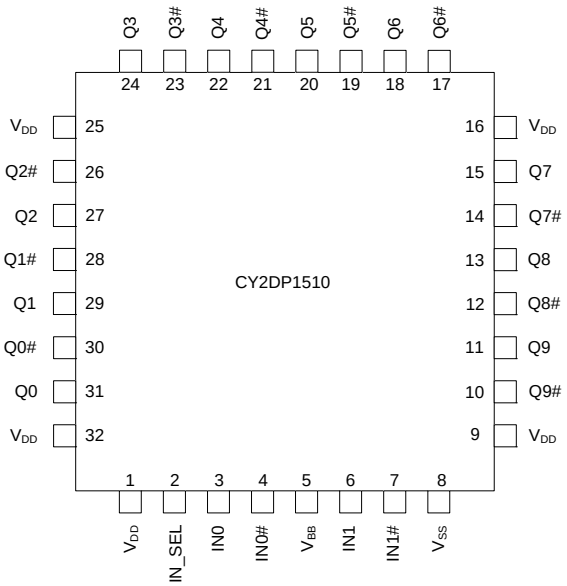


Table 1. Pin Definitions

Pin No.	Pin Name	Pin Type	Description
1, 9, 16, 25, 32	V_{DD}	Power	Power supply
2	IN_SEL	Input	Input clock select pin. Low-voltage complementary metal oxide semiconductor (LVCMOS)/low-voltage transistor-transistor-logic (LVTTL). When IN_SEL = Low, the IN0/IN0# differential input pair is active When IN_SEL = High, the IN1/IN1# differential input pair is active
3	IN0	Input	LVPECL input clock. Active when IN_SEL = Low
4	IN0#	Input	LVPECL complementary input clock. Active when IN_SEL = Low
5	V_{BB}	Output	LVPECL reference voltage output
6	IN1	Input	LVPECL input clock. Active when IN_SEL = High
7	IN1#	Input	LVPECL complementary input clock. Active when IN_SEL = High
8	V_{SS}	Power	Ground
10,12,14,17,19,21, 23,26,28,30	Q(0:9)#	Output	LVPECL complementary output clocks
11,13,15,18,20,22, 24,27,29,31	Q(0:9)	Output	LVPECL output clocks
–	EPAD	–	Exposed paddle. Connect to ground plane for package heat dissipation. No electrical connection.

Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	Nonfunctional	–0.5	4.6	V
V_{IN}[2]	Input voltage, relative to V_{SS}	Nonfunctional	–0.5	lesser of 4.0 or V_{DD} + 0.4	V
V_{OUT}[2]	DC output or I/O voltage, relative to V_{SS}	Nonfunctional	–0.5	lesser of 4.0 or V_{DD} + 0.4	V
T_S	Storage temperature	Nonfunctional	–55	150	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	–	V
L_U	Latch up		Meets or exceeds JEDEC Spec JESD78B IC latch up test		
UL–94	Flammability rating	At 1/8 in	V – 0		
MSL	Moisture sensitivity level		3		

Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.5-V supply	2.375	2.625	V
		3.3-V supply	3.135	3.465	V
T_A	Ambient operating temperature	Commercial	0	70	°C
		Industrial	–40	85	°C
t_{PU}	Power ramp time	Power-up time for V_{DD} to reach minimum specified voltage (power ramp must be monotonic).	0.05	500	ms

Note
2. The voltage on any I/O pin cannot exceed the power pin during power up. Power supply sequencing is not required.

DC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Max	Unit
I_{DD}	Operating supply current	All LVPECL outputs floating (internal I_{DD})	–	120	mA
V_{IH1}	Input high voltage, LVPECL input clocks IN0 and IN0#, IN1 and IN1#		–	V_{DD} + 0.3	V
V_{IL1}	Input low voltage, LVPECL input clocks IN0 and IN0#, IN1 and IN1#		–0.3	–	V
V_{IH2}	Input high voltage, IN_SEL	V_{DD} = 3.3 V	2.0	V_{DD} + 0.3	V
V_{IL2}	Input low voltage, IN_SEL	V_{DD} = 3.3 V	–0.3	0.8	V
V_{IH3}	Input high voltage, IN_SEL	V_{DD} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL3}	Input low voltage, IN_SEL	V_{DD} = 2.5 V	–0.3	0.7	V
V_{ID}[3]	Input differential amplitude	See Figure 2 on page 7	0.4	1.0	V
V_{ICM}	Input common mode voltage	See Figure 2 on page 7	0.5	V_{DD} – 0.2	V
I_{IH}	Input high current, All inputs	Input = V_{DD}[4]	–	150	µA
I_{IL}	Input low current, All inputs	Input = V_{SS}[4]	–150	–	µA
V_{OH}	LVPECL output high voltage	Terminated with 50 Ω to V_{DD} – 2.0[5]	V_{DD} – 1.20	V_{DD} – 0.70	V
V_{OL}	LVPECL output low voltage	Terminated with 50 Ω to V_{DD} – 2.0[5]	V_{DD} – 2.0	V_{DD} – 1.63	V
V_{BB}	Output reference voltage	0 to 150 µA output current	V_{DD} – 1.40	V_{DD} – 1.16	V
R_P	Internal pull-down resistance	IN_SEL pin	60	140	kΩ
C_{IN}	Input capacitance	Measured at 10 MHz; per pin	–	3	pF

Notes
3. V_{ID} minimum of 400 mV is required to meet all output AC electrical specifications. The device is functional with V_{ID} minimum of greater than 200 mV.
4. Positive current flows into the input pin, negative current flows out of the input pin.
5. Refer to Figure 3 on page 7.

AC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{IN}	Input frequency		DC	–	1.5	GHz
F_{OUT}	Output frequency	$F_{OUT} = F_{IN}$	DC	–	1.5	GHz
V_{PP}	LVPECL differential output voltage peak to peak, single ended. Terminated with 50 Ω to V_{DD} – 2.0[6]	Fout = DC to 150 MHz	600	–	–	mV
		Fout = >150 MHz to 1.5 GHz	400	–	–	mV
t_{PD}[7]	Propagation delay input pair to output pair	Input rise/fall time < 1.5 ns (20% to 80%)	–	–	600	ps
t_{ODC}[8]	Output duty cycle	50% duty cycle at input Frequency range up to 1 GHz	48	–	52	%
t_{SK1}[9]	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	40	ps
$t_{SK1\ D}$[9]	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
PN_{ADD}	Additive RMS phase noise 156.25-MHz input Rise/fall time < 150 ps (20% to 80%) V_{ID} > 400 mV	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–130	dBc/Hz
		Offset = 100 kHz	–	–	–140	dBc/Hz
		Offset = 1 MHz	–	–	–150	dBc/Hz
		Offset = 10 MHz	–	–	–154	dBc/Hz
		Offset = 20 MHz	–	–	–155	dBc/Hz
t_{JIT}[10]	Additive RMS phase jitter (Random)	156.25 MHz, 12 kHz to 20 MHz offset; input rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV	–	–	0.11	ps
t_R,t_F[11]	Output rise/fall time	50% duty cycle at input, 20% to 80% of full swing (V_{OL} to V_{OH}) Input rise/fall time < 1.5 ns (20% to 80%)	–	–	300	ps

Notes
6. Refer to Figure 3 on page 7.
7. Refer to Figure 4 on page 7.
8. Refer to Figure 5 on page 7.
9. Refer to Figure 6 on page 8.
10. Refer to Figure 7 on page 8.
11. Refer to Figure 8 on page 8.

Figure 2. Input Differential and Common Mode Voltages

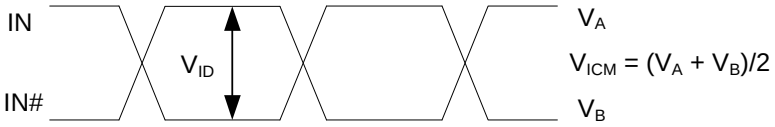


Figure 3. Output Differential Voltage

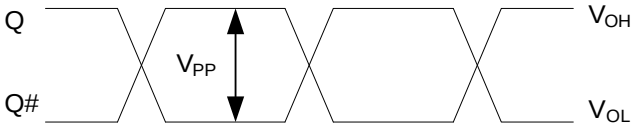


Figure 4. Input to Any Output Pair Propagation Delay

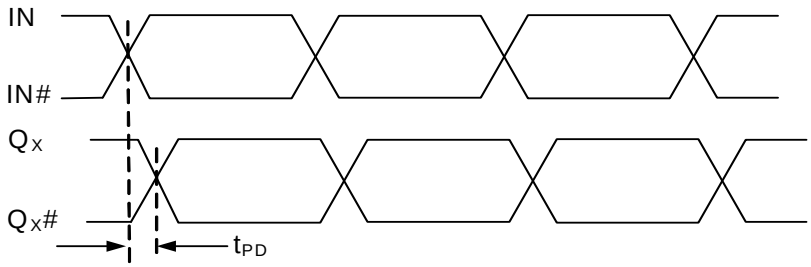


Figure 5. Output Duty Cycle

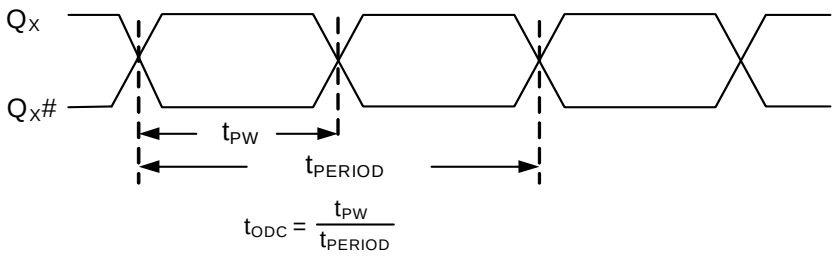


Figure 6. Output-to-Output and Device-to-Device Skew

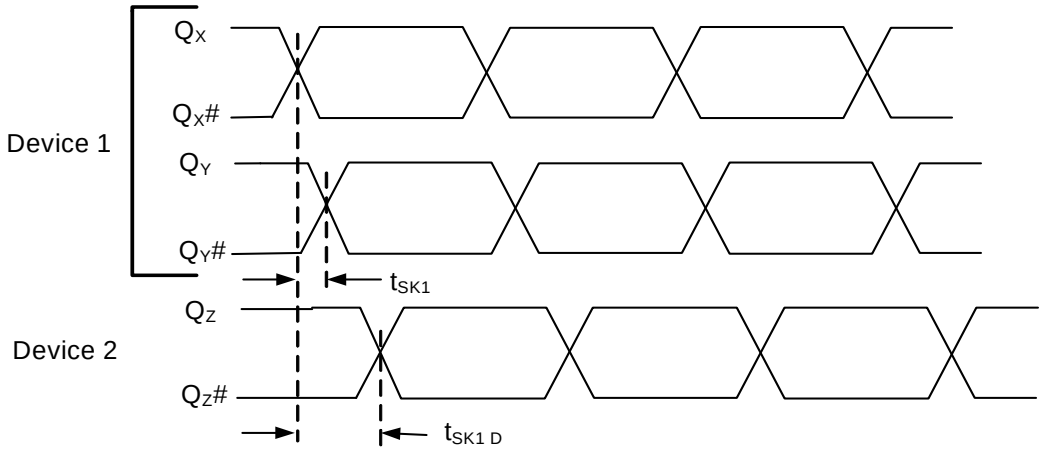


Figure 7. RMS Phase Jitter

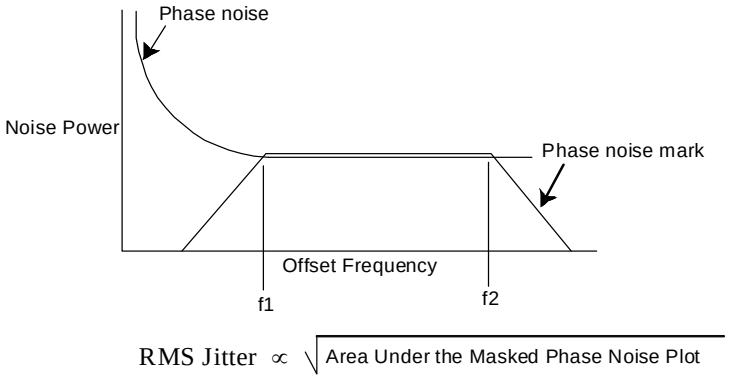
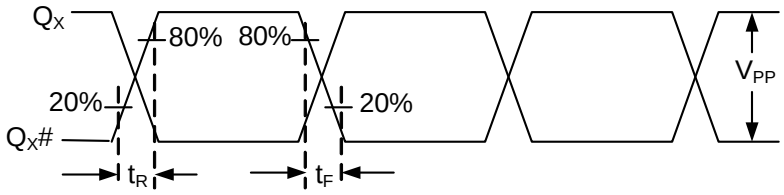


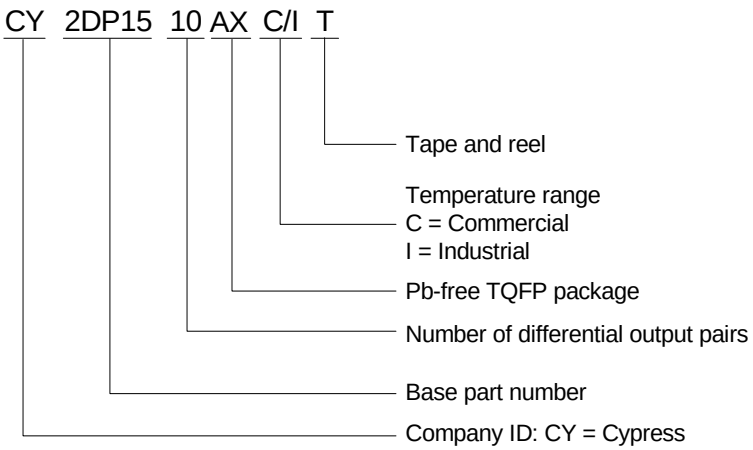
Figure 8. Output Rise/Fall Time



Ordering Information

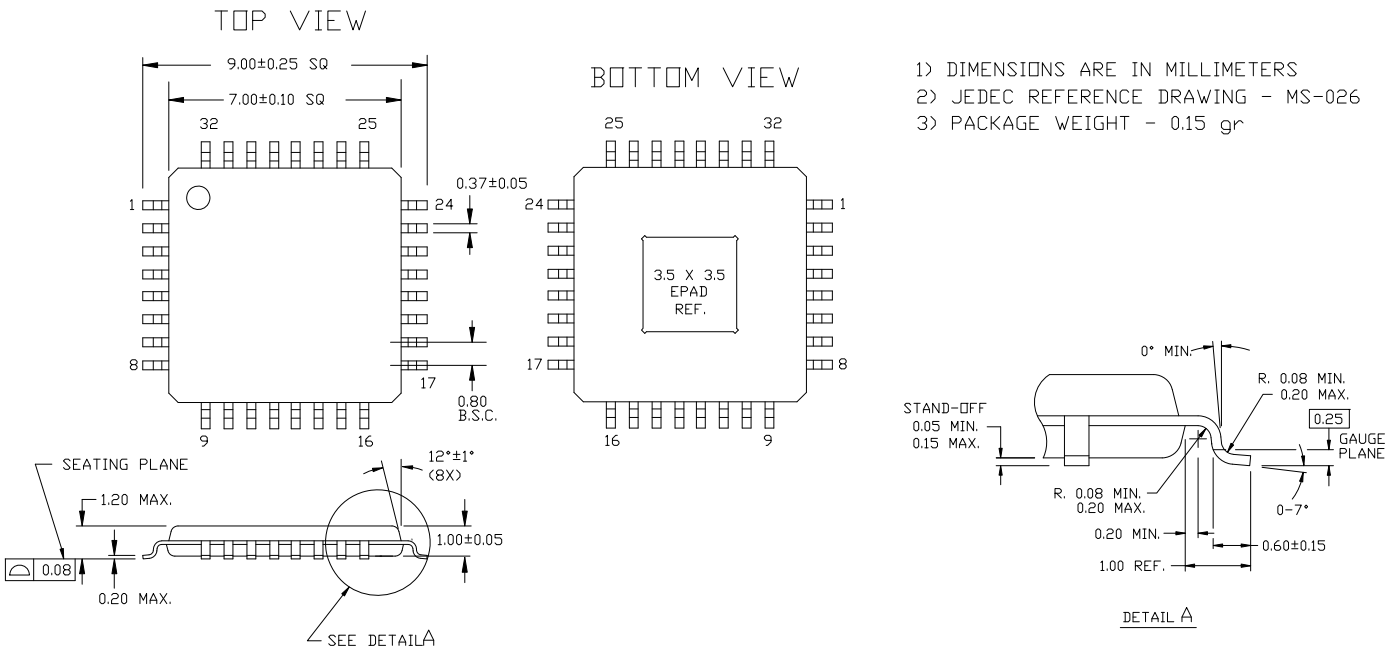
Part Number	Type	Production Flow
Pb-free		
CY2DP1510AXC	32-Pin TQFP	Commercial, 0 °C to 70 °C
CY2DP1510AXCT	32-Pin TQFP tape and reel	Commercial, 0 °C to 70 °C
CY2DP1510AXI	32-Pin TQFP	Industrial, –40 °C to 85 °C
CY2DP1510AXIT	32-Pin TQFP tape and reel	Industrial, –40 °C to 85 °C

Ordering Code Definition



Package Dimension

Figure 9. 32-Pin Thin Plastic Quad Flat Pack 7 × 7 × 1.0 mm



001-54497 *A

Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
ESD	electrostatic discharge
HBM	human body model
JEDEC	Joint electron devices engineering council
LVDS	low-voltage differential signal
LVCMOS	low-voltage complementary metal oxide semiconductor
LVPECL	low-voltage positive emitter-coupled logic
LVTTL	low-voltage transistor-transistor logic
OE	Output enable
RMS	root mean square
TQFP	thin quad flat pack

Document Conventions

Table 3. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	giga hertz
Hz	hertz
KΩ	kilo ohm
µA	microamperes
µF	micro Farad
µs	microsecond
mA	milliamperes
ms	millisecond
mV	millivolt
MHz	megahertz
ns	nanosecond
Ω	ohm
pF	pico Farad
ps	pico second
V	volts
W	watts

Document History Page

Document Title: CY2DP1510 1:10 LVPECL Fanout Buffer with Selectable Clock Input Document Number: 001-55566				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2782891	CXQ	10/09/09	New Datasheet.
*A	2838916	CXQ	01/05/2010	Changed status from “ADVANCE” to “PRELIMINARY”. Changed from 0.34 ps to 0.25 ps maximum additive jitter in “Features” on page 1 and in t_{JIT} in the AC Electrical Specs table on page 5. Added t_{PU} spec to the Operating Conditions table on page 3. Changed V_{OH} in the DC Electrical Specs table on page 4: minimum from V_{DD} - 1.15V to V_{DD} - 1.20V; maximum from V_{DD} - 0.75V to V_{DD} - 0.70V. Removed V_{OD} spec in the DC Electrical Specs table on page 4. Changed V_{BB} max spec in the DC Electrical Specs table on page 4 from V_{DD} - 1.38V to V_{DD} - 1.40V. Added R_P spec in the DC Electrical Specs table on page 4. Min = 60 kΩ, Max = 140 kΩ. Added a measurement definition for C_{IN} in the DC Electrical Specs table on page 4. Added V_{PP} spec to the AC Electrical Specs table on page 5. V_{PP} min = 600 mV for DC - 150 MHz and min = 400 mV for 150 MHz to 1.5 GHz. Changed letter case and some names of all the timing parameters in the AC Electrical Specs table on page 5 to be consistent with EROS. Lowered all additive phase noise mask specs by 3 dB in the AC Electrical Specs table on page 5. Added condition to t_R and t_F specs in the AC Electrical specs table on page 5 that input rise/fall time must be less than 1.5 ns (20% to 80%). Changed letter case and some names of all the timing parameters in Figures 3, 4, 5, 6 and 8, to be consistent with EROS.
*B	2885033	CXQ	02/26/2010	Updated 32-Pin TQFP package diagram.
*C	3011766	CXQ	08/23/2010	Changed from 0.25 ps to 0.11 ps maximum additive jitter in “Features” on page 1 and in t_{JIT} in the AC Electrical Specs table on page 6. Added description of EPAD to Table 1 pin definitions. Added note 3 to describe I_{IH} and I_{IL} specs. Changed V_{BB} max from V_{DD} - 1.26V to V_{DD} - 1.16V in DC Electrical Specs. Removed reference to data distribution from “Functional Description”. Changed R_P for differential inputs from 100 kΩ to 150 kΩ in the Logic Block Diagram and from 60 kΩ min / 140 kΩ max to 90 kΩ min / 210 kΩ max in the DC Electrical Specs table. Added max V_{ID} of 1.0V in DC Electrical Specs table. Changed t_{PD} max spec from 480 ps to 600 ps. Updated phase noise specs for 1 k/10 k/100 k/1 M/10 M/20 MHz offset to -120/-130/-135/-150/-150/-150dBc/Hz, respectively, in the AC Electrical Specs table. Added “Frequency range up to 1 GHz” condition to t_{ODC} spec. Updated package drawing to 001-54497 to reflect use of EPAD package. Added Acronyms and Ordering Code Definition.
*D	3017258	CXQ	08/27/2010	Corrected Output Rise/Fall time diagram.
*E	3100234	CXQ	11/18/2010	Changed V_{IN} and V_{OUT} specs from 4.0V to “lesser of 4.0 or V_{DD} + 0.4” Removed 200mA min LU spec, replaced with “Meets or exceeds JEDEC Spec JESD78B IC Latchup Test” Removed R_P spec for differential input clock pins IN_X and IN_X#. Changed C_{IN} condition to “Measured at 10 MHz”. Changed PN_{ADD} specs for 100kHz, 10MHz, and 20MHz offsets.
*F	3135201	CXQ	01/12/2011	Removed “Preliminary” status heading. Removed pull-up/pull-down resistors from IN_x/IN_x# pins in Logic Block Diagram.
*G	3090938	CXQ	02/25/2011	Post to external web.

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