# ComLink™ Series
# CY2LL842

## Two-channel LVDS Repeater/Mux

### Features

- **ANSI TIA/EIA-644-1995-compliant**
- **Does not exceed Belcore 802.3 standards**
- **Operation at => 350 MHz–700 Mbps**
- **Single 2 × 2**
- **Low-voltage differential signaling (LVDS) with output voltages of ± 350 mV into 100-ohm load version (Std)**
- **Single 3.3V supply**
- **Accepts ± 350 mV differential inputs**
- **Output drivers are high-impedance when disabled or when $V_{DD} \leq 1.5V$**
- **16-pin SOIC/TSSOP packages**
- **Industrial version available**

### Description

The CYPRESS CY2LL842 are differential line drivers and receivers that utilize LVDS to achieve signaling rates of 650 Mbs. The receiver outputs can be switched to either or both drivers thru the multiplexer control signals S0/S1. This provides flexibility in application for either a splitter or router configuration with a single device.

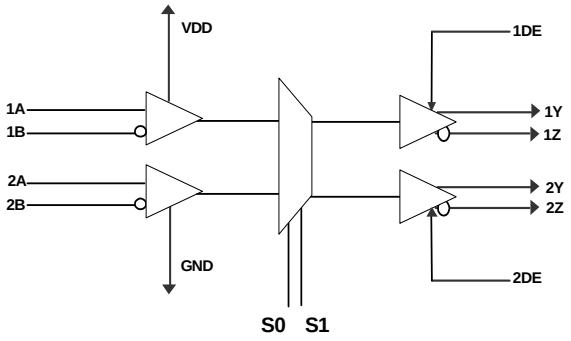
The CYPRESS CY2LL842 is configured as a single two-channel repeater/Mux.

The LVDS standard provides a minimum differential output voltage of 247 mV into a 100-ohm load and receipt of as little as 100-mV signals with up to 1V of DC offset between transmitter and receiver.

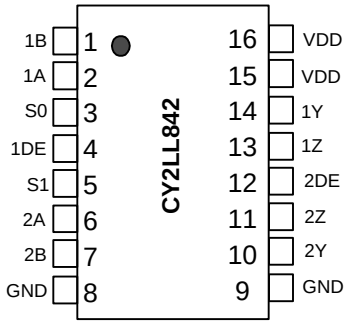
A doubly terminated bus LVDS line enables multipoint configurations.

Designed for both point to point based-band multi-point data transmission over controlled impedance lines.

### Block Diagram




### Pin Configuration




**16 pin SOIC/TSSOP**

## Pin Description

| Pin Number | Pin Name | Pin Description |
|---|---|---|
| 1,2 | 1B, 1A | Differential Input Channel 1 |
| 3 | S0 | Function Select 0 |
| 4 | 1DE | Data Enable Channel 1 |
| 5 | S1 | Function Select 1 |
| 6,7 | 2A, 2B | Differential Input Channel 2 |
| 8,9 | GND | Ground |
| 10,11 | 2Y, 2Z | Differential Output Channel 2 |
| 12 | 2DE | Data Enable Channel 2 |
| 14,13 | IY, 1Z | Differential Output Channel 1 |
| 15,16 | $V_{DD}$ | Supply Voltage |

**Table 1. Mux Function Table**

| Input | | Output[1] | | Function |
|---|---|---|---|---|
| S0 | S1 | 1Y/1Z | 2Y/2Z | |
| 0 | 0 | 1A/1B | 1A/1B | Splitter A |
| 1 | 0 | 2A/2B | 2A/2B | Splitter B |
| 0 | 1 | 1A/1B | 2A/2B | Pass Thru Router |
| 1 | 1 | 2A/2B | 1A/1B | Cross Point Router |

**Table 2. Absolute Maximum Rating Over Operating Free-air Temperature[2]**

| | |
|---|---|
| Supply Voltage Range, $V_{DD}$(1) | –0.5V to 4V |
| Voltage Range (DE,S0,S1) | –0.5V to 6.0V |
| Input Voltage Range, VIN (A or B) | –0.5V to $V_{DD}$+0.5V |
| ESD (All pins) | Class 3, A: 2KV, B: 500V |
| Storage Temperature Range | –65°C to 150°C |

**Table 3. Recommended Operating Conditions[3]**

| Parameter | Description | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 3 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level Input Voltage | (S0,S1,1DE,2DE) | 2 | | | |
| $V_{IL}$ | Low-level Input Voltage | (S0,S1,1DE,2DE) | | | 0.8 | |
| $V_{ID}$ | Magnitude of Differential Input Voltage | | 0.1 | | 0.6 | |
| $V_{IC}$ | Common Mode Input Voltage | ( see *Figure 6*,*Figure 7*, and *Figure 8*) | $V_{ID}$/2 | | 2.4–(VID/2) | |
| $T_A$ | Operating Free Air Temperature | | –40 | | 85 | °C |

**Table 4. Receiver Electrical Characteristics Over Recommended Operating Conditions**

| Parameter | Description | Test Conditilons | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VITH+ | Positive-going Differential Input Voltage Threshold | $V_{CM}$ = 1.2V | | | 100 | mV |
| VITH- | Negative-going Differential Input Voltage Threshold | $V_{CM}$ = 1.2V | –100 | | | mV |
| II | Input Current ( A Inputs) | VI = 0V | –0.5 | | –10 | uA |
| | | VI = 2.4V | | | –10 | uA |
| II | Input Current (B Inputs) | VI = 0.8V | 0.5 | | 10 | uA |
| | | VI = 2.4V | | | 10 | uA |
| II (Off) | Power-off Current (A or B Inputs) | $V_{DD}$ = 0V | | 0.1 | 10 | uA |

**Notes:**
1. See *Figure 1*.
2. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
3. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**Table 5. Receiver Electrical Characteristics Over Recommended Operating Conditions**

| Parameter | Description | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential Output Voltage Swing | RL = 100 Ohm | See *Figure 9* | 247 | 340 | 454 | mV |
| ~$V_{OD}$ | Change in differential Output Voltage Swing between logic states | | | –50 | | 50 | mV |
| $V_{OC}$(SS) | Steady State Common-mode output voltage | | See *Figure 10* | 1.125 | | 1.375 | V |
| ~$V_{OC}$(SS) | Change in Steady State Common-mode output between logic states | | | –50 | 3 | 50 | mV |
| $V_{OC}$(PP) | Peak to Peak Common-mode output voltage | | | | | 150 | mV |
| $I_{CC}$ | Supply Current | No load f = 100 MHz | | | | 25 | mA |
| | | RL = 100 ohm f = 100 MHz | | | | 25 | mA |
| | | Both Channels Disabled f = 100 MHz | | | | 20 | mA |
| $I_H$ | High-level Input Current | S0,S1,DE | $V_{IH}$ = 5V | | 20 | | uA |
| $I_{IL}$ | Low-level Input Current | S0,S1,DE | $V_{IL}$ = 0.8V | | 5 | | uA |
| $I_{OS}$ | Short-circuit Current | | $V_{OY}$ or $V_{0Z}$ = 0V | | | 20 | mA |
| | | | $V_{OD}$ = 0V | | | 20 | |
| $I_{OZ}$ | High-impedance Output Current | | $V_{OD}$ = 60mV | | 0.1 | 1 | uA |
| | | | $V_O$= 0V or $V_{DD}$ | | 0.1 | 1 | |
| $C_{in}$ | Input Capacitance | | 1A, 1B, 2A, 2B | | 3 | | pF |
| | Control Input Capacitance | | S0, S1, 1DE, 2DE | | 8 | | pF |

**Table 6. Differential Receiver to Driver Switching Characteristics Over Recommended Operating Conditions[5]**

| Parameter | Description | Test Conditions | Min. | Typ.[4] | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{PLH}$ | Differential Propagation delay, low to high | CL = 10 pF (see *Figure 11*) | | 4 | 6 | nS |
| $T_{PHL}$ | Differential Propagation delay, high to low | | | 4 | 6 | nS |
| $T_{sk(p)}$ | Pulse Skew ( $T_{PHL}$–$T_{PLH}$) | | | 0.2 | | nS |
| $T_r$ | Transition Low to High | | | 800 | 1500 | pS |
| $T_f$ | Transition High to Low | | | 800 | 1500 | pS |
| $T_{PHZ}$ | Propagation delay, high-level to high-impedance output | (see *Figure 12*) | | 4 | 10 | nS |
| $T_{PLZ}$ | Propagation delay, low-level to high-impedance output | | | 4.3 | 10 | nS |
| $T_{PZH}$ | Propagation delay, high-impedance to high-level output | | | 3 | 10 | nS |
| $T_{PZL}$ | Propagation delay, high-impedance to low-level output | | | 2 | 10 | nS |
| $T_{PHL\_skR1\_Dx}$ | Channel to Channel skew-receiver 1 to Any mux related drivers | | | 95 | | pS |
| $T_{PLH\_skR1\_Dx}$ | Channel to Channel skew-receiver 1 to Any mux related drivers | | | 95 | | pS |
| $T_{PPHL\_skR2\_Dx}$ | Channel to Channel skew-receiver 2 to Any mux related drivers | | | 95 | | pS |
| $T_{PLH\_skR2\_Dx}$ | Channel to Channel skew-receiver 2 to Any mux related drivers | | | 95 | | pS |
| $D_J$(P-P) | Deterministic Jitter (100 MHz 25C VID = 0.4 So,S1=00) | PRBS Differential | | 95 | | pS |

**Notes:**
4. All typical values are measured at 25°C with a 3.3V supply.
5. These parameters are measured over supply voltage and temperature ranges recommended for the device.

## High-frequency Parametrics

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Fmax | Maximum frequency $V_{DD}$ = 3.3V | 50% duty cycle tW(50–50)<br>Standard Load Circuit. | | | 400 | MHz |

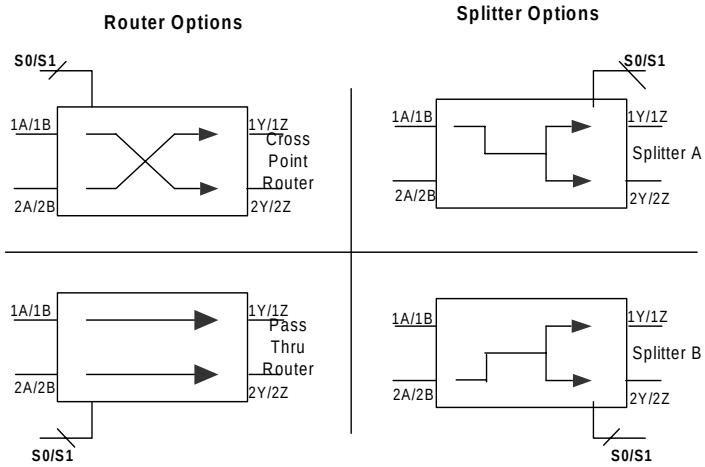



**Figure 1. 2 Channel Cross Point Switch/Mux**

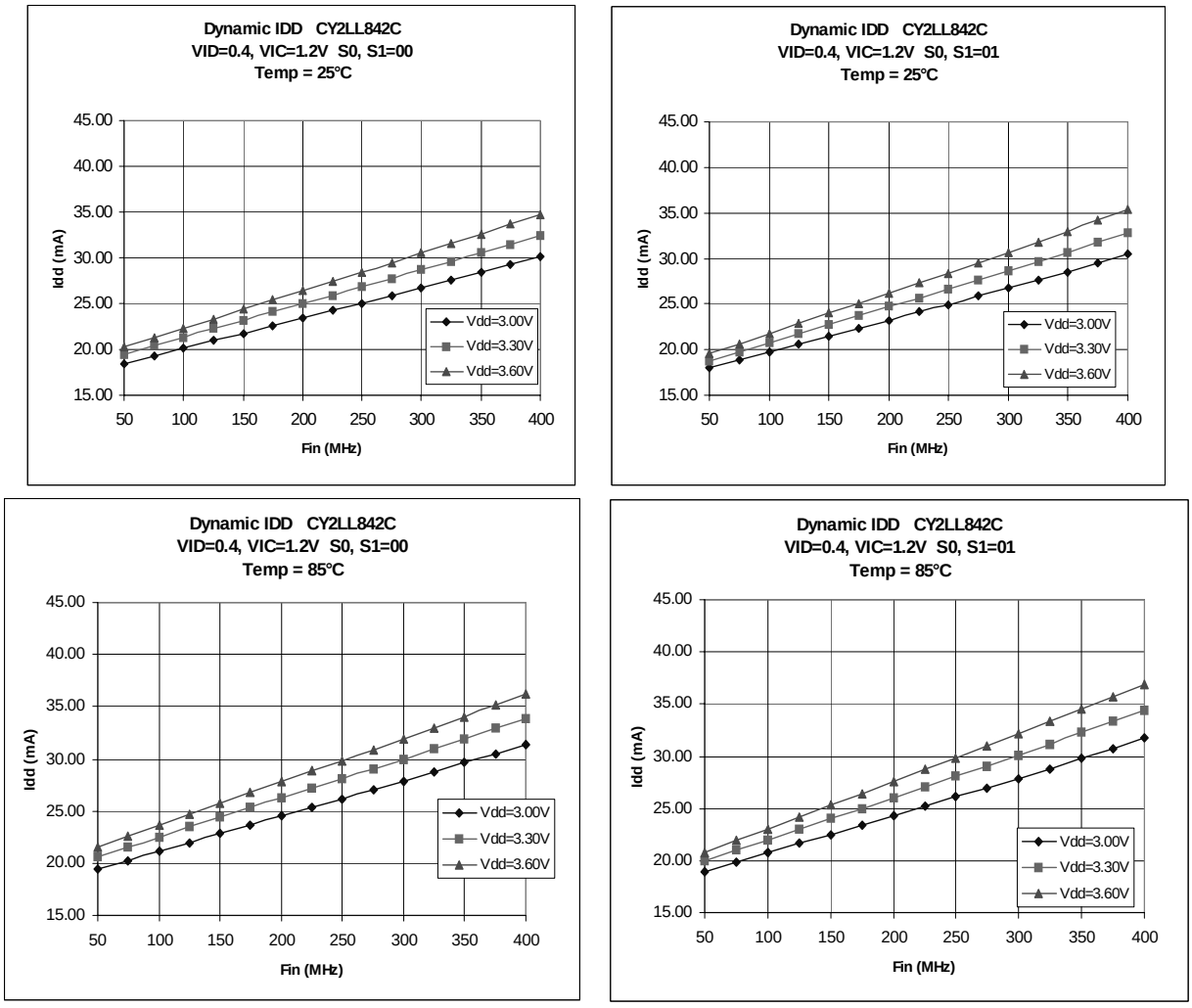



**Figure 2. IDD vs. Frequency**

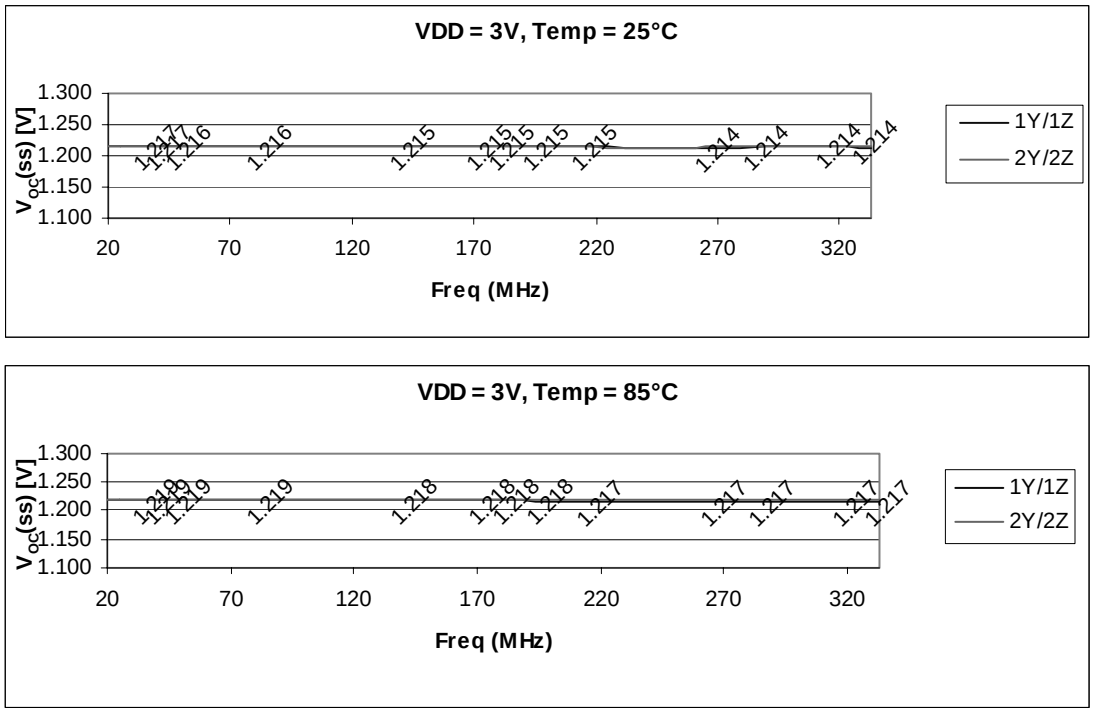



**Figure 3. VOC(ss) of PRBS at Network Frequencies**

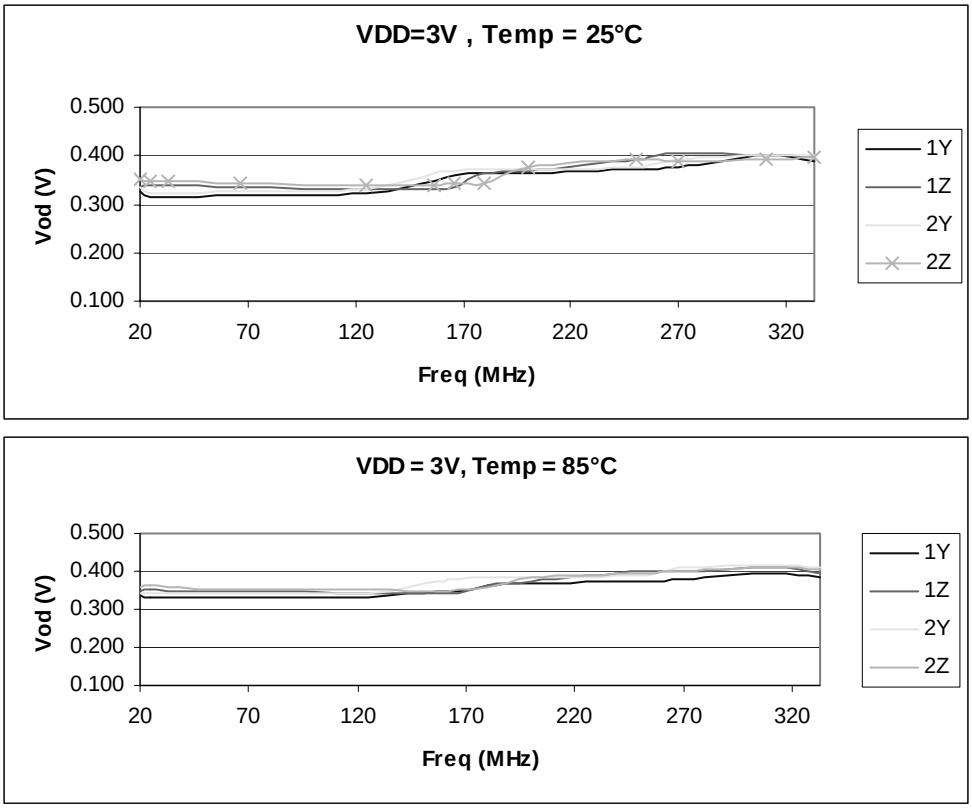



**Figure 4. VOD of PRBS at Network Frequencies**

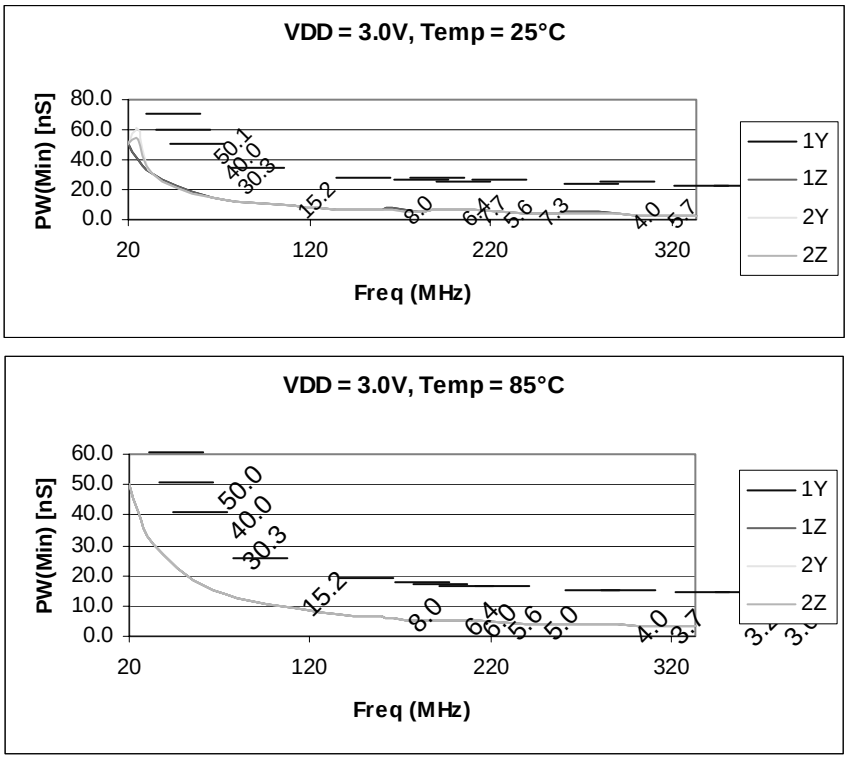



**Figure 5. PRBS Waveform Minimum Pulse**

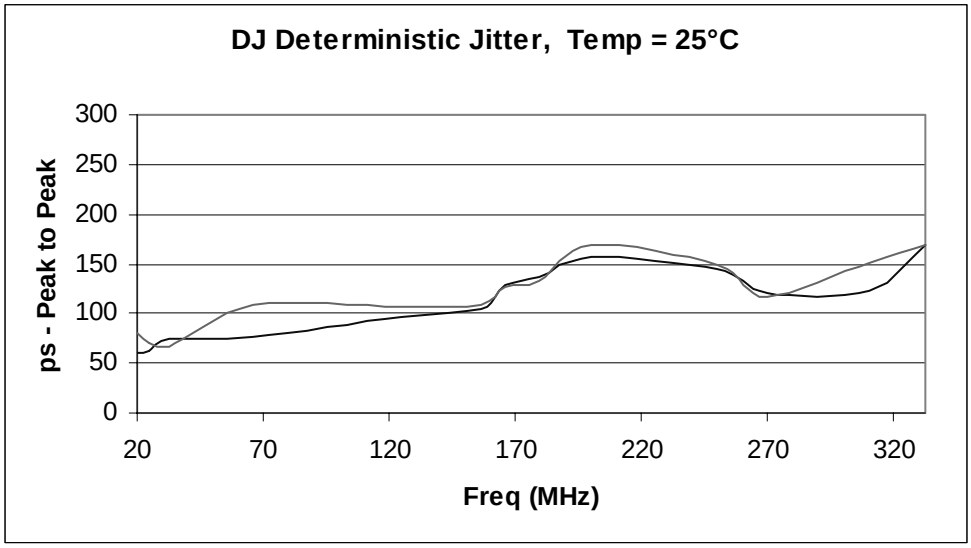



**Figure 5. Determinate Jitter**

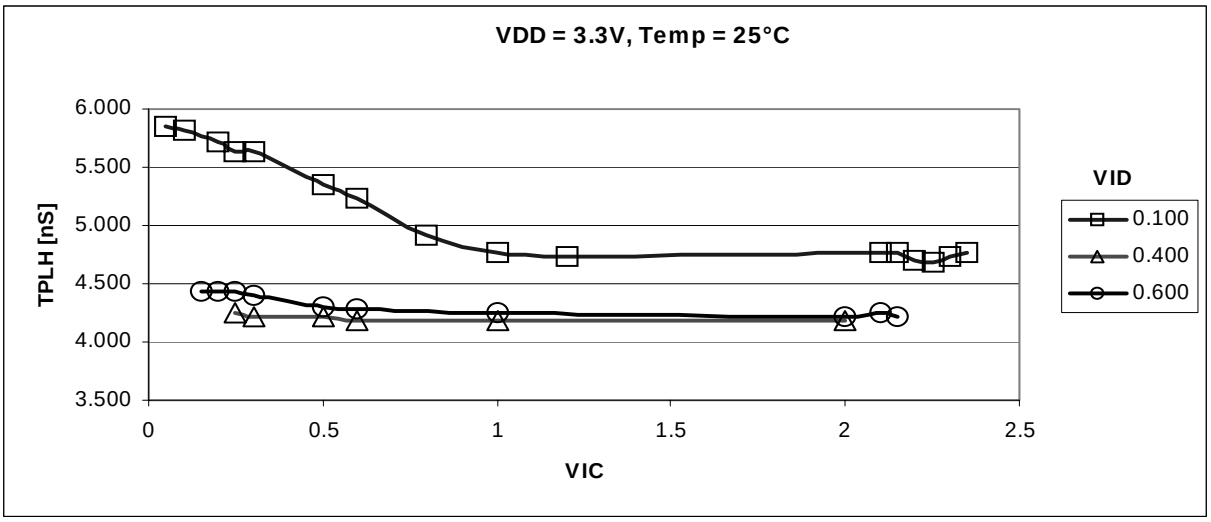



**Figure 6. TPLH vs VIC 3.3V, 50 MHz**

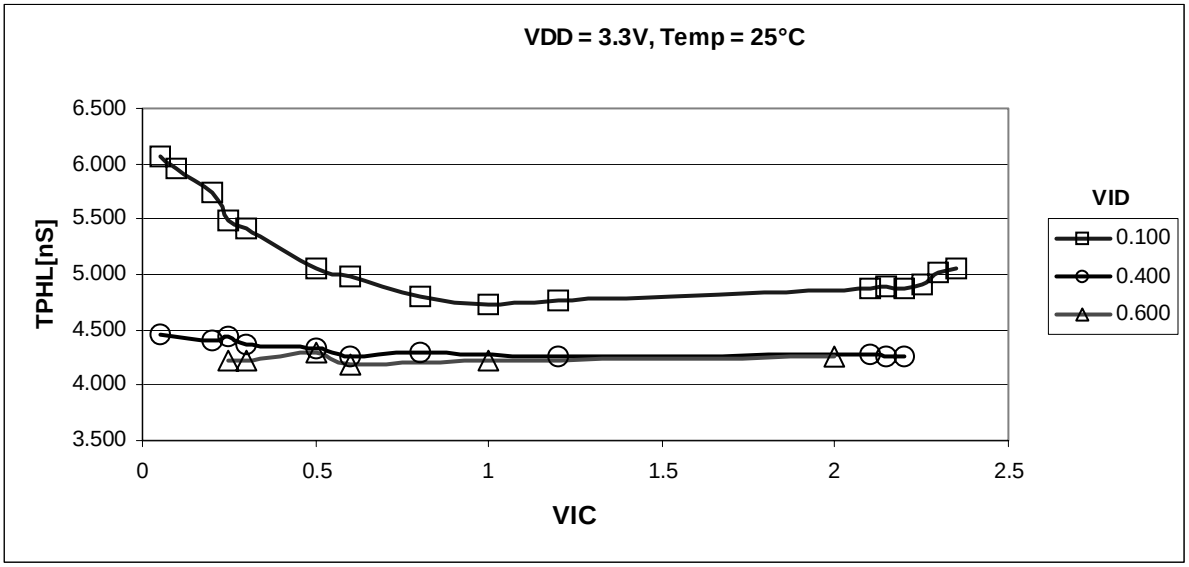



**Figure 7. TPHL vs. VIC 3.3V, 50 MHz**

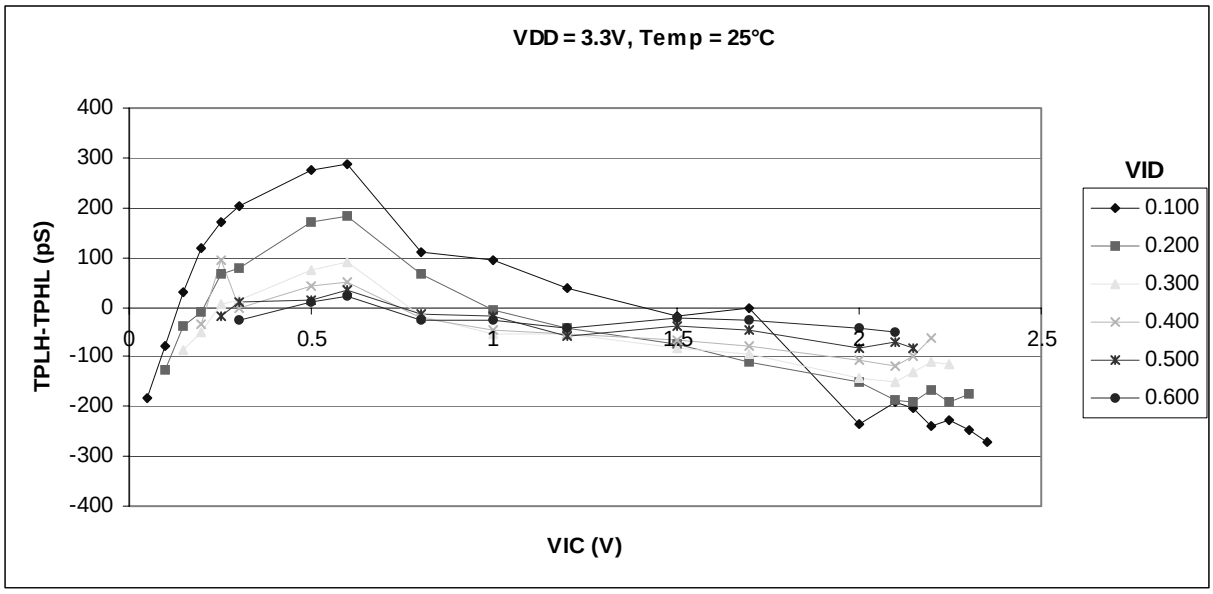



**Figure 8. TPLH-TPHL vs VIC 3.3V 50 MHz**

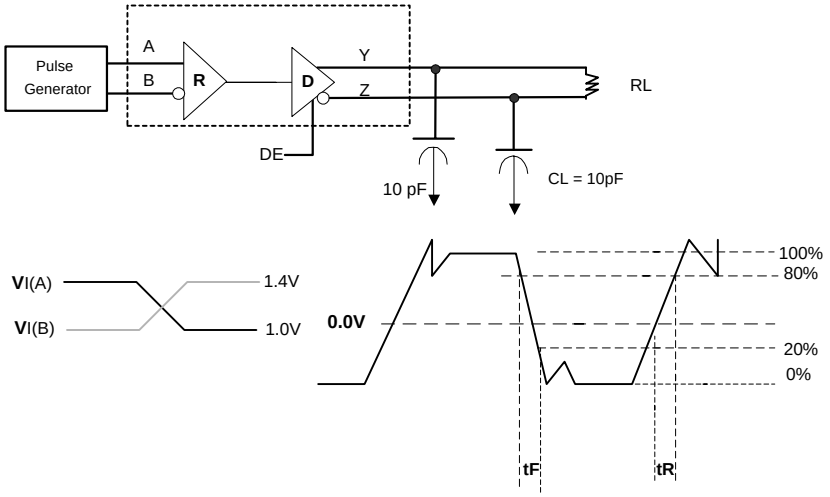



**Figure 9. Test Circuit and Voltage Definitions for the Differential Output Signal**[6,7,8]

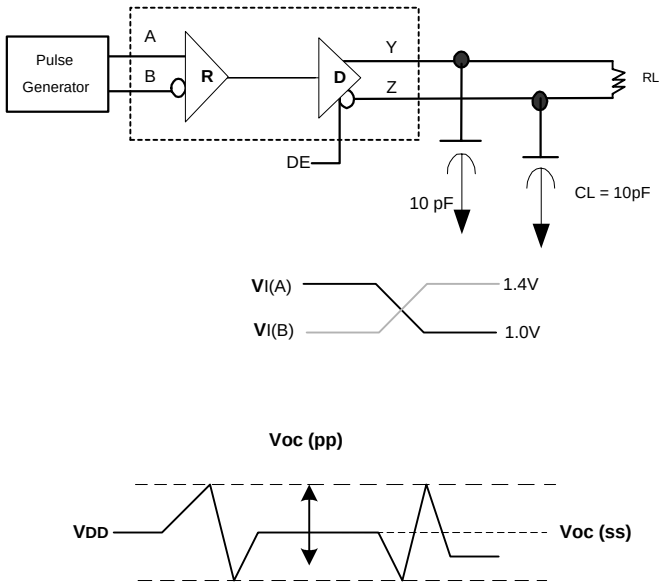



**Figure 10. Test Circuit & Voltage Definitions for the Driver Common-Mode Output Voltage**[6,7,8,9]

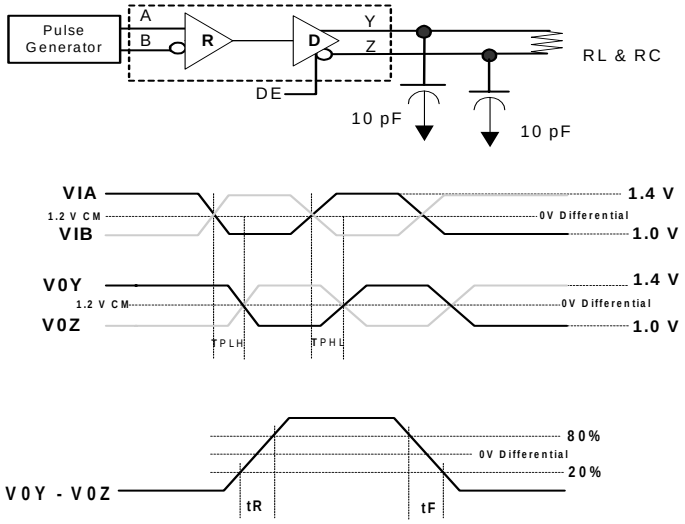



**Figure 11. Test Circuit & Voltage Definitions for the Driver Common-Mode Output Voltage**[6,10]

**Notes:**

6. All input pulses are supplied by a frequency generator with the following characteristics: $t_R$ and $t_F$ £ 1 nS; pulse rep rate = 50 MppS; pulse width = 10 ± 0.2 nS.
7. RL = 100 Ohm.
8. CL includes instrumentation and fixture capacitance within 6 mm of the DUT.
9. VOC measurement requires equipment with a 3-dB bandwith of at least 300 MHz.
10. RL = 100 Ohm ± 1%.

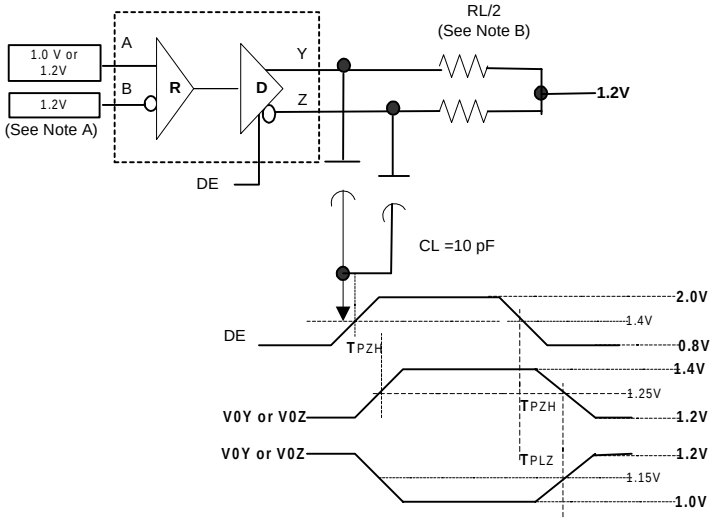



**Figure 12. Differential Receiver to Driver Propagation Delay and Driver Transition Time**[6,10,11]

## Application Engineering

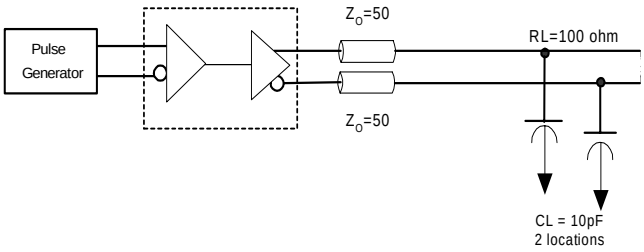



**Figure 13. Termination Scheme for 100-Ohm External Termination**

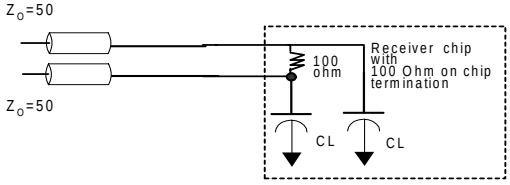



**Figure 14. Termination Scheme for 100-Ohm Self-termination Interface Chip**

## Typical Characteristics (@ $V_{DD}$ = 3.3V/TA = 25C)

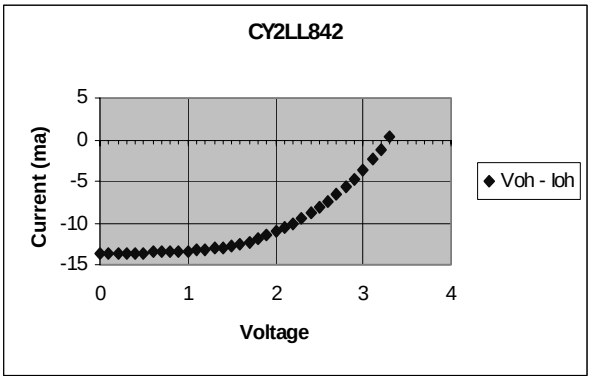



**Figure 15. VOH vs IOH**

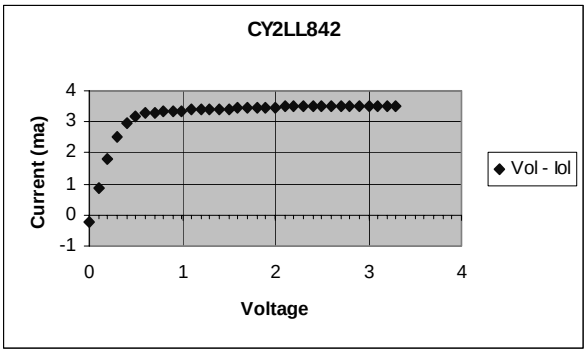



**Figure 16. VOL vs IOL**

**Note:**
11. Point to Point: RL = 100 Ohm ± 1% CL 3 pF.

**Table 7. Technical Notes on STD Drive (LL842, A and D) vs. High Drive (LL843, B and C)[12]**

| | A | B | C | D | Unit |
|---|---|---|---|---|---|
| VOX | 1.2 | 1.2 | 1.2 | 1.2 | V |
| DC Offset | 1.0 | 1.0 | 1.0 | 1.0 | V |
| VOD Min | 0.25 | 0.5 | 0.25 | 0.125 | V |
| VOD Max | 0.45 | 0.9 | 0.45 | 0.225 | V |
| T/Rise | 1.4 | 1.4 | 0.6 | 0.6 | ns |
| T/Fall | 1.4 | 1.4 | 0.6 | 0.6 | ns |

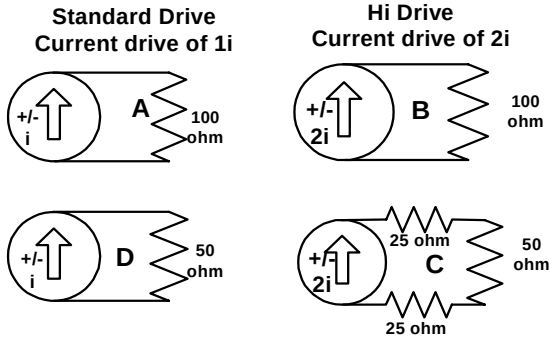


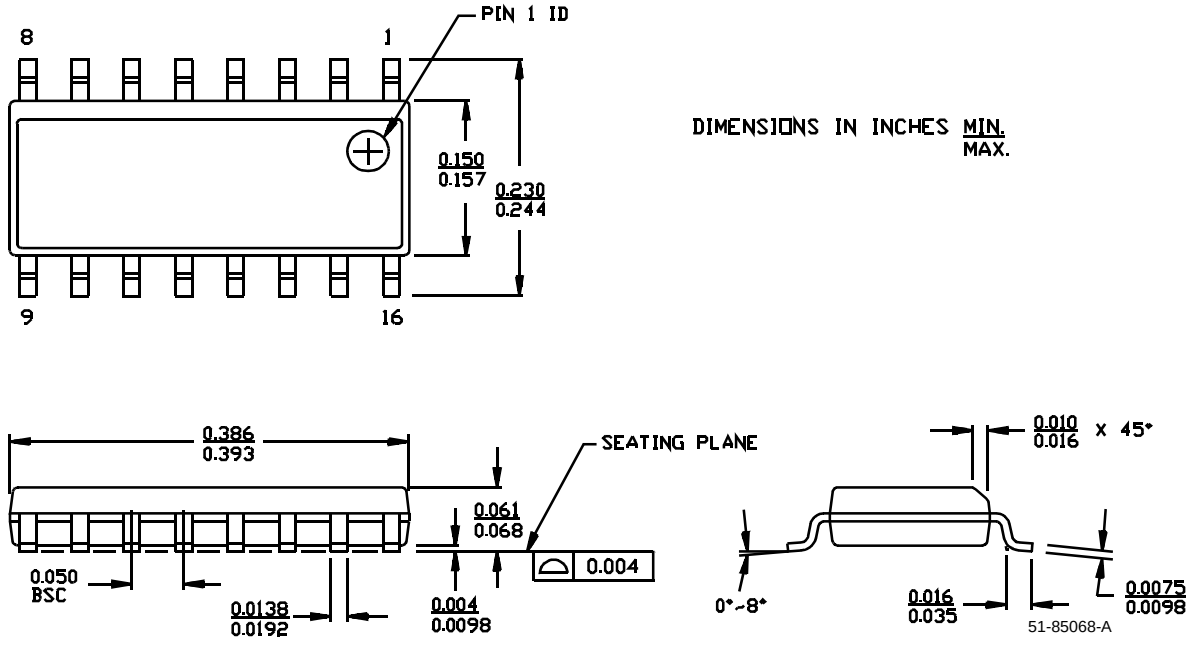

**Figure 17. Comparison Standard Drive ‘842 vs. High Drive ‘843**

## Ordering Information

| Part Number | Package Type | Product Flow |
|---|---|---|
| CY2LL842SI | 16-lead SOIC | Industrial, –40° to 85°C |
| CY2LL842SIT | 16-lead SOIC–Tape and Reel | Industrial, –40°C to 85°C |
| CY2LL842ZI | 16-lead TSSOP | Industrial, –40° to 85°C |
| CY2LL842ZIT | 16-lead TSSOP–Tape and Reel | Industrial, –40°C to 85°C |
| CY2LL842SC | 16-lead SOIC | Commercial, 0°C to 70°C |
| CY2LL842SCT | 16-lead SOIC–Tape and Reel | Commercial, 0°C to 70°C |
| CY2LL842ZC | 16-lead TSSOP | Commercial, 0°C to 70°C |
| CY2LL842ZCT | 16-lead TSSOP–Tape and Reel | Commercial, 0°C to 70°C |

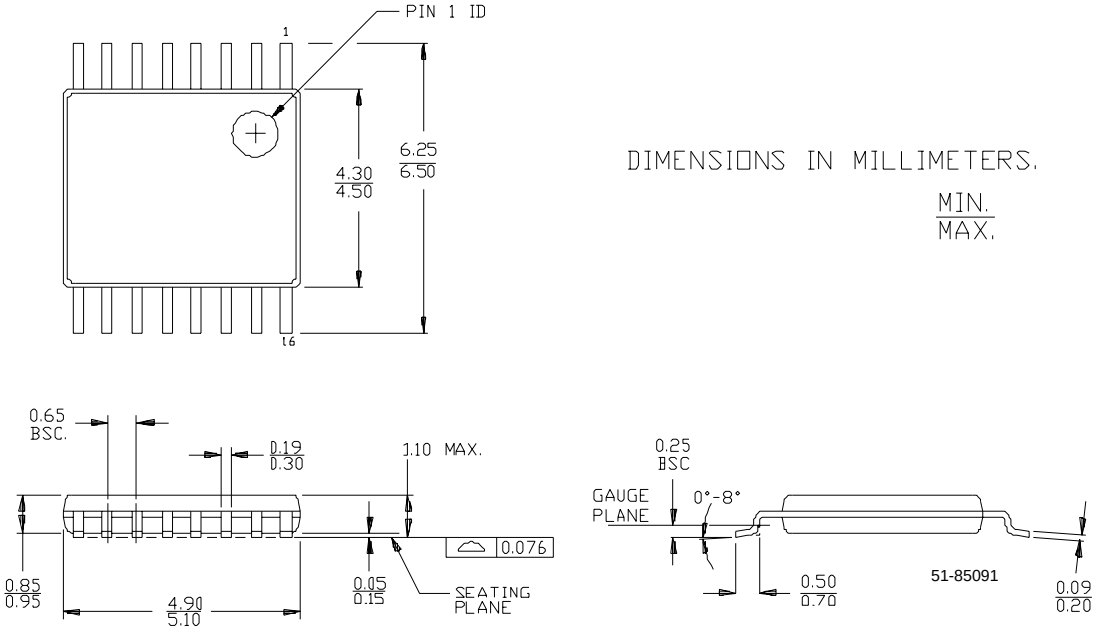
## Package Drawings

**16-lead (150-mil) Molded SOIC S16**




**Note:**
12. See *Figure 17*.

**16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16**

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| Document Title: ComLink™ Series CY2LL842 Two-channel LVDS Repeater/Mux<br>Document Number: 38-07063 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 116746 | 08/01/02 | HWT | New Data Sheet |
| *A | 122749 | 12/15/02 | RBI | Added power-up requirements to operating conditions information. |