CY74FCT16646T
CY74FCT162646T

16-Bit Registered Transceivers

Features

- **Low power, pin-compatible replacement for ABT functions**
- **FCT-C speed at 5.4 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000 V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Extended commercial range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16646T Features:

- **64 mA sink current (Com'l), 32 mA source current (Com'l)**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162646T Features:

- **Balanced output drivers: 24 mA**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A = 25°C**

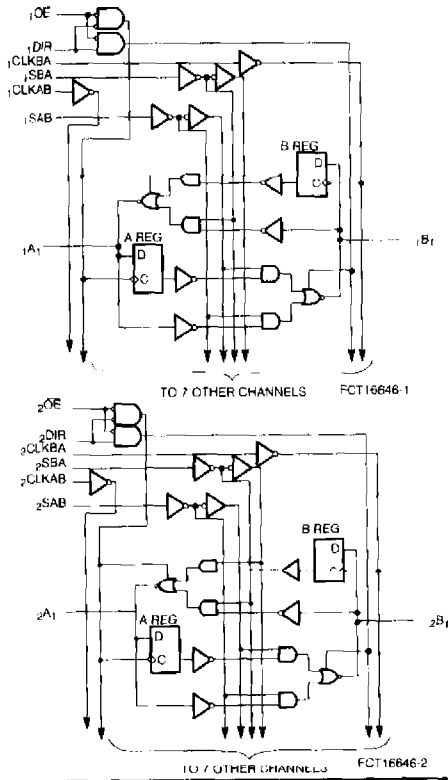
Functional Description

The CY74FCT16646T and CY74FCT162646T 16-bit transceivers are three-state, D-type registers, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Output Enable ($\overline{OE}$) and direction pins (DIR) are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the Output Enable ($\overline{OE}$) is Active LOW. In the isolation mode (Output Enable ($\overline{OE}$) HIGH), A data may be stored in the B register and/or B data may be stored in the A register. The output buffers are designed with a power-off disable feature that allows live insertion of boards.

The CY74FCT16646T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

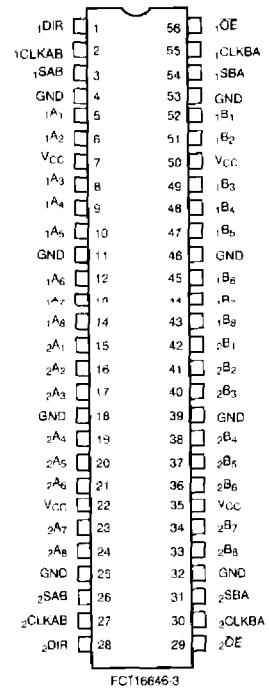
The CY74FCT162646T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162646T is ideal for driving transmission lines.

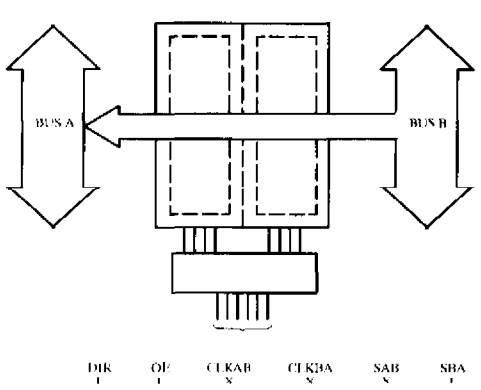
Logic Block Diagrams



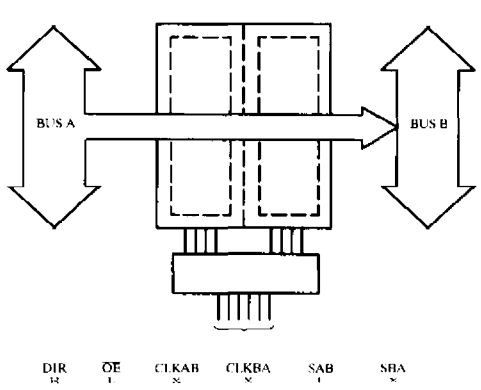
Pin Configuration

SSOP/TSSOP
Top View

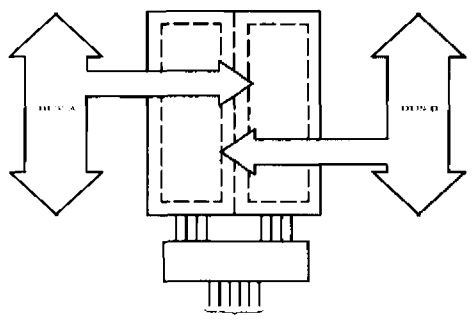




Real-Time Transfer
Bus B to Bus A

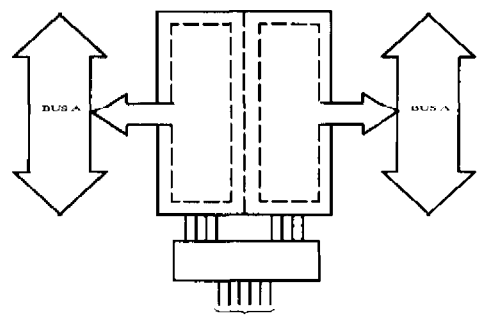


Real-Time Transfer
Bus A to Bus B



DIR	OE	CLKAB	CLKBA	SAB	SBA
H	H	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

Storage from
A and/or B



DIR[3]	OE	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Transfer Stored Data
to A and/or B

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Maximum Ratings[4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l	−55°C to +125°C
Ambient Temperature with Power Applied ..... Com'l	−55°C to +125°C
DC Input Voltage	−0.5V to +7.0V
DC Output Voltage	−0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	−60 to +120 mA
Power Dissipation	1.0W
Static Discharge Voltage ..... (per MIL-STD-883, Method 3015)	>2001V

Notes:

3. Cannot transfer data to A-bus and B-bus simultaneously.
4. Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics

Parameter	Description	Test Conditions[9]		Min.	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN}\leq 0.2V$ $V_{IN}\geq V_{CC}-0.2V$	—	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN}=3.4V[10]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max. Outputs Open DIR=OE=GND One-Bit Toggling 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max. Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle DIR=$\overline{OE}$=GND One-Bit Toggling f_1=5 MHz 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	—	1.3	3.2	
		V_{CC}=Max. Outputs Open f_0=10 MHz (CLKBA) 50% Duty Cycle DIR=$\overline{OE}$=GND Sixteen-Bits Toggling f_1=2.5 MHz 50% Duty Cycle	$V_{IN}=V_{CC}$ or V_{IN}=GND	—	3.8	6.5[13]	
			V_{IN}=3.4V or V_{IN}=GND	—	8.3	20.0[13]	

Notes:

9. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.

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Switching Characteristics Over the Operating Range

Parameter	Description	Cond.	74FCT16646T 74FCT162646T		74FCT16646AT 74FCT162646AT		74FCT16646CT 74FCT162646CT		Unit	Fig. No.[14]
			Min.[15]	Max.	Min.[15]	Max.	Min.[15]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L=50 pF R_L=500Ω	1.5	9.0	1.5	6.3	1.5	5.4	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time DIR or $\overline{OE}$ to Bus		1.5	14.0	1.5	9.8	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time DIR or $\overline{OE}$ to Bus		1.5	9.0	1.5	6.3	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		1.5	9.0	1.5	6.3	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		1.5	11.0	1.5	7.7	1.5	6.2	ns	1,5
t_{SU}	Set-Up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	ns	4
t_H	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	1.5	—	ns	4
t_W	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	5.0	—	ns	6
$t_{SK(O)}$	Output Skew[16]		—	0.5	—	0.5	—	0.5	ns	—

Ordering Information CY74FCT16646

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT16646CTPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16646CTPVC	O56	48-Lead (300-Mil) SSOP	
6.3	CY74FCT16646ATPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16646ATPVC	O56	48-Lead (300-Mil) SSOP	
9.0	CY74FCT16646TPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16646TPVC	O56	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162646

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT162646CTPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162646CTPVC	O56	48-Lead (300-Mil) SSOP	
6.3	CY74FCT162646ATPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162646ATPVC	O56	48-Lead (300-Mil) SSOP	
9.0	CY74FCT162646TPAC	Z56	48-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162646TPVC	O56	48-Lead (300-Mil) SSOP	

Notes:
14. See "Parameter Measurement Information" in the General Information Section.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. Skew any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.