CYPRESS

Features

- Low power, pin-compatible replacement for ABT functions
- FCT-C speed at 5.4 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000 V
- TSSOP (19.6-mil pitch) and SSOP (Z5-mil pitch) pael
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 5V \pm 10\%$
- CY74FCT16652T Features:
- 64 mA sink current (Com'l), 32 mA source current (Com'l)
- Typical V_{OLP} (ground bounce) ~1.0V at V_{CC} = 5V, T_A = 25°C

CY74FCT162652T Features:

- Balanced output drivers: 24 mA • Reduced system switching noise
- Typical $V_{OJ,P}$ (ground bounce) <10.0V at $V_{CC} = 5$ V, $T_A = 25^{\circ}C$
- **Functional Description**

These16-bit, high-speed, low-power, reg-istered transceivers that are organized as two independent 8-bit bus transceivers with three-state D-type registers and con-trol circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage regis-ters. OEAB and OEBA control plus are provided to control the transceiver functions. SAB and SBA control pins are pro-vided to select either real-time or stored data transfer.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the ap-propriate clock pins (CLKAB or CL.KBA), regardless of the select or en-

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16-Bit Registered Transceivers

able control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simulta-neously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state. The output buff-ers are designed with a power-off disable feature that allows live insertion of boards.

The CY74FCT16652T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162652T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal underhoout and reduced ground bounce. The CY74FCT162652T is ideal for driving transmission lines.

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Maximum Ratings^[4] (Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
Ambient Temperature with Power Applied
DC Input Voltage
DC Output Voltage
DC Output Current (Maximum Sink Current/Pin)60 to +120 mA

Note: • Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and func-tional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for ex-tended periods may affect reliability.

Power Dissipation 1.0W 9

Operating Range					
Range	Ambient Temperature	V _{CC}			
Commercial	-40°C to +85°C	$5V \pm 10\%$			



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Ordering Information CY74FCT16652

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT16652CTPAC	2.56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16652CTPVC	O56	56-Lead (300-Mil) SSOP	
6.3	CY74FCT16652ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16652ATPVC	O56	56-Lead (300-Mil) SSOP	
9.0	CY74FCT16652TPAC	Z56	56-Lead (240-Mit) TSSOP	Commercial
	CY74FCT16652TPVC	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162652

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
54	CV74FCT162652CTPAC	7.56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162652CTPVC	O56	56-Lead (300-Mil) SSOP	
6.3	CY74FCT162652ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercia
	CY74FCT162652ATPVC	O56	56-Lead (300-Mil) SSOP	
9.0	CY74FCT162652TPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162652TPVC	O56	56-Lead (300-Mil) SSOP	

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