



SCCS064B - August 1994 - Revised September 2001

20-Bit Buffers/Line Drivers

Features

- Ioff Supports Partial-Power-Down Mode Operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to +85°C
- $V_{CC} = 5V \pm 10\%$

CY74FCT16827T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C

CY74FCT162827T Features:

- · Balanced 24 mA output drivers
- · Reduced system switching noise
- Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A = 25°C

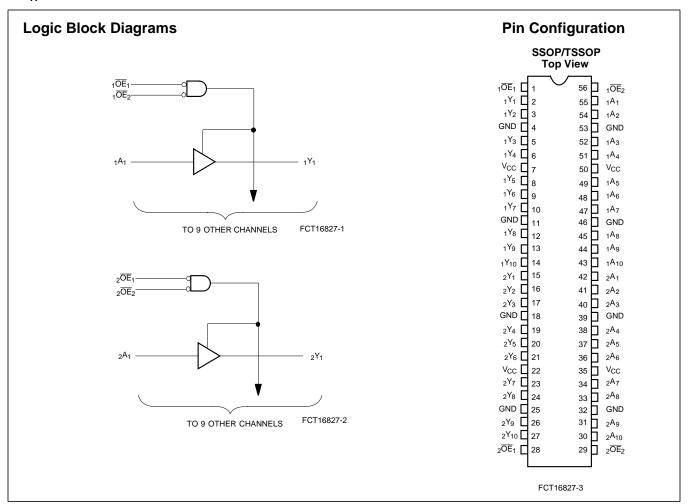
Functional Description

The CY74FCT16827T 20-bit buffer/line driver and the CY74FCT162827T 20-bit buffer/line driver provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. These parts can be used as a single 20-bit buffer or two 10-bit buffers. Each 10-bit buffer has a pair of NANDed \overline{OE} for increased flexibility.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16827T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162827T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162827T is ideal for driving transmission lines.





Pin Description

Name	Description					
ŌĒ	Output Enable Inputs (Active LOW)					
Α	Data Inputs					
Υ	Three-State Outputs					

Function Table^[1]

	Outputs		
OE ₁	ŌE ₂	Α	Y
L	L	L	L
L	L	Н	Н
Н	Х	Х	Z
X	Н	Х	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For use guidelines, not tested.)
Storage Temperature55°C to +125°C
Ambient Temperature with Power Applied –55°C to +125°C
DC Input Voltage0.5V to +7.0V
DC Output Voltage0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)60 to +120 mA
Power Dissipation1.0W
Static Discharge Voltage>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Input Hysteresis ^[5]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	μΑ
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	μΑ
l _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	μА
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	μА
Ios	Short Circuit Current ^[6]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
Io	Output Drive Current ^[6]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V ^[7]			±1	μΑ

Output Drive Characteristics for CY74FCT16827T

Parameter	Description	Test Conditions	Test Conditions Min. Typ. ^[4]		Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.Z = HIGH Impedance.

 Operation beyond the limits set forth may impair the useful life of the device. Unless noted, these limits are over the operating free-air temperature range. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

 Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.

 This parameter is specified but not tested.

- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, Ios tests should be performed last.
- 7. Tested at +25°C.



Output Drive Characteristics for CY74FCT162827T

Parameter	Description	Test Conditions	Min.	Typ. ^[4]	Max.	Unit
I _{ODL}	Output LOW Current ^[6]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[6]	V_{CC} =5V, V_{IN} = V_{IH} or V_{IL} , V_{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance^[5] ($T_A = +25^{\circ}C$, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. ^[4]	Max.	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Condi	tions	Min.	Typ. ^[4]	Max.	Unit
I _{CC}			$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} = 0.2V$	_	5	500	μΑ
Δl _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max.	V _{IN} =3.4V ^[8]	_	0.5	1.5	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE ₁ =OE ₂ =GND,	V _{IN} =V _{CC} or V _{IN} =GND	_	60	100	μA/MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., f ₁ =10 MHz,	V _{IN} =V _{CC} or V _{IN} =GND	_	0.6	1.5	mA
		50% Duty Cycle, Outputs Open, One Bit Toggling, OE ₁ =OE ₂ =GND	V _{IN} =3.4V or V _{IN} =GND	_	0.9	2.3	
		V _{CC} =Max., f ₁ =2.5 MHz,	V _{IN} =V _{CC} or V _{IN} =GND	_	3.0	5.5 ^[11]	
	(-	50% Duty Cycle, Outputs Open, Twenty Bits Toggling, $\overline{\text{OE}}_1 = \overline{\text{OE}}_2 = \overline{\text{GND}}$	V _{IN} =3.4V or V _{IN} =GND	_	8.0	20.5 ^[11]	

Notes:

8. Per TTL driven input (V_{IN} =3.4V); all other inputs at V_{CC} or GND.

This parameter is not directly testable, but is derived for use in Total Power Supply calculations. $\begin{array}{ll}
l_{C} &= l_{QUIESCENT} + l_{INPUTS} + l_{DYNAMIC} \\
l_{C} &= l_{CC} + \Delta l_{CC} D_{H} N_{T} + l_{CCD} (f_{0}/2 + f_{1}N_{1}) \\
l_{CC} &= Quiescent Current with CMOS input levels
\end{array}$

 $\begin{array}{lll} \Delta I_{CC} &=& \text{Power Supply Current for a TTL HIGH input } (V_{IN} = 3.4V) \\ D_H &=& \text{Duty Cycle for TTL inputs HIGH} \\ N_T &=& \text{Number of TTL inputs at } D_H \end{array}$

I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)

= Clock frequency for registered devices, otherwise zero

= Input signal frequency

= Number of inputs changing at f₁

All currents are in milliamps and all frequencies are in megahertz.

11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.



Switching Characteristics Over the Operating $\mathsf{Range}^{[12]}$

			CY74FCT		CY74FCT	162827BT		
Parameter	Description	Condition ^[13]	Min.	Max.	Min.	Max.	Unit	Fig. No. ^[13]
t _{PLH} t _{PHL}	Propagation Delay A to Y	C_L =50 pF R_L =500 Ω	1.5	8.0	1.5	5.0	ns	1, 3
		C_L =300 pF R_L =500 Ω	1.5	15.0	1.5	13.0		
t _{PZH} t _{PZL}	Output Enable Time OE to Y	C_L =50 pF R_L =500 Ω	1.5	12.0	1.5	8.0	ns	1, 7, 8
		C_L =300 pF R_L =500 Ω	1.5	23.0	1.5	15.0		
t _{PHZ} t _{PLZ}	Output Disable Time OE to Y	$C_L=5 pF$ $R_L=500\Omega$	1.5	9.0	1.5	6.0	ns	1, 7, 8
		C_L =50 pF R_L =500 Ω	1.5	10.0	1.5	7.0		
t _{SK(O)}	Output Skew ^[14]		_	0.5	_	0.5	ns	_

			CY74FCT16827CT CY74FCT162827CT			
Parameter	Description	Condition ^[12]	Min.	Max.	Unit	Fig. No. ^[13]
t _{PLH}	Propagation Delay A to Y	C_L =50 pF R_L =500 Ω	1.5	4.2	ns	1, 3
		C_L =300 pF R_L =500 Ω	1.5	10.0		
t _{PZH} t _{PZL}	Output Enable Time OE to Y	C_L =50 pF R_L =500 Ω	1.5	5.6	ns	1, 7, 8
		C_L =300 pF R_L =500 Ω	1.5	14.0		
t _{PHZ}	Output Disable Time OE to Y	$C_L=5 pF$ $R_L=500\Omega$	1.5	5.7	ns	1, 7, 8
		C_L =50 pF R_L =500 Ω	1.5	6.0		
t _{SK(O)}	Output Skew ^[14]		_	0.5	ns	_

Notes:

Minimum limits are specified but not tested on Propagation Delays.
 See "Parameter Measurement Information" in the General Information section.
 Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.



Ordering Information CY74FCT16827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT16827CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16827CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT16827ATPVC/PVCT	Z56	56-Lead (240-Mil) SSOP	Industrial

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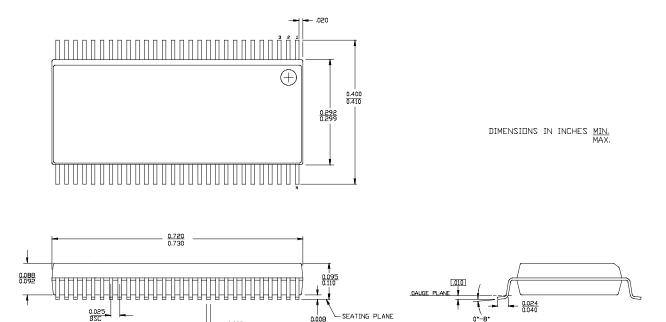
Ordering Information CY74FCT162827

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	74FCT162827CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162827CTPVC	Z56	56-Lead (240-Mil) SSOP	
	74FCT162827CTPVCT	Z56	56-Lead (240-Mil) SSOP	
5.0	CY74FCT162827BTPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162827BTPVCT	O56	56-Lead (300-Mil) SSOP	
8.0	CY74FCT162827ATPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162827ATPVCT	O56	56-Lead (300-Mil) SSOP	

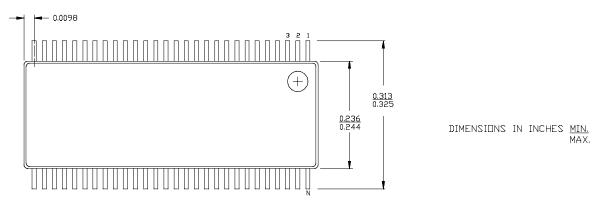


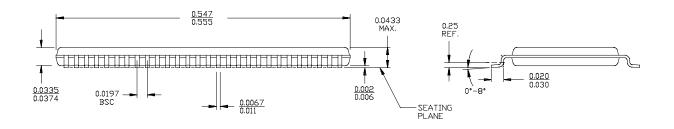
Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56









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PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
74FCT162827ATPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162827A	Samples
74FCT162827ATPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162827A	Samples
74FCT162827BTPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162827B	Samples
74FCT162827CTPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162827C	Samples
74FCT162827ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
74FCT162827ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
74FCT16827ATPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827A	Samples
74FCT16827ATPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827A	Samples
74FCT16827ATPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827A	Samples
74FCT16827CTPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827C	Samples
74FCT16827CTPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827C	Samples
74FCT16827CTPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827C	Samples
74FCT16827CTPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827C	Samples
CY74FCT162827ATPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162827A	Samples
CY74FCT162827BTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162827B	Samples
CY74FCT162827ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT162827ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16827ATPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827A	Samples
CY74FCT16827ATPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827A	Samples





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Orderable Device	Status	Package Type	Package	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing			(2)		(3)		(4)	
CY74FCT16827CTPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827C	Samples
CY74FCT16827CTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827C	Samples
CY74FCT16827CTPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16827C	Samples
CY74FCT16827ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16827ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16827ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
CY74FCT16827ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
FCT162827ATPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162827A	Samples
FCT162827ATPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162827A	Samples
FCT162827CTPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162827C	Samples
FCT162827CTPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162827C	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



PACKAGE OPTION ADDENDUM

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(4) Only one of markings shown within the brackets will appear on the physical device.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

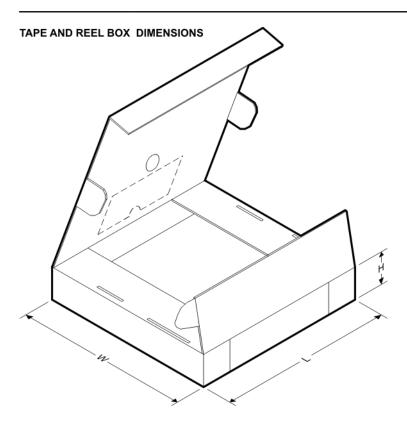
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162827ATPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
74FCT162827CTPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
CY74FCT16827ATPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
CY74FCT16827CTPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
CY74FCT16827CTPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
74FCT162827ATPACT	TSSOP	DGG	56	2000	367.0	367.0	45.0	
74FCT162827CTPACT	TSSOP	DGG	56	2000	367.0	367.0	45.0	
CY74FCT16827ATPACT	TSSOP	DGG	56	2000	367.0	367.0	45.0	
CY74FCT16827CTPACT	TSSOP	DGG	56	2000	367.0	367.0	45.0	
CY74FCT16827CTPVCT	SSOP	DL	56	1000	367.0	367.0	55.0	

DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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