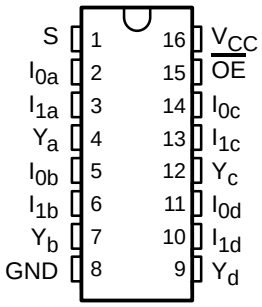
- **Function and Pinout Compatible With FCT and F Logic**
- **25-Ω Output Series Resistors to Reduce Transmission-Line Reflection Noise**
- **TTL Output Level Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **12-mA Output Sink Current**
  15-mA Output Source Current
- **3-State Outputs**

Q OR SO PACKAGE
(TOP VIEW)



description

The CY74FCT2257T has four identical two-input multiplexers that select four bits of data from two sources under the control of a common data-select (S) input. The I_0 inputs are selected when S is low, and the I_1 inputs are selected when S is high. Data appears at the output in noninverted form for the CY74FCT2257T. On-chip termination resistors at the outputs reduce system noise caused by reflections. The CY74FCT2257T can replace the FCT257T to reduce noise in an existing design.

The CY74FCT2257T is a logic implementation of a four-pole, two-position switch, in which the position of the switch is determined by the logic levels supplied to S. Outputs are forced to the high-impedance off state when the output-enable ($\overline{OE}$) input is high.

All but one device must be in the high-impedance state to prevent currents from exceeding the maximum ratings if outputs are tied together. Design of the $\overline{OE}$ signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	DESCRIPTION
I	Data inputs
S	Common data-select input
$\overline{OE}$	Output-enable input (active low)
Y	Data outputs

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	4.3	CY74FCT2257CTQCT	FR257-3
	SOIC – SO	Tube	4.3	CY74FCT2257CTSOC	FCT2257C
		Tape and reel	4.3	CY74FCT2257CTSOCT	
	QSOP – Q	Tape and reel	5	CY74FCT2257ATQCT	FR257-1

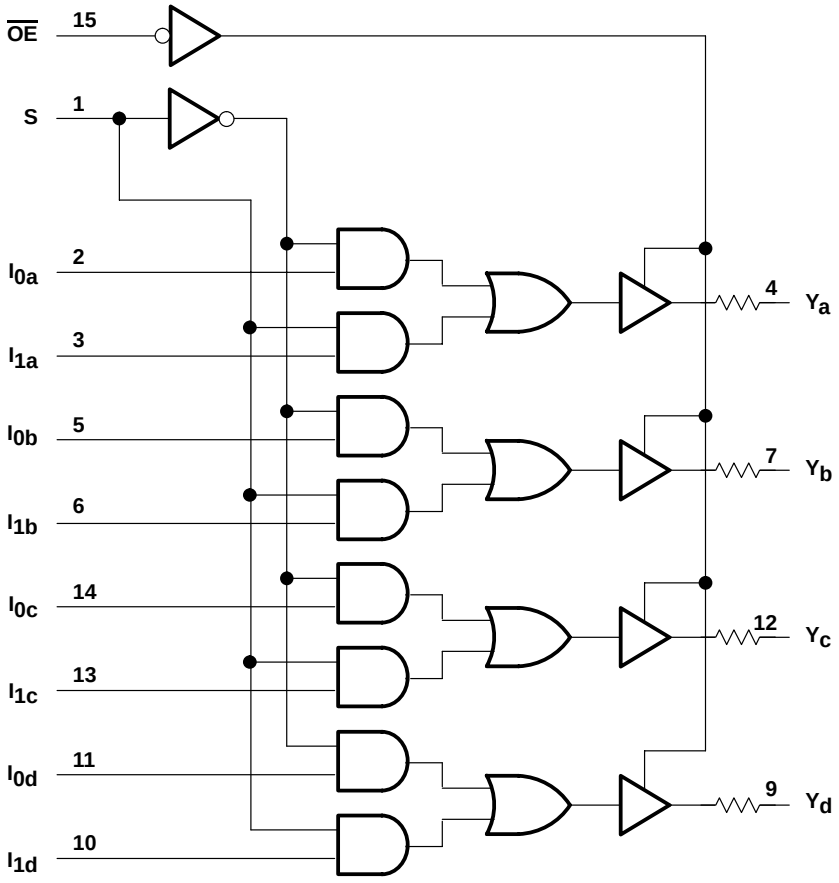
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High logic level, L = Low logic level, X = Don't care, Z = High-impedance (off) state

logic diagram (positive logic)



absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential . . . . . –0.5 V to 7 V
DC input voltage range . . . . . –0.5 V to 7 V
DC output voltage range . . . . . –0.5 V to 7 V
DC output current (maximum sink current/pin) . . . . . 120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package . . . . . 90°C/W
SO package . . . . . 57°C/W
Ambient temperature range with power applied, T_A . . . . . –65°C to 135°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_{IN} = –18 mA			–0.7	–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –15 mA		2.4	3.3		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 12 mA			0.3	0.55	V
R_{out}	V_{CC} = 4.75 V,	I_{OL} = 12 mA		20	25	40	Ω
V_{hys}	All inputs				0.2		V
I_{IH}	V_{CC} = 5.25 V,	V_{IN} = 2.7 V				±1	µA
I_{IL}	V_{CC} = 5.25 V,	V_{IN} = 0.5 V				±1	µA
I_{OZH}	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V				10	µA
I_{OZL}	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V				–10	µA
I_{OS}‡	V_{CC} = 5.25 V,	V_{OUT} = 0 V		–60	–120	–225	mA
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V				±1	µA
I_{CC}	V_{CC} = 5.25 V,	$V_{IN} \le$ 0.2 V,	$V_{IN} \ge V_{CC}$ – 0.2 V		0.1	0.2	mA
ΔI_{CC}	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open				0.5	2	mA
I_{CCD}¶	V_{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}$ = GND, $V_{IN} \le$ 0.2 V or $V_{IN} \ge V_{CC}$ – 0.2 V				0.06	0.12	mA/ MHz
I_C#	V_{CC} = 5.25 V, Outputs open, $\overline{OE}$ = GND	One bit switching at f_1 = 10 MHz at 50% duty cycle	$V_{IN} \le$ 0.2 V or $V_{IN} \ge V_{CC}$ – 0.2 V		0.7	1.4	mA
			V_{IN} = 3.4 V or GND		1	2.4	
		Four bits switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le$ 0.2 V or $V_{IN} \ge V_{CC}$ – 0.2 V		0.7	1.4‖	
			V_{IN} = 3.4 V or GND		1.7	5.4‖	
C_i					5	10	pF
C_o					9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current
I_{CC} = Power-supply current with CMOS input levels
ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)
D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
f_0 = Clock frequency for registered devices, otherwise zero
f_1 = Input signal frequency
N_1 = Number of inputs changing at f_1

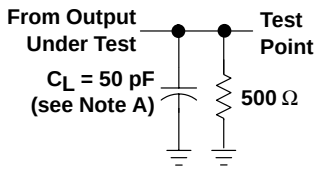
All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

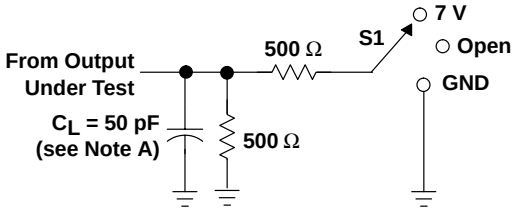
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT2257AT		CY74FCT2257CT		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	I_a or I_b	Y	1.5	5	1.5	4.7	ns
t_{PHL}			1.5	5	1.5	4.7	
t_{PLH}	S	Y	1.5	7	1.5	5.2	ns
t_{PHL}			1.5	7	1.5	5.2	
t_{PZH}	$\overline{OE}$	Y	1.5	7	1.5	6	ns
t_{PZL}			1.5	7	1.5	6	
t_{PHZ}	$\overline{OE}$	Y	1.5	5.5	1.5	5	ns
t_{PLZ}			1.5	5.5	1.5	5	

PARAMETER MEASUREMENT INFORMATION

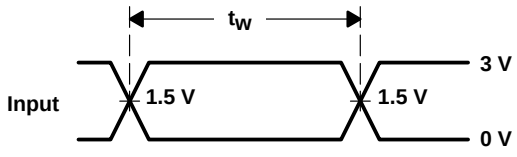


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

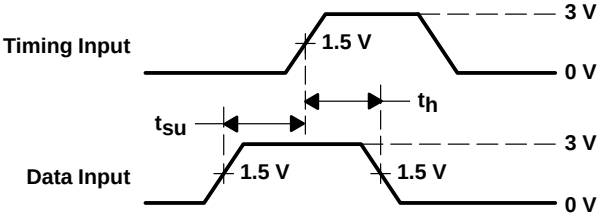


LOAD CIRCUIT FOR
3-STATE OUTPUTS

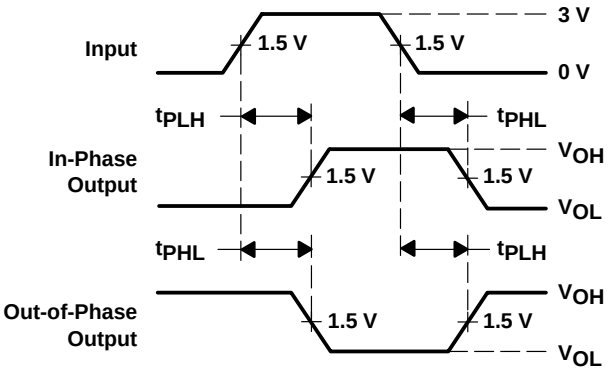
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



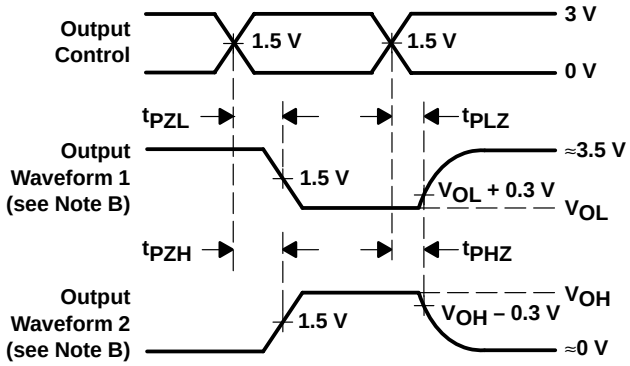
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
74FCT2257CTSOCTE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74FCT2257CTSOCTG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CY74FCT2257ATQCT	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT2257ATQCTE4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT2257ATQCTG4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
CY74FCT2257CTSOCT	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

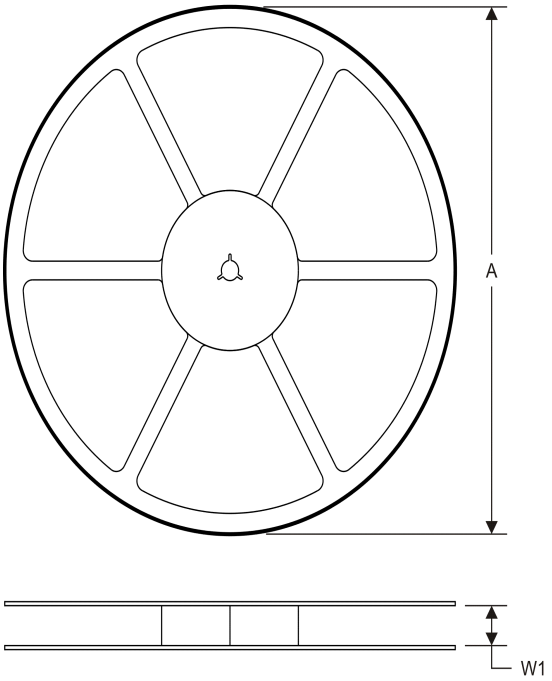
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

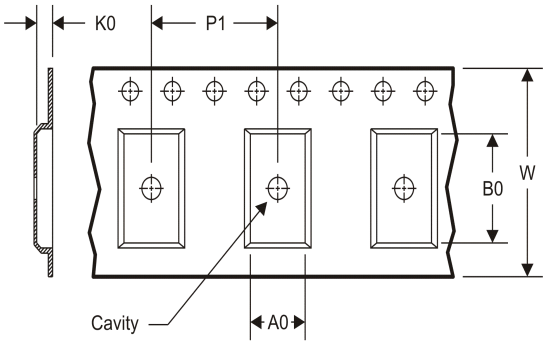
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



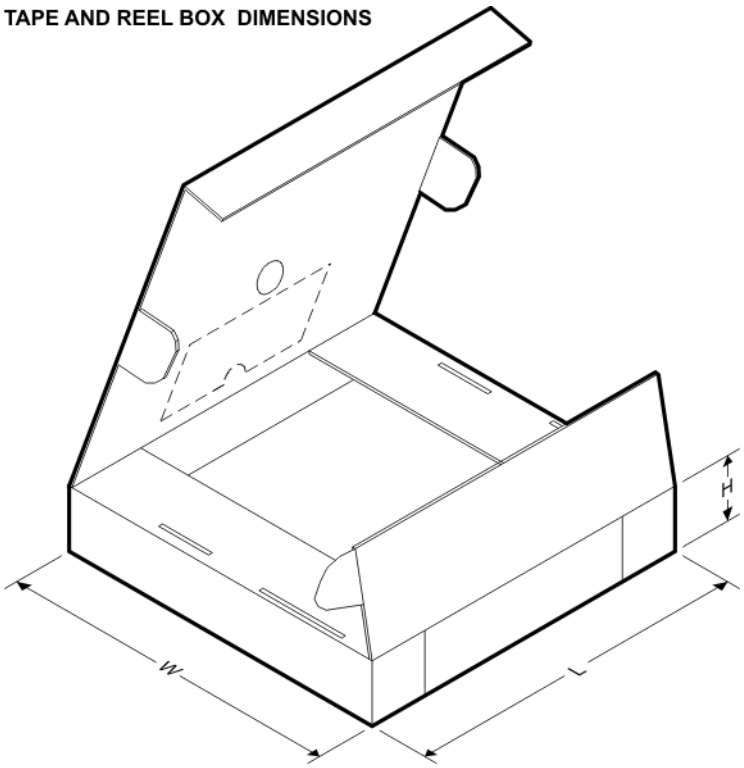
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT2257CTSOCT	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

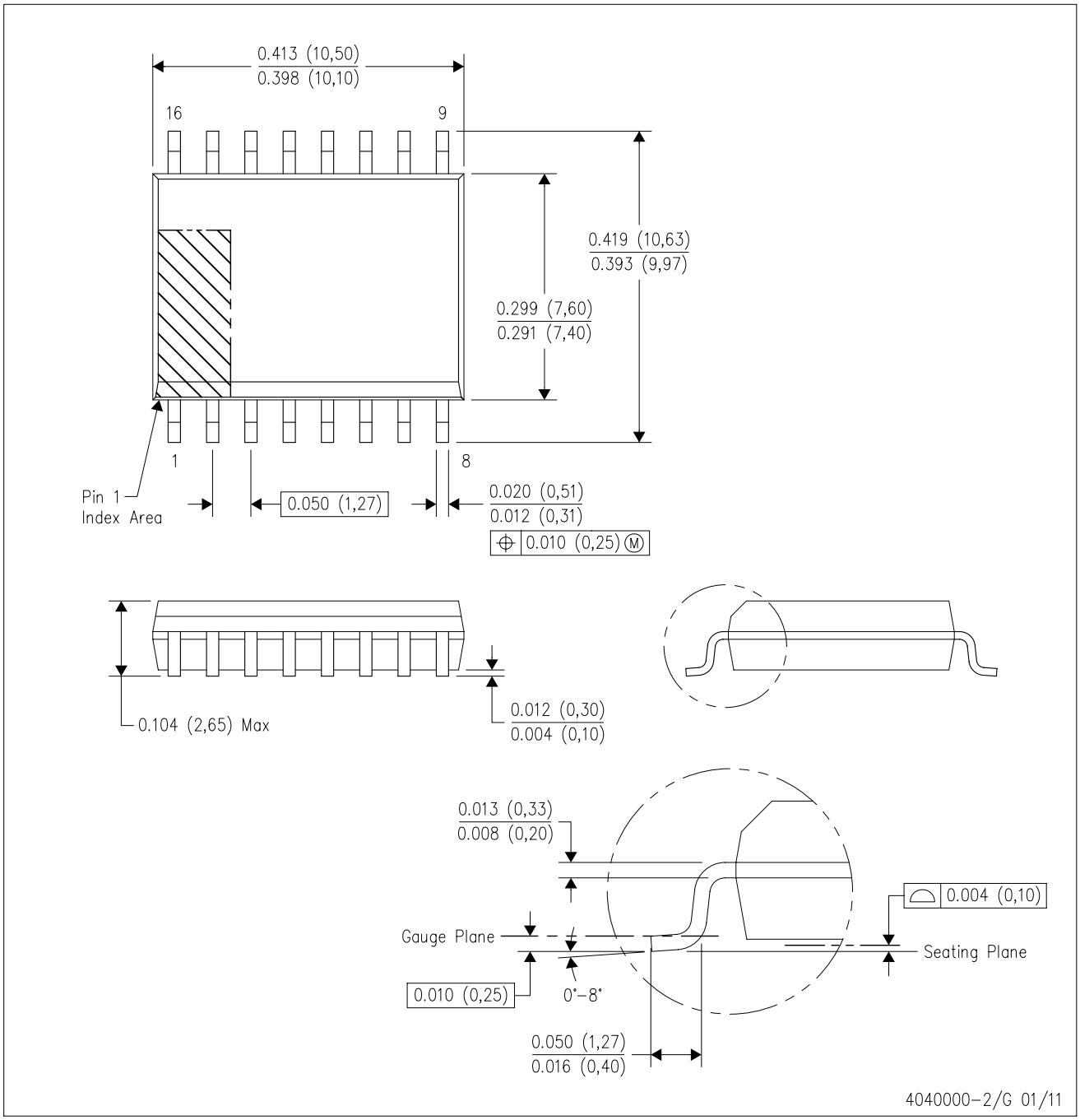
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

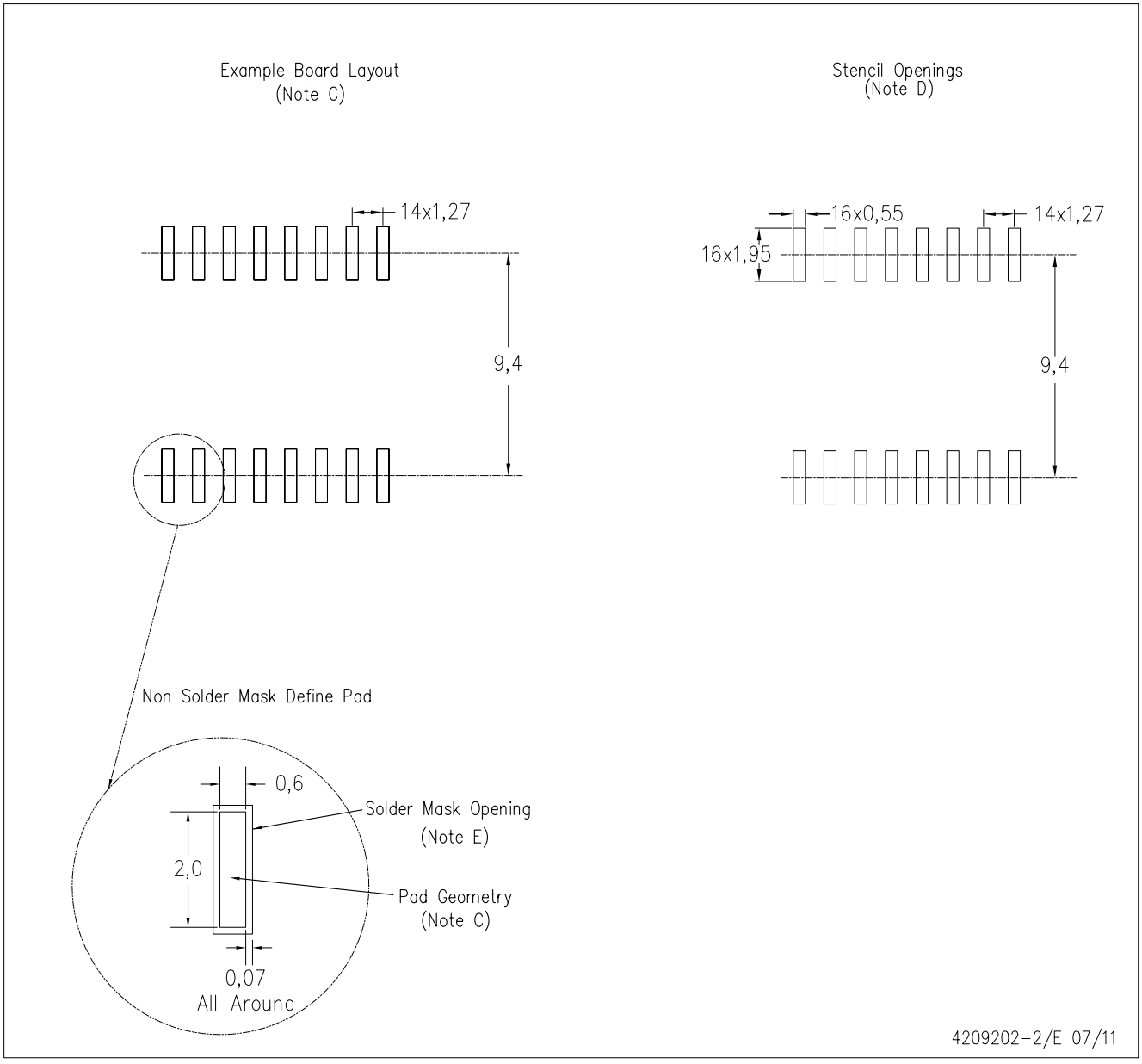
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT2257CTSOCT	SOIC	DW	16	2000	367.0	367.0	38.0

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



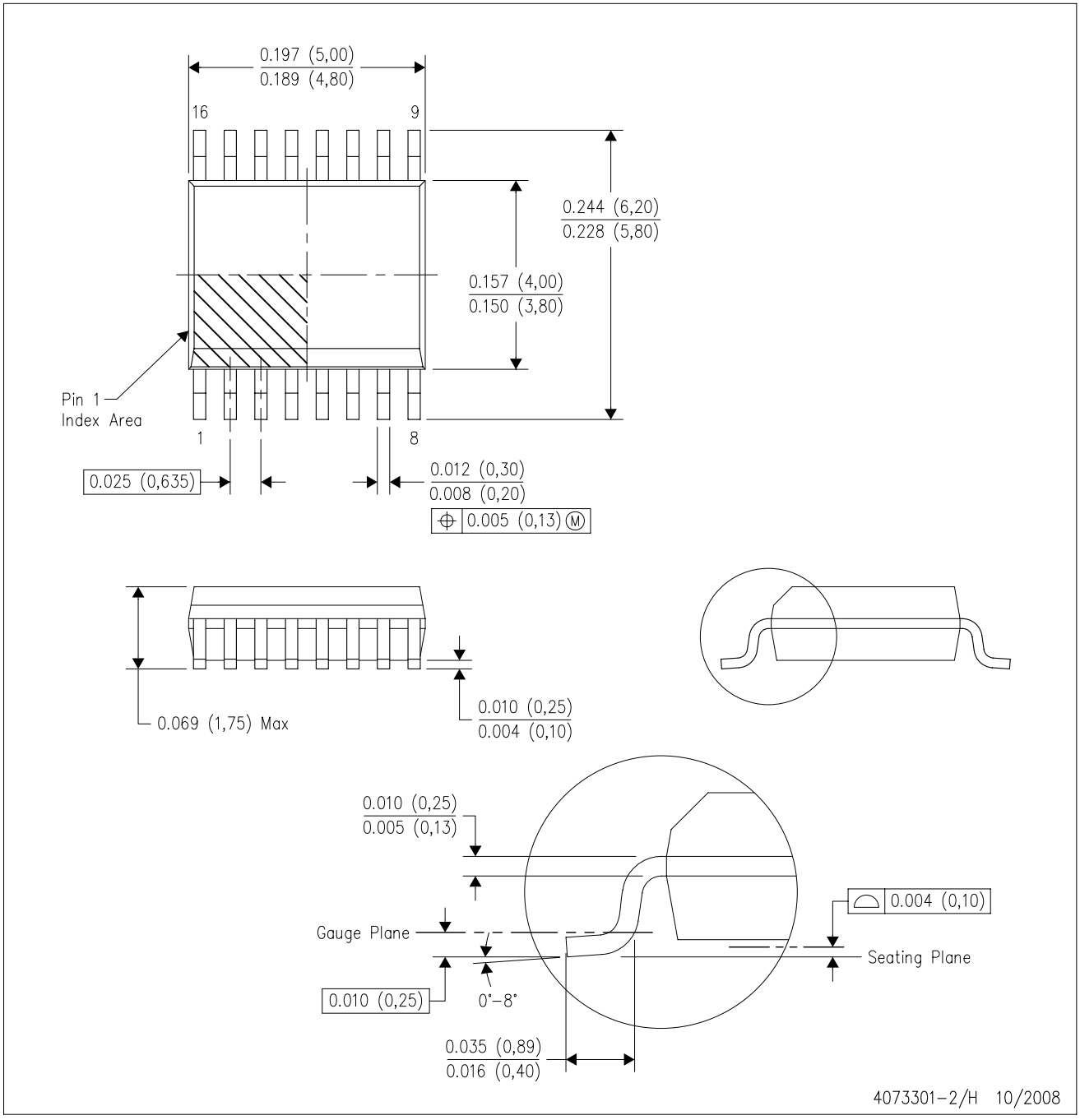
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



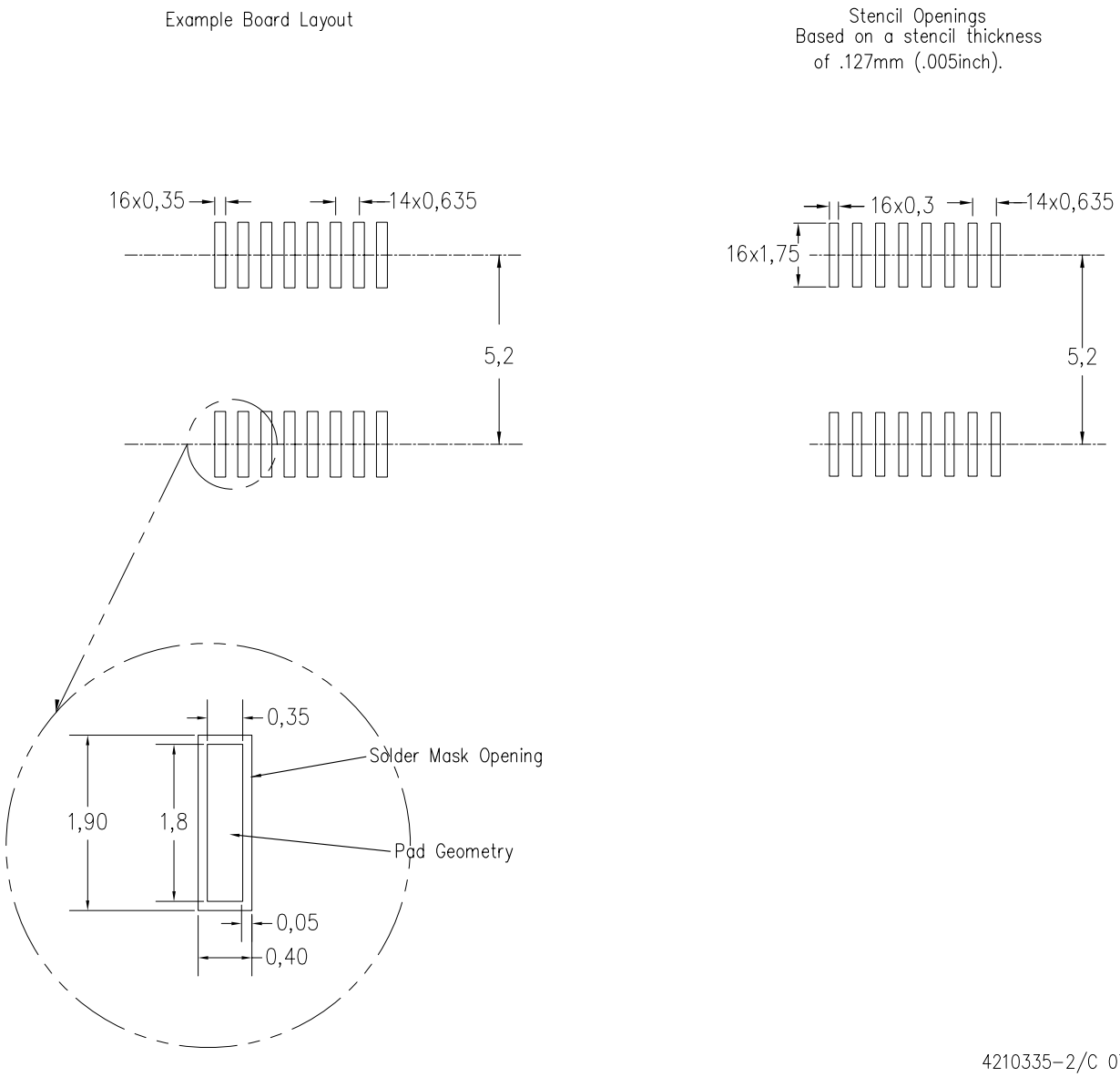
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

DBQ (R–PDSO–G16) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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