Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[7]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN} \le 0.2V$, $V_{IN} \ge V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	V_{CC}=Max., V_{IN}=3.4V,[10] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.06	0.12	mA/MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, f_0=$\overline{LEAB}$ = 10 MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, f_0=$\overline{LEAB}$ = 10 MHz, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, f_0=$\overline{LEAB}$ = 10 MHz, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC}-0.2V$	2.8	5.6[13]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, $\overline{CEAB}$ and $\overline{OEAB}$=LOW, $\overline{CEBA}$=HIGH, f_0=$\overline{LEAB}$ = 10 MHz, V_{IN}=3.4V or V_{IN}=GND	5.1	14.6[13]	mA

Notes:

10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

9

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.4	CY74FCT543DTSOC	S13	24-Lead (300-Mil) Molded SOIC	Commercial
	CY74FCT543DTQC	Q13	24-Lead (150-Mil) QSOP	
5.3	CY74FCT543CTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT543CTQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT543CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
6.1	CY54FCT543CTDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT543CTLMB	L64	28-Square Leadless Chip Carrier	
6.5	CY74FCT543ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT543ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT543ATSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT543ATDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT543ATLMB	L64	28-Square Leadless Chip Carrier	
8.5	CY74FCT543TPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT543TQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT543TSOC	S13	24-Lead (300-Mil) Molded SOIC	
10.0	CY54FCT543TDMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY54FCT543TLMB	L64	28-Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38-00264-A

9