CY7C1021CV26

1-Mbit (64 K × 16) Static RAM

Features

- Temperature Range
  - Automotive: –40 °C to 125 °C
- High speed
  - t_{AA} = 15 ns
- Optimized voltage range: 2.5 V to 2.7 V
- Low active power: 220 mW (Max)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- CMOS for optimum speed/power
- Available in Pb-free and non Pb-free 44-pin TSOP II, 44-pin (400-Mil) Molded SOJ and Pb-free 48-ball FBGA packages

Functional Description

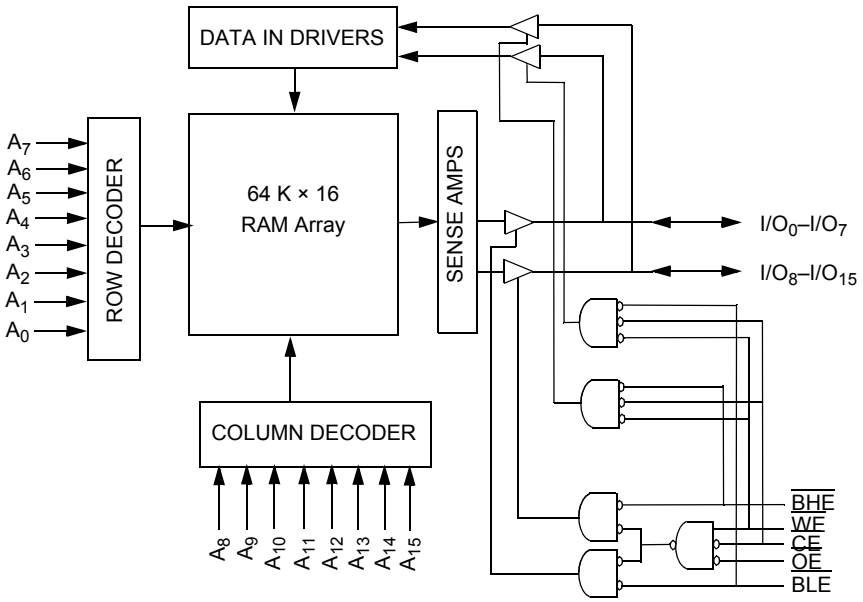
The CY7C1021CV26 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Logic Block Diagram



Contents

Selection Guide

Description [1]	-15	Unit
Maximum Access Time	15	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current	10	mA

Pin Configuration

Figure 1. 44-pin SOJ/TSOP II [2]

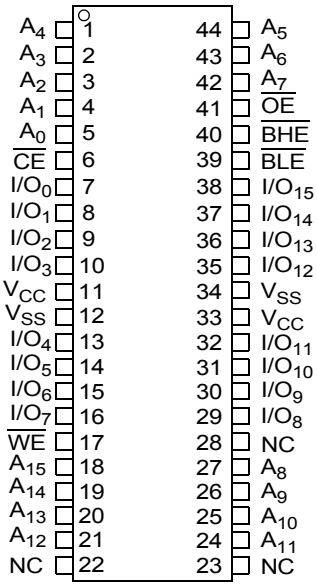
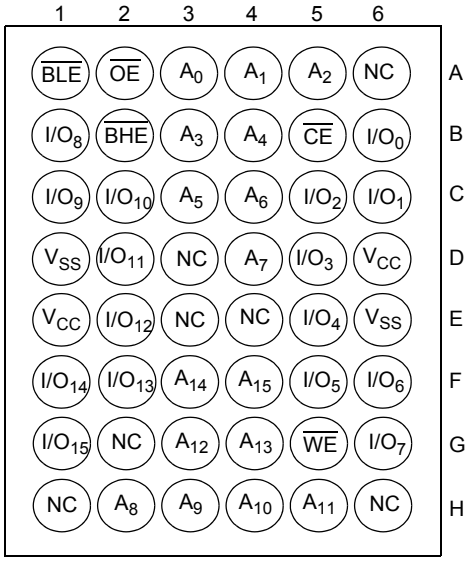


Figure 2. 48-ball FBGA Pinout [2]



Notes
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25$ °C.
2. NC pins are not connected on the die.

Pin Definitions

Pin Name	Pin Number	I/O Type	Description
A_0–A_{15}	1–5, 18–21, 24–27, 42–44	Input	**Address Inputs used to select one of the address locations.**
I/O_0–I/O_{15}	7–10, 13–16, 29–32, 35–38	Input/Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	**No Connects**. This pin is not connected to the die.
$\overline{WE}$	17	Input/Control	**Write Enable Input, active LOW**. When selected LOW, a Write is conducted. When selected HIGH, a Read is conducted.
$\overline{CE}$	6	Input/Control	**Chip Enable Input, active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{BHE}$, $\overline{BLE}$	40, 39	Input/Control	**Byte Write Select Inputs, active LOW**. $\overline{BHE}$ controls I/O_{15}–I/O_8, $\overline{BLE}$ controls I/O_7–I/O_0.
$\overline{OE}$	41	Input/Control	**Output Enable, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When de-asserted HIGH, I/O pins are tri-stated, and act as input data pins.
V_{SS}	12, 34	Ground	**Ground for the device**. Should be connected to ground of the system.
V_{CC}	11, 33	Power Supply	**Power Supply inputs to the device.**

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND[3] .....–0.5 V to +4.6 V

DC voltage applied to outputs in high Z state[3] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage[3] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage ..... > 2001 V (per MIL-STD-883, method 3015)

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Automotive	–40 °C to +125 °C	2.5 V–2.7 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-15		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –1.0 mA	2.3	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 1.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage[3]		–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}	–3	+3	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{CC}, output disabled	–3	+3	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	–	80	mA
I_{SB1}	Automatic CE power-down Current —TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	15	mA
I_{SB2}	Automatic CE power-down Current —CMOS inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	–	10	mA

Capacitance

Parameter [4]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 2.6 V	8	pF
C_{OUT}	Output capacitance		8	pF

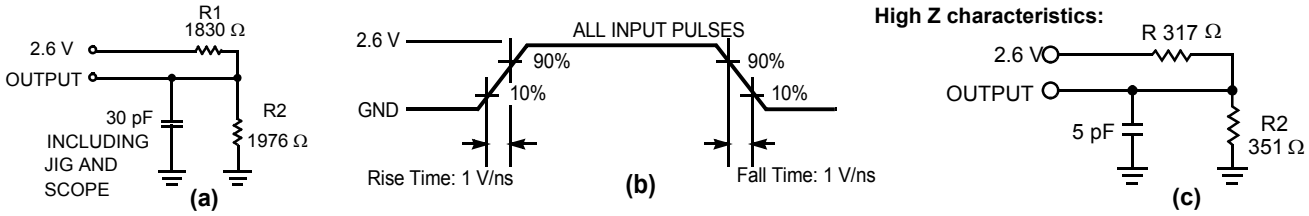
Thermal Resistance

Parameter [4]	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	76.92	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		15.86	°C/W

Notes
3. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 0.5 V for pulse durations of less than 20 ns.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [5]



Switching Characteristics

Over the Operating Range

Parameter [6]	Description	-15		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	15	–	ns
t_{AA}	Address to data valid	–	15	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	7	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z[7]	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[7, 8]	–	7	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z[7]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z[7, 8]	–	7	ns
t_{PU}[9]	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}[9]	$\overline{CE}$ HIGH to power-down	–	15	ns
t_{DBE}	Byte enable to data valid	–	7	ns
t_{LZBE}	Byte enable to low Z	0	–	ns
t_{HZBE}	Byte disable to high Z	–	7	ns

Notes
5. AC characteristics (except high Z) are tested using the Thevenin load shown in Figure 3 (a). High Z characteristics are tested for all speeds using the test load shown inFigure 3 (c).
6. Test conditions assume signal transition time of 2.6 ns or less, timing reference levels of 1.3 V, input pulse levels of 0 to 2.6 V.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of Figure 3. Transition is measured ±500 mV from steady-state voltage.
9. This parameter is guaranteed by design and is not tested.

Switching Characteristics *(continued)*

Over the Operating Range

Parameter [6]	Description	-15		Unit
		Min	Max	
Write Cycle[10]				
t_{WC}	Write cycle time	15	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	10	–	ns
t_{AW}	Address set-up to write end	10	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	10	–	ns
t_{SD}	Data set-up to write end	8	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z[11]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z[11, 12]	–	7	ns
t_{BW}	Byte enable to end of write	9	–	ns

Notes

10. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW and $\overline{BHE}$/$\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$ and $\overline{BHE}$/$\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of Figure 3 on page 6. Transition is measured ±500 mV from steady-state voltage.

Switching Waveforms

Figure 4. Read Cycle No. 1 [13, 14]

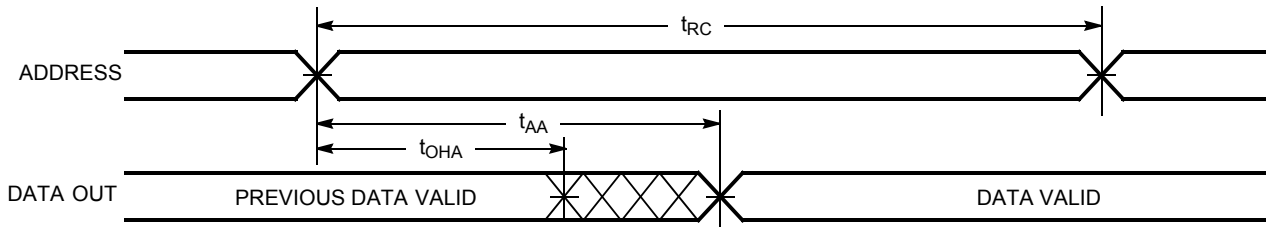
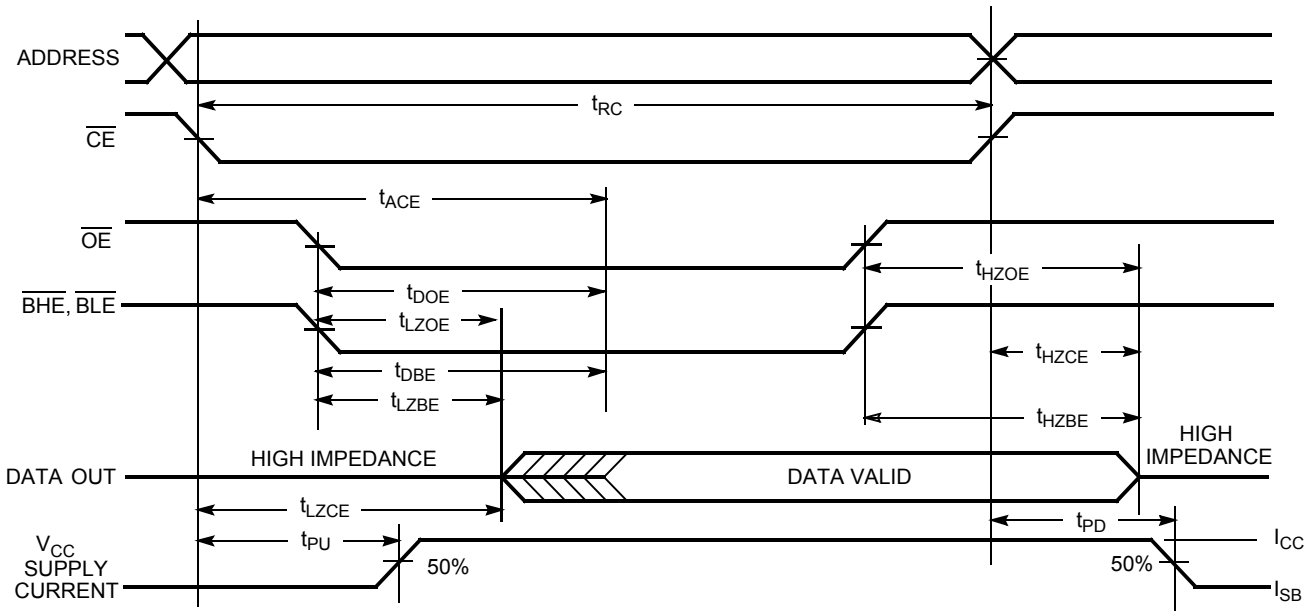


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [14, 15]



Notes
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
14. $\overline{WE}$ is HIGH for Read cycle.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms *(continued)*

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled) [16, 17]

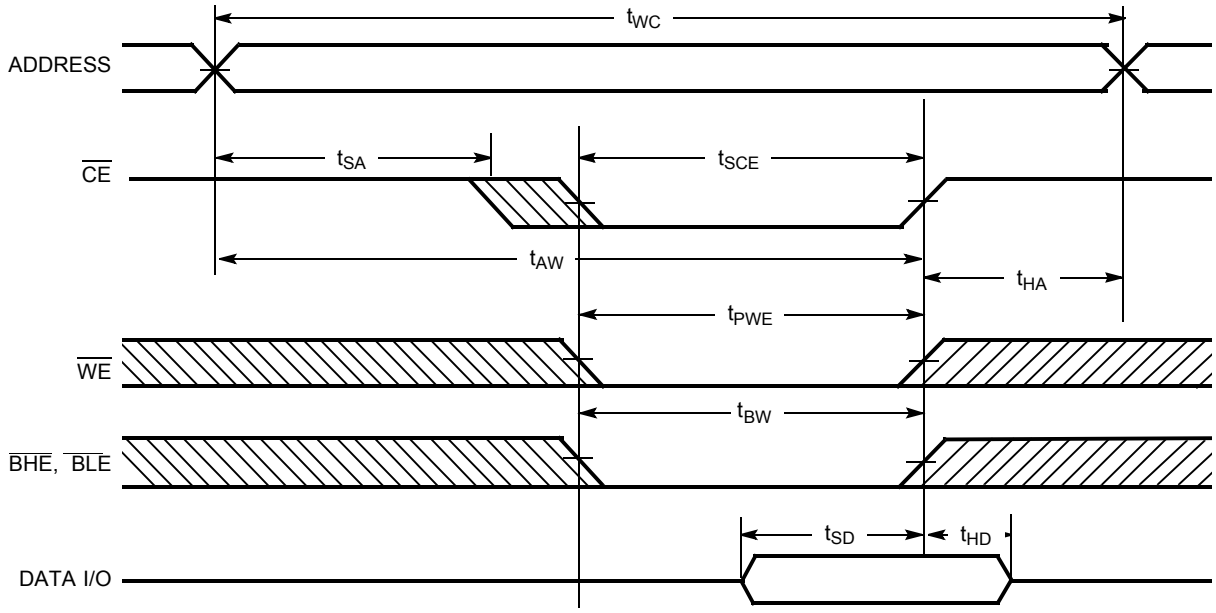
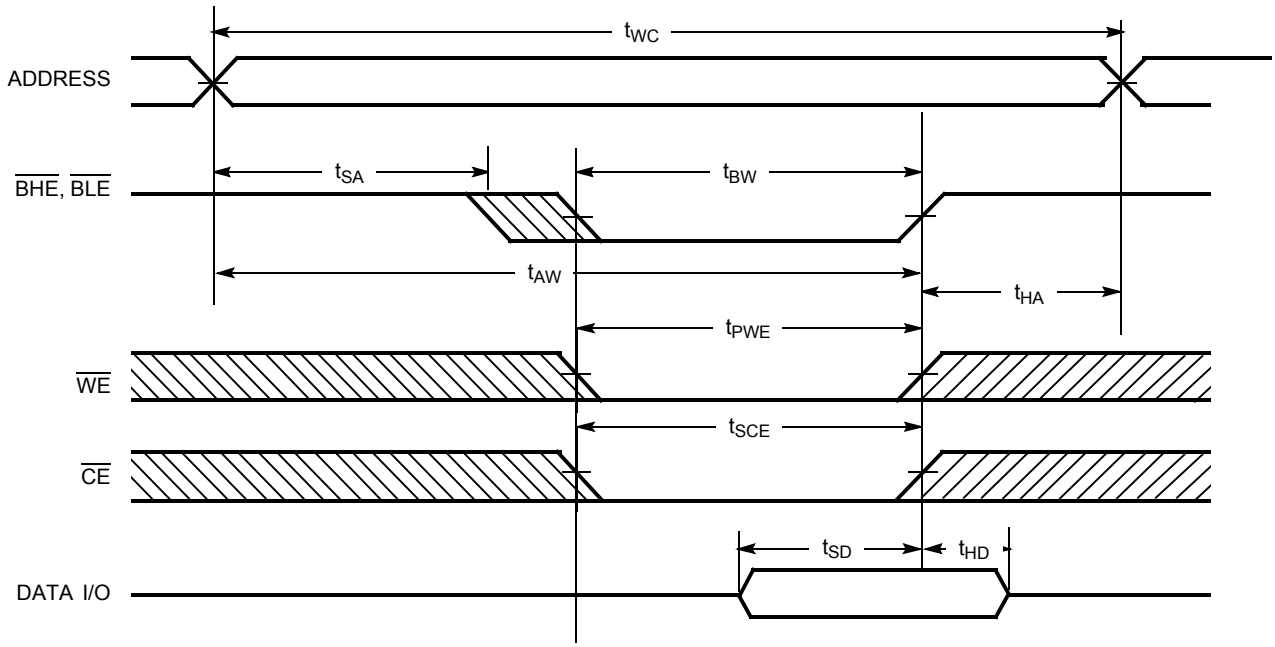


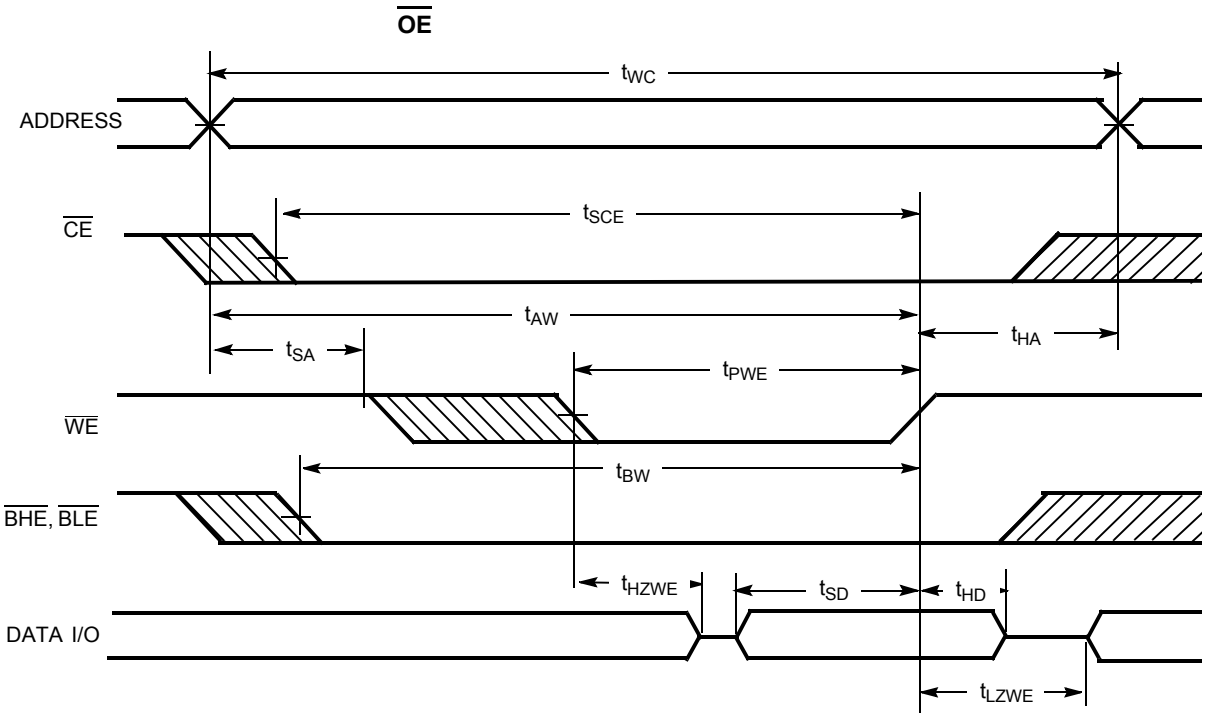
Figure 7. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
16. Data I/O is high-impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms *(continued)*

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at http://www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

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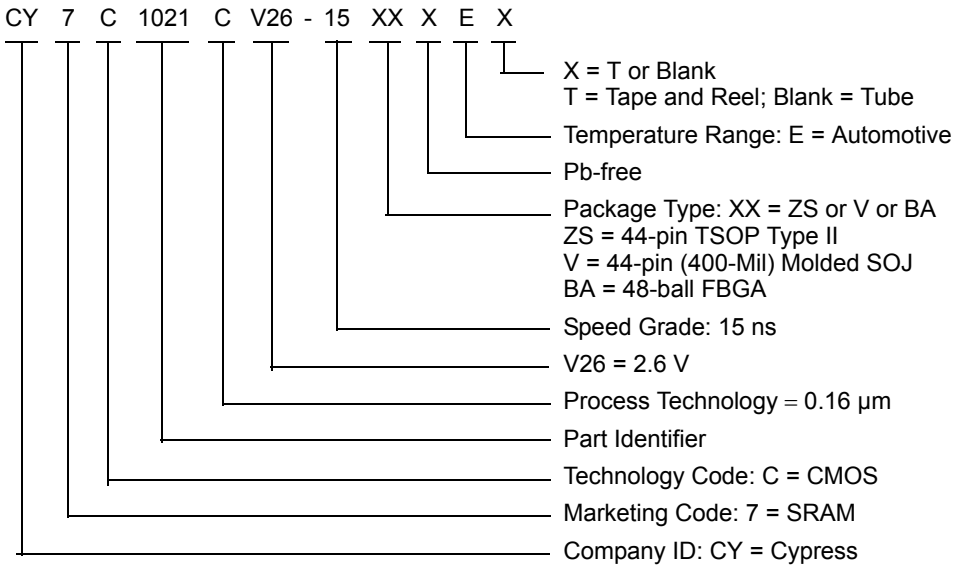
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1021CV26-15ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	Automotive
	CY7C1021CV26-15VXE	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	
	CY7C1021CV26-15BAE	51-85150	48-ball FBGA (6 × 8 × 1 mm) (Pb-free)	
	CY7C1021CV26-15BAET	51-85150	48-ball FBGA (6 × 8 × 1 mm) (Pb-free)	
	CY7C1021CV26-15VXET	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	
	CY7C1021CV26-15ZSXET	51-85087	44-pin TSOP Type II (Pb-free)	

Ordering Code Definitions



Package Diagrams

Figure 9. 44-pin TSOP Z44-II, 51-85087

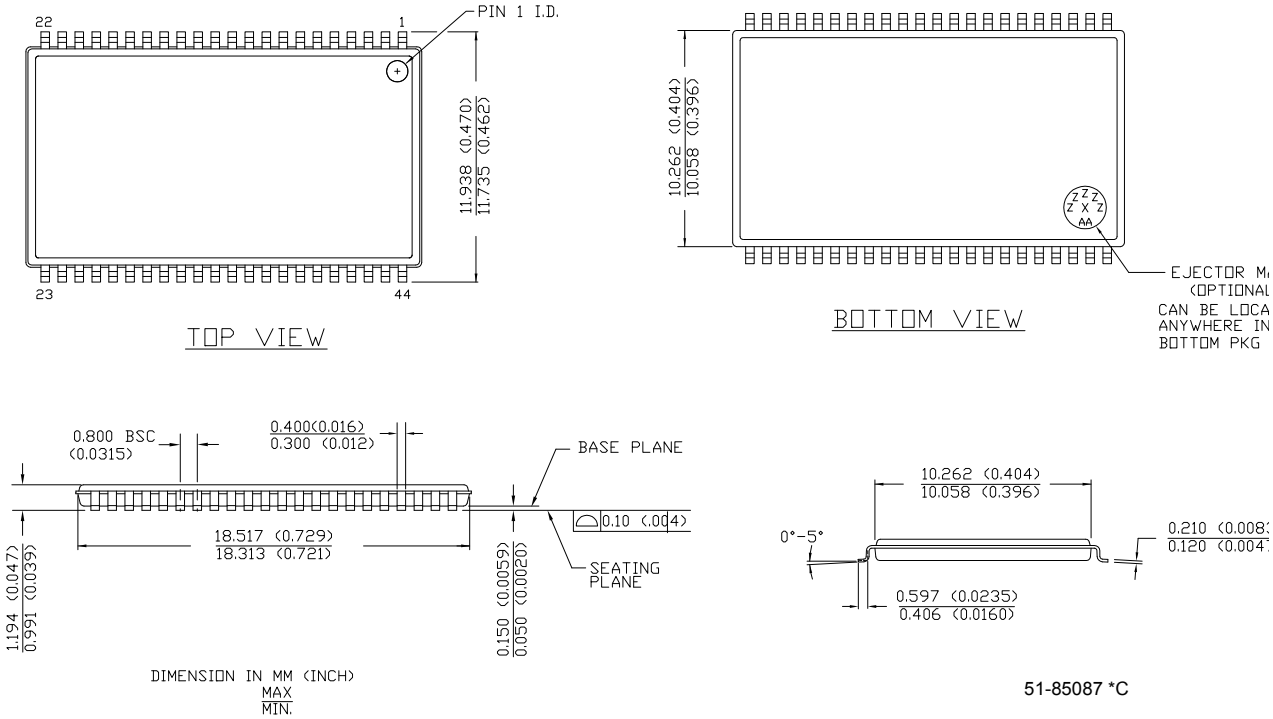
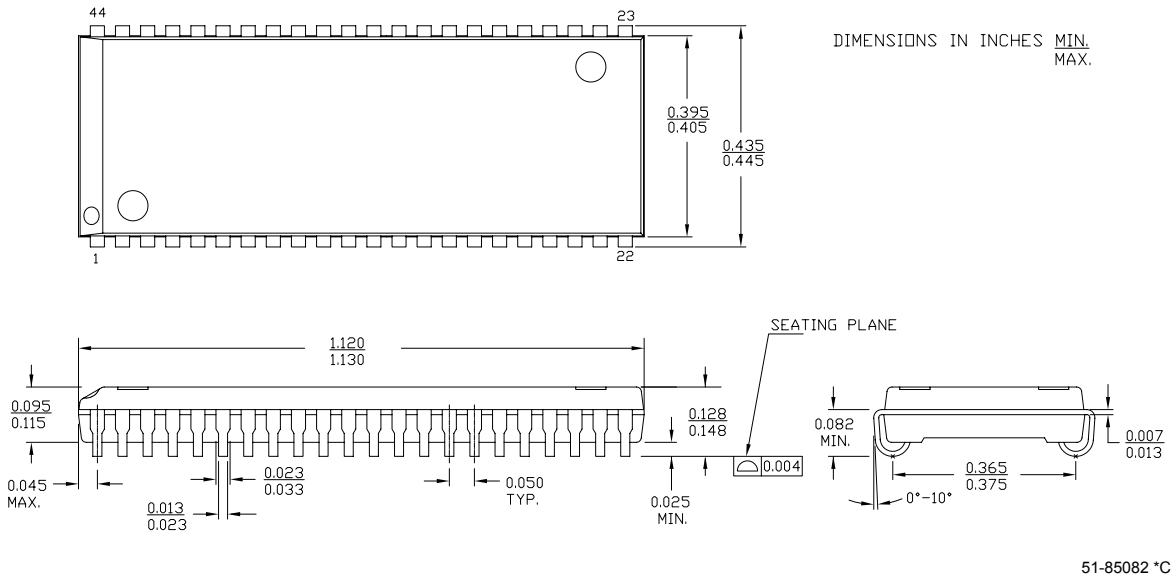
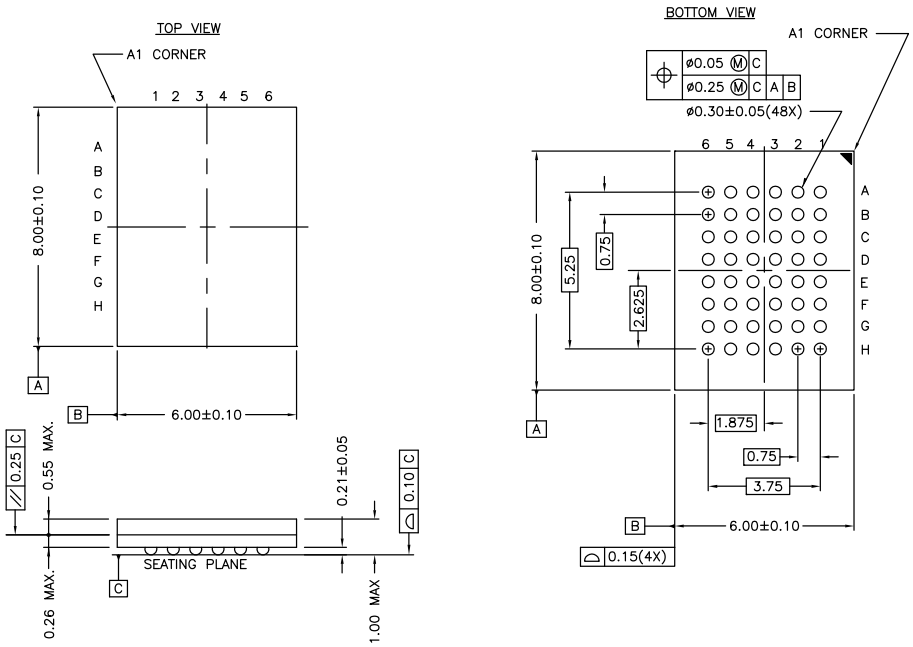


Figure 10. 44-pin Molded SOJ (400-Mil) V44.4, 51-85082



Package Diagrams *(continued)*

Figure 11. 48-ball FBGA (6 × 8 × 1 mm), 51-85150



51-85150 *F

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
$\overline{CE}$	chip enable
I/O	input/output
$\overline{OE}$	output enable
SOJ	small outline J-lead
SRAM	static random access memory
TSOP	thin small-outline package
TTL	transistor-transistor logic
FBGA	fine-pitch ball grid array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	micro Amperes
mA	milli Amperes
mm	milli meter
mW	milli Watts
MHz	Mega Hertz
ns	nano seconds
pF	pico Farad
V	Volts
W	Watts
%	percent

Document History Page

Document Title: CY7C1021CV26, 1-Mbit (64 K × 16) Static RAM Document Number: 38-05589				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	238454	See ECN	RKF	New data sheet for Automotive
*A	335861	See ECN	SYT	Added Lead-Free Product Information Included the 44-Lead (400-Mil) Molded SOJ V34 Package
*B	493543	See ECN	NXR	Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated Ordering Information Table
*C	2897087	03/22/10	AJU	Removed obsolete parts from ordering information table Updated package diagrams
*D	3057593	10/13/2010	PRAS	Updated Ordering Information and added Ordering Code Definitions. Updated Package Diagrams.
*E	3098812	12/01/2010	PRAS	Added Acronyms and Units of Measure. Minor edits and updated in new template.
*F	3277371	06/08/2011	AJU	Updated Pin Configuration (Included pin configurations for 44-pin SOJ and 48-ball FBGA packages).

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