

# 4-Mbit (256 K × 16) Static RAM

#### Features

- Pin-and function-compatible with CY7C1041B
- High speed □ t<sub>AA</sub> = 10 ns
- Low active power □ I<sub>CC</sub> = 90 mA at 10 ns (Industrial)
- Low CMOS standby power □ I<sub>SB2</sub> = 10 mA
- 2.0 V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE features
- Available in Pb-free 44-Pin (400-Mil) Molded SOJ and 44-Pin TSOP II packages

#### Functional Description<sup>[1]</sup>

The CY7C1041D is a high-performance CMOS static RAM organized as 256K words by 16 bits. Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>17</sub>).

<u>Reading</u> from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable (BHE) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1041D is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

## Logic Block Diagram



#### **Selection Guide**

	–10 (Industrial)	–12 (Automotive) <sup>[2]</sup>	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	90	95	mA
Maximum CMOS Standby Current	10	15	mA

Note

1. For guidelines on SRAM system design, please refer to the "System Design Guidelines" Cypress application note, available on the internet at www.cypress.com.

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#### **Pin Configuration**

#### Figure 1. SOJ / TSOP II – Top View

A₀ ⊏	1	<sup>44</sup> ☐ A <sub>17</sub>
A <sub>1</sub> 🗆	2	43 🛛 A <sub>16</sub>
A <sub>2</sub> L	3	42 🛛 A <sub>15</sub>
A <sub>3</sub> ⊑	4	41 🛛 OE
A <sub>4</sub> L	5	40 🛛 BHE
CĒĽ	6	39 🛛 BLE
I/O₀ □	7	<sup>38</sup> I/O <sub>15</sub>
I/O <sub>1</sub> [	8	37 🛛 I/O <sub>14</sub>
I/O <sub>2</sub> □	9	<sup>36</sup> I/O <sub>13</sub>
I/O <sub>3</sub> 🗆	10	35 🛛 I/O12
V <sub>CC</sub> □	11	<sup>34</sup> 🖵 V <sub>SS</sub>
V <sub>SS</sub> [	12	<sup>33</sup> 🗆 V <sub>CC</sub>
I/O4 □	13	32 📙 I/O <sub>11</sub>
I/O <sub>5</sub> [	14	31 🛛 I/O <sub>10</sub>
I/O <sub>6</sub> [	15	30 🛛 I/O <sub>9</sub>
1 <u>/07</u> L	16	29 I/O <sub>8</sub>
WEL	17	28 🛛 NC
A <sub>5</sub> [	18	27 🛛 A <sub>14</sub>
	19	$^{26}$ $A_{13}$
	20 21	$25 \square A_{12}$
A <sub>8</sub> ⊑ A <sub>9</sub> ⊑	21	24 🛛 A <sub>11</sub> 23 🗖 A <sub>10</sub>
, vg 🗆	22	23 A <sub>10</sub>

#### **Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature65°C to +150°C
Ambient Temperature with Power Applied55°C to +125°C
Supply Voltage on $V_{CC}$ to Relative $GND^{[3]}{-}0.5$ V to +6.0 V
DC Voltage Applied to Outputs in High Z State $^{[3]}$ 0.5 V to V_{CC} +0.5 V
DC Input Voltage <sup>[3]</sup> 0.5 V to $V_{CC}$ +0.5 V
Current into Outputs (LOW) 20 mA

Static Discharge Voltage	.>2001 V
(per MIL-STD-883, Method 3015)	
Latch-up Current	>200 mA

## **Operating Range**

Range	Ambient Temperature	V <sub>cc</sub>	Speed	
Industrial	–40°C to +85°C	$5~V\pm0.5$	10 ns	
Automotive	–40°C to +125°C	$5~V\pm0.5$	12 ns	



## Electrical Characteristics Over the Operating Range

Deremeter	Description	Test Conditio		-10 (In	dustrial)	-12 (Aut	omotive)	
Parameter	Description	Test Conditions		Min	Max	Min	Max	Unit
V <sub>OH</sub>	Output HIGH Voltage	$V_{CC}$ = Min, $I_{OH}$ = -4.0 $V_{CC}$ = Min, $I_{OL}$ = 8.0 m		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage				0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.0	V <sub>CC</sub> + 0.5	2.0	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage <sup>[3]</sup>			-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled		-1	+1	-1	+1	μΑ
I <sub>CC</sub>		V <sub>CC</sub> = Max,	100 MHz		90		-	mA
	Current	$f = f_{MAX} = 1/t_{RC}$	83 MHz		80		95	mA
			66 MHz		70		85	mA
			40 MHz		60		75	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	$\begin{array}{l} \text{Max } V_{\text{CC}}, \ \overline{\text{CE}} \geq V_{\text{IH}} \ V_{\text{IN}} \geq V_{\text{IH}} \ \text{or} \\ V_{\text{IN}} \leq V_{\text{IL}}, \ f = f_{\text{MAX}} \end{array}$			20		25	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	$\begin{array}{l} \text{Max } V_{\text{CC}}, \ \overline{\text{CE}} \geq V_{\text{CC}} - \\ V_{\text{IN}} \geq V_{\text{CC}} - 0.3 \text{ V, or V} \\ \text{f} = 0 \end{array}$			10		15	mA

#### Capacitance<sup>[4]</sup>

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	$T_A = 25^{\circ}C$ , $f = 1$ MHz,	8	pF
C <sub>OUT</sub>	I/O Capacitance	$V_{CC} = 5.0 V$	8	pF

#### Thermal Resistance<sup>[4]</sup>

Parameter	Description	Test Conditions	SOJ Package	TSOP II Package	Unit
$\Theta_{JA}$	Thermal resistance (Junction to Ambient) <sup>[4]</sup>	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	57.91	50.66	°C/W
Θ <sub>JC</sub>	Thermal resistance (Junction to Case) <sup>[4]</sup>		36.73	17.17	°C/W

- Notes

Automotive product information is Preliminary.
 V<sub>IL</sub> (Min) = -2.0 V and V<sub>IH</sub> (max) = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.
 Tested initially and after any design or process changes that may affect these parameters.



#### AC Test Loads and Waveforms<sup>[5]</sup>





Equivalent to:	THÉVENIN	EQUIVA	LENT
OUTPUT	0		1.73 V

#### Switching Characteristics<sup>[6]</sup> Over the Operating Range

		–10 (In	–10 (Industrial)		-12 (Automotive)	
Parameter	Description	Min	Max	Min	Max	Unit
Read Cycle	·					
t <sub>power</sub>	V <sub>CC</sub> (typical) to the First Access <sup>[7]</sup>	100		100		μS
t <sub>RC</sub>	Read Cycle Time	10		12		ns
t <sub>AA</sub>	Address to Data Valid		10		12	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		ns
t <sub>ACE</sub>	CE LOW to Data Valid		10		12	ns
t <sub>DOE</sub>	OE LOW to Data Valid		5		6	ns
t <sub>LZOE</sub>	OE LOW to Low Z	0		0		ns
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[8, 9]</sup>		5		6	ns
t <sub>LZCE</sub>	CE LOW to Low Z <sup>[9]</sup>	3		3		ns
t <sub>HZCE</sub>	CE HIGH to High Z <sup>[8, 9]</sup>		5		6	ns
t <sub>PU</sub>	CE LOW to Power-Up	0		0		ns
t <sub>PD</sub>	CE HIGH to Power-Down		10		12	ns
t <sub>DBE</sub>	Byte Enable to Data Valid		5		6	ns
t <sub>LZBE</sub>	Byte Enable to Low Z	0		0		ns
t <sub>HZBE</sub>	Byte Disable to High Z		5		6	ns

Notes

- AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load 5. shown in Figure (c)
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance. 6.
- t<sub>POWER</sub> gives the minimum amount of time that the power supply should be at typical V<sub>CC</sub> values until the first memory access can be performed.
   t<sub>POWER</sub> gives the minimum amount of time that the power supply should be at typical V<sub>CC</sub> values until the first memory access can be performed.
   t<sub>PACE</sub>, t<sub>PACE</sub>, t<sub>PACE</sub>, and t<sub>PACE</sub> are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.



#### Switching Characteristics<sup>[6]</sup> Over the Operating Range(continued)

		–10 (Inc	dustrial)	-12 (Aut	omotive)	
Parameter	Description	Min	Max	Min	Max	Unit
Write Cycle <sup>[10, 11</sup>	]			•	•	
t <sub>WC</sub>	Write Cycle Time	10		12		ns
t <sub>SCE</sub>	CE LOW to Write End	7		10		ns
t <sub>AW</sub>	Address Set-Up to Write End	7		10		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	WE Pulse Width	7		10		ns
t <sub>SD</sub>	Data Set-Up to Write End	6		7		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>LZWE</sub>	WE HIGH to Low Z <sup>[9]</sup>	3		3		ns
t <sub>HZWE</sub>	WE LOW to High Z <sup>[8, 9]</sup>		5		6	ns
t <sub>BW</sub>	Byte Enable to End of Write	7		10		ns

#### Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions <sup>[13]</sup>		Min	Max	Unit
V <sub>DR</sub>	$V_{CC}$ for Data Retention			2.0		V
I <sub>CCDR</sub>	Data Retention Current	$\frac{V_{CC}}{CE} = V_{DR} = 2.0 \text{ V},$ $CE \ge V_{CC} - 0.3 \text{ V},$	Ind'l		10	mA
I <sub>CCDR</sub>	Data Retention Current	$CE \ge V_{CC} - 0.3 V,$ $V_{IN} \ge V_{CC} - 0.3 V \text{ or } V_{IN} \le 0.3 V$	Auto		15	mA
t <sub>CDR</sub> <sup>[4]</sup>	Chip Deselect to Data Retention Time			0		ns
t <sub>R</sub> <sup>[12]</sup>	Operation Recovery Time			t <sub>RC</sub>		ns

#### **Data Retention Waveform**



#### Notes

Notes 10. The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write. 11. The minimum Write cycle time for Write Cycle No. 3 (WE controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ . 12. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(Min)</sub>  $\ge$  50 µs or stable at V<sub>CC(Min)</sub>  $\ge$  50 µs

<sup>13.</sup> No input may exceed  $V_{CC}$  + 0.5 <u>V</u> 14. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$ , and/or  $\overline{BHE}$  = V<sub>IL</sub>.



## **Switching Waveforms**



Figure 3. Read Cycle No. 2 (OE Controlled) <sup>[15,16]</sup>





#### Switching Waveforms (continued)



Figure 4. Write Cycle No. 1 (CE Controlled)<sup>[17, 18]</sup>



 Notes

 15. WE is HIGH for read cycle.

 16. Address valid prior to or coincident with CE transition LOW

 17. Data I/O is high impedance if OE or BHE and/or BLE= VIH.

 18. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.



## Switching Waveforms (continued)



Figure 6. Write Cycle No. 3 (WE Controlled, OE HIGH During Write)<sup>[16, 17]</sup>



Note 19. During this period the I/Os are in the output state and input signals should not be applied.





#### Truth Table

CE	OE	WE	BLE	BHE	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	Mode	Power
Н	Х	Х	Х	Х	High Z	High Z	Power Down	Standby (I <sub>SB</sub> )
L	L	Н	L	L	Data Out	Data Out	Read All bits	Active (I <sub>CC</sub> )
L	L	Н	L	Н	Data Out	High Z	Read Lower bits only	Active (I <sub>CC</sub> )
L	L	Н	Н	L	High Z	Data Out	Read Upper bits only	Active (I <sub>CC</sub> )
L	Х	L	L	L	Data In	Data In	Write All bits	Active (I <sub>CC</sub> )
L	Х	L	L	Н	Data In	High Z	Write Lower bits only	Active (I <sub>CC</sub> )
L	Х	L	Н	L	High Z	Data In	Write Upper bits only	Active (I <sub>CC</sub> )
L	Н	Н	Х	Х	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

#### **Ordering Information**

Table 1 lists the CY7C1041D key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 1. Key Features and Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1041D-10VXI	51-85082	44-Pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1041D-10ZSXI	51-85087	44-Pin TSOP Type II (Pb-free)	

#### **Ordering Code Definitions**





#### **Package Diagrams**





## Acronyms

Acronym	Description		
CE	chip enable		
CMOS	Complementary metal oxide semiconductor		
I/O	Input/output		
OE	output enable		
SRAM	Static random access memory		
SOJ	Small Outline J-Lead		
TSOP	Thin Small Outline Package		
VFBGA	Very Fine-Pitch Ball Grid Array		

### **Document Conventions**

#### **Units of Measure**

Symbol	Unit of Measure	
ns	nano seconds	
V	Volts	
μA	micro Amperes	
mA	milli Amperes	
mV	milli Volts	
mW	milli Watts	
MHz	Mega Hertz	
pF	pico Farad	
°C	degree Celcius	
W	Watts	



## **Document History Page**

	Document Title: CY7C1041D 4-Mbit (256K x 16) Static RAM Document Number: 38-05472					
Revision	ECN	Orig. of Change	Submission Date	Description of Change		
**	201560	SWI	See ECN	Advance Datasheet for C9 IPP		
*A	233729	RKF	See ECN	1.AC, DC parameters are modified as per EROS (Spec #01-2165) 2.Pb-free offering in the 'ordering information'		
*В	351117	PCI	See ECN	Changed from Advance to Preliminary Removed 17 and 20 ns Speed bin Added footnote # 4 Redefined I <sub>CC</sub> values for Com'l and Ind'l temperature ranges I <sub>CC</sub> (Com'l): Changed from 67 and 54 mA to 75 and 70 mA for 12 and 15 ns speed bins respectively I <sub>CC</sub> (Ind'l): Changed from 80, 67 and 54 mA to 90, 85 and 80 mA for 10, 12 and 15 ns speed bins respectively Changed footnote # 10 on t <sub>R</sub> Changed t <sub>SCE</sub> from 8 to 7 ns for 10 ns speed bin Added Static Discharge Voltage and latch-up current spec Added V <sub>IH(max</sub> ) spec in footnote # 2 Changed reference voltage level for measurement of Hi-Z parameters from $\pm$ 500 mV to $\pm$ 200 mV Added Write Cycle (WE Controlled, $\overline{OE}$ HIGH During Write) Timing Diagram Changed part names from Z to ZS in the Ordering Information Table Removed L-Version Added 10 ns parts in the Ordering Information Table Added Lead-Free Ordering Information Shaded Ordering Information Table		
*C	446328	NXR	See ECN	Converted Preliminary to Final Removed -15 speed bin Removed Commercial Operating Range product information Added Automotive Operating Range product information Changed Maximum Rating for supply voltage from 7 V to 6 V Updated Thermal Resistance table Changed t <sub>HZWE</sub> from 6 ns to 5 ns Updated footnote #8 on High-Z parameter measurement Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table		
*D	2897049	VKN	03/22/10	Removed inactive parts from the ordering information table.		
*E	3109184	AJU	12/13/2010	Added Ordering Code Definitions.		
*F	3236731	PRAS	04/21/2011	Template updates. Added acronyms and units tables.		



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