CY8CMBR2016

CapSense® Express™ 16 Button Matrix Controller

Features

- Hardware Configurable Matrix CapSense® Controller
  - Does not require software tools or programming
  - 16 buttons can be configured individually or as a matrix
  - Supports 3x4 and 4x4 matrix configurations
- Matrix Host Interface Communication
  - Industry standard host interface protocols reuse existing host processor firmware
    - Key Scan Interface
    - Truth Table Interface
  - Encoded GPO Interface - minimizes number of pins required
- SmartSense™ Auto-Tuning
  - Maintains optimal button performance even in noisy environments
  - CapSense parameters dynamically set in runtime
  - Wide parasitic capacitance (C_P) range (5–40 pF)
  - Saves time and effort in device tuning
- Noise Immunity
  - High sensitivity, low noise capacitive sensing algorithm
  - Strong immunity to RF and AC noise
  - Low radiated noise emission
- System Diagnostics of CapSense Buttons
  - Reports any faults at device power up
  - Button shorts
  - Improper value of modulating capacitor (C_{MOD})
  - Parasitic capacitance (C_P) out of range
- Advanced Features
  - Flanking Sensor Suppression (FSS) provides robust sensing even with closely spaced buttons
  - Buzzer Signal Output
  - Configurable sensitivity for all buttons
  - Interrupt line to host to indicate any CapSense button status change
  - Serial Debug Data out
    - Simplifies production line testing and system debug
- Wide operating range
  - 1.71–5.5 V
  - Ideal for both regulated and unregulated battery applications [1]
- Low power consumption
  - Supply current in run mode as low as 20 µA[2] per button
  - Deep sleep current: 100 nA
- Industrial temperature range: –40 °C to + 85 °C
- 48-pin QFN package (6 × 6 × 0.6 mm)

Overview

The CY8CMBR2016 CapSense Express capacitive touch sensing controller incorporates several innovative features to save time and money to quickly enable a capacitive touch sensing user interface in your design. It is a hardware configurable device and does not require any software tools, firmware coding or device programming. This device is enabled with Cypress's revolutionary SmartSense™ auto-tuning algorithm. SmartSense™ auto-tuning ends the need to manually tune the user interface during development and production ramp. This speeds the time to volume and saves valuable engineering time, test time and production yield loss.

The device supports up to 16 capacitive touch buttons that can be organized in any format, such as a matrix array. With its backward compatible key scan interface, it can enable users to achieve quick-to-market (retrofit) designs in large keypad applications such as fire alarm control panels, security systems, and door locks. Any application that requires up to 16 CapSense buttons can utilize CY8CMBR2016.

The wide operating range of 1.71 V to 5.5 V enables unregulated battery operation, further saving component cost. This device supports ultra low-power consumption in both run mode and deep sleep mode to stretch battery life. In addition, this device also supports many advanced features, which enhance the robustness and user interface of the end solution. Some of the key advanced features include Noise Immunity and FSS. Noise Immunity improves the immunity of the device against radiated and conducted noise, such as audio and radio frequency (RF) noise. FSS provides robust sensing even with closely spaced buttons. FSS is a critical requirement in small form factor applications.

The CY8CMBR2016 provides three different host interface communication modes. These include the industry standard host interface protocols such as Key Scan Interface and Truth Table Interface. These two protocols reuse existing host processor firmware leading to easy conversion of existing mechanical buttons to CapSense. The third host interface communication is the Encoded GPO Interface with a 4-bit output, which minimizes the number of pins required for a button output. These three outputs are configurable which helps provide a wide variety of device usage in multiple applications.

Serial Debug Data output gives the critical information about the design, such as button Cp and raw counts. This further helps in production line testing.

Notes
1. Supply variation should not be more than 5% for proper CapSense operation
2. Power consumption calculated with 250 ms scan time, 2% touch time and C_P of each button < 19 pF.

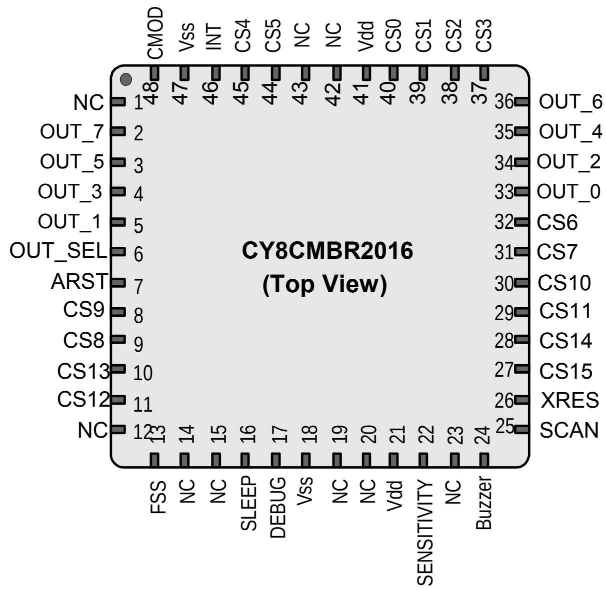
Contents

Pinout

Table 1. Pinout for the Device

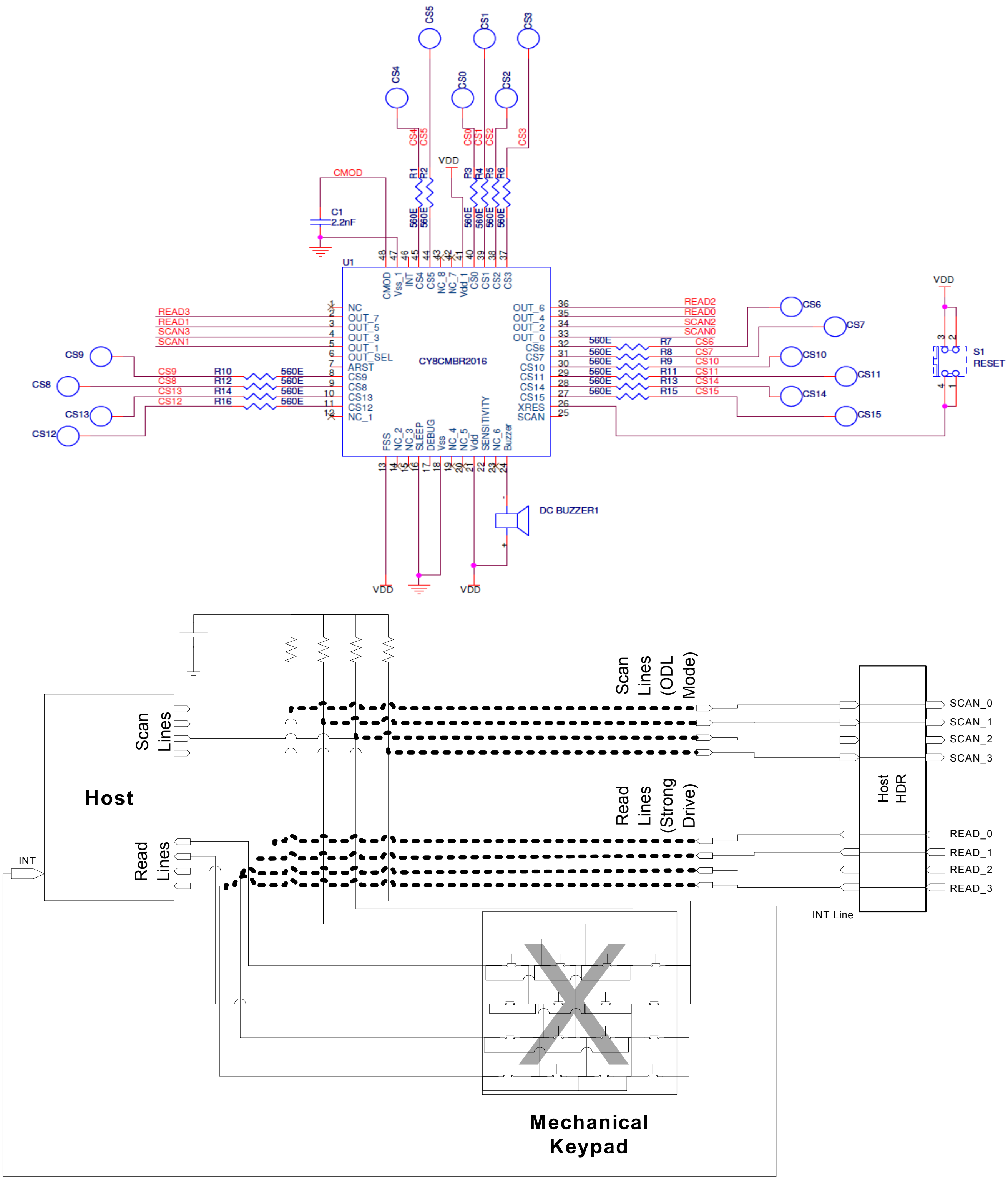
Pin	Pin Name	Type	Description
1	NC	–	No connection
2	OUT_7	DO	READ_3/TT_ROW_3/EO_3/ FMEA_CLK line - Output port interface pin 7
3	OUT_5	DO	READ_1/TT_ROW_1/EO_1 - Output port interface pin 5
4	OUT_3	DIO	SCAN_3/TT_COL_3 - Output port interface pin 3
5	OUT_1	DIO	SCAN_1/TT_COL_1 - Output port interface pin 1
6	OUT_SEL	AI	Selects the output interface
7	ARST	AI	Controls button auto reset period
8	CS9	AI	CapSense button 9
9	CS8	AI	CapSense button 8
10	CS13	AI	CapSense button 13
11	CS12	AI	CapSense button 12
12	NC	–	Reserved pin
13	FSS	DI	Controls FSS feature
14	NC	–	No connection
15	NC	–	No connection
16	SLEEP	DI	Controls entry/exit to Deep Sleep
17	DEBUG	DO	Serial Debug Data out from the device (UART TX8 line)
18	V_{SS}	–	GND
19	NC	–	No connection
20	NC	–	No connection
21	V_{DD}	–	Power supply
22	SENSITIVITY	AI	Selects the sensitivity of the CS system
23	NC	–	Reserved for shield out
24	BUZZER	DO	Connects to DC Buzzer for audio feedback
25	SCAN	AI	Controls the sleep rate of the system
26	XRES	DI	System reset pin
27	CS15	AI	CapSense button 15
28	CS14	AI	CapSense button 14
29	CS11	AI	CapSense button 11
30	CS10	AI	CapSense button 10
31	CS7	AI	CapSense button 7
32	CS6	AI	CapSense button 6
33	OUT_0	DIO	SCAN_0/TT_COL_0 - Output port interface pin 0
34	OUT_2	DIO	SCAN_2/TT_COL_2 - Output port interface pin 2
35	OUT_4	DO	READ_0/TT_ROW_0/EO_0 - Output port interface pin 4
36	OUT_6	DO	READ_0/TT_ROW_0/EO_2/FMEA_DATA - Output port interface pin 6
37	CS3	AI	CapSense button 3
38	CS2	AI	CapSense button 2
39	CS1	AI	CapSense button 1
40	CS0	AI	CapSense button 0
41	Vdd	–	Power supply
42	NC	–	No connection
43	NC	–	No connection
44	CS5	AI	CapSense button 5
45	CS4	AI	CapSense button 4
46	INT	DO	Interrupt line to Host
47	Vss	–	GND
48	C_{MOD}	AI	Modulator capacitor, 2.2 nF

Figure 1. Device Pinout



Typical Circuits

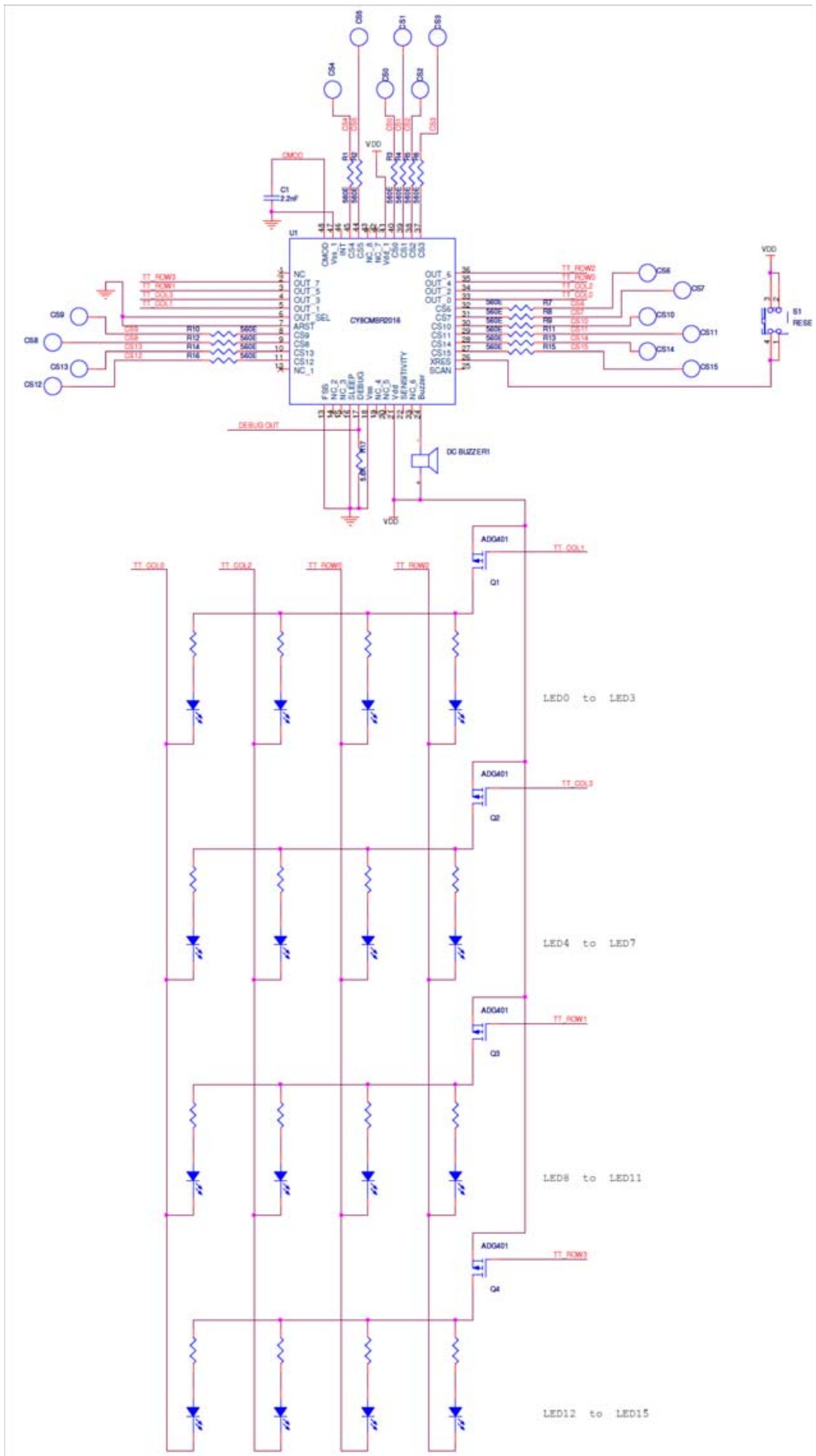
Figure 2. Schematic 1: 16 Buttons with Key Scan Output Mode



In Schematic 1, CY8CMBR2016 is configured as follows:

- 16 CapSense buttons
- Key Scan Interface
- Continuous scan mode
- High sensitivity for all buttons
- FSS enabled
- Button Auto Reset disabled
- Serial Debug Data Out disabled
- DC buzzer output
- Reset button
- Interrupt line output

Figure 3. Schematic 2: 16 Buttons with Truth Table Output Mode



In Schematic 2, CY8CMBR2016 is configured as follows:

- 16 CapSense buttons
- Truth Table Output configured to drive LEDs
- Continuous Scan mode
- High sensitivity for all buttons
- FSS disabled
- Button Auto Reset enable, with a period of 5 seconds
- Serial Debug Data Out enabled
- DC buzzer output
- Reset button
- Interrupt line output

Configuring the CY8CMBR2016

The CY8CMBR2016 device features are configured using external resistors. The resistors on the hardware configurable pins are determined by the device upon power-on. The Appendix on page 26 gives the matrix of features enabled using different external resistor configurations.

Device Features

Table 2. Device Feature List

Feature	Description/Use
16 CapSense Buttons	Mechanical button/keypad replacement
Flanking Sensor Suppression (FSS)	Helps in distinguishing closely spaced buttons
Key Scan Interface	Mechanical matrix replacement
Truth Table Output	Easy to decode truth table based output mode
4-bit Encoded Output	Fewer pins needed to output button status
Button Auto Reset	Prevents buttons from getting stuck during run time
Scan/Sleep Rate	Configures the device based on power needs
Configurable Sensi-tivity	Selects the sensitivity for the system – minimum change in capacitance to be detected
Deep Sleep	Reduce power consumption by hibernating the device
System Diagnostics	Supports for production testing and debugging

CapSense Buttons

- Device supports up to 16 CapSense Buttons.
- Ground the CSx Pin to disable CapSense input.
- 2.2 nF (± 10%) capacitor should be connected on C_{MOD} pin for proper CapSense operation.
- The parasitic capacitance (C_P) of each button must be less than 40 pF for proper CapSense operation.

SmartSense Auto-Tuning

- Device supports auto-tuning of CapSense button parameters.
- No manual tuning required; all parameters are automatically tuned by the device.
- Compensates printed circuit board (PCB) variations, device process variations, and PCB vendor changes.
- Ensures portability of the user interface design.

Flanking Sensor Suppression (FSS)

- Helps to distinguish closely spaced buttons.
- Also used in situations when a button can produce opposite effects. For example, an interface with two buttons for brightness control (UP or DOWN).
- FSS action can be explained for the following different scenarios:
  - When only one button is touched, it is reported as ON.
  - When more than one button is detected as ON and previously one of those buttons was touched, then the previously touched button is reported as ON. (Refer to Figure 4.)

Key Scan Interface

- Mimics legacy mechanical keypads - Four SCAN lines (I/P) and four READ lines (O/P)
- Reads the SCAN lines and updates the READ lines based on the button status (Refer to Figure 5).
- ‘Plug' n 'Play' replacement for mechanical keypads.
- When buttons are disabled or found to be invalid, Table 3 helps identifying the scan and read lines.
- When the SCAN lines are not used, they should be connected to V_{DD}
- OUT0 to OUT3 in the pin out form the SCAN lines and OUT4 to OUT7 form the READ lines
- Refer Figure 6 for SCAN line waveform details.

Table 3. Key Scan interface Selection based on # of Buttons

No. of Buttons	SCAN × READ Lines	Scan Lines
(>12)	4 × 4	OUT0 to OUT3
(<=12) && (>8)	3 × 4	OUT0 to OUT2
(<=8) && (>4)	2 × 4	OUT0 to OUT1
(<=4)	1 × 4	OUT0

Figure 4. Button Status with Respect to Finger Touch when FSS is Enabled [3]

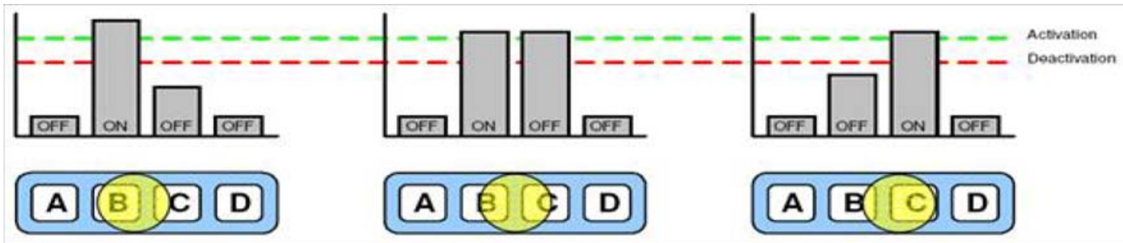


Figure 5. Key Scan interface Retrofit

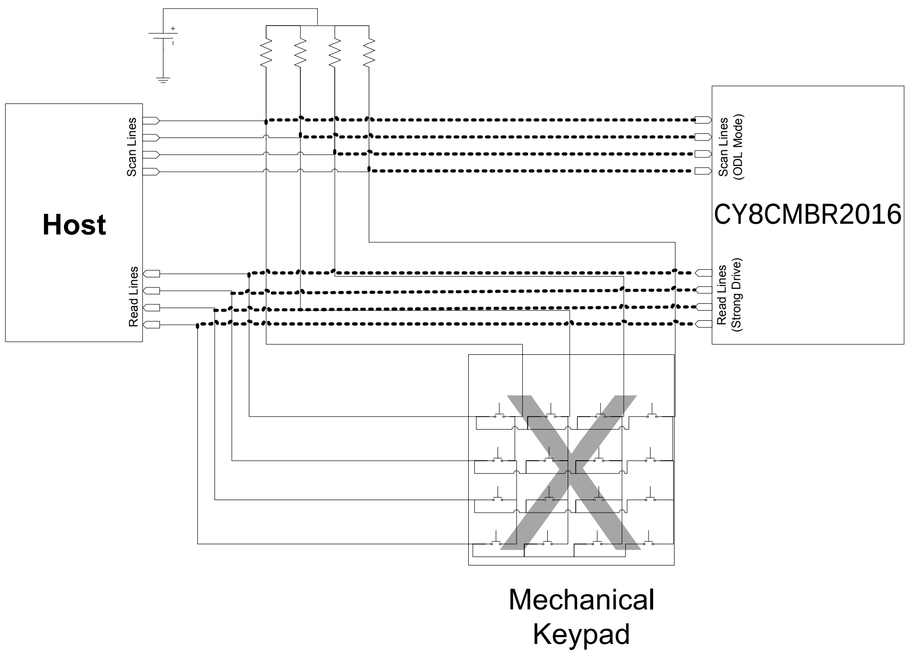
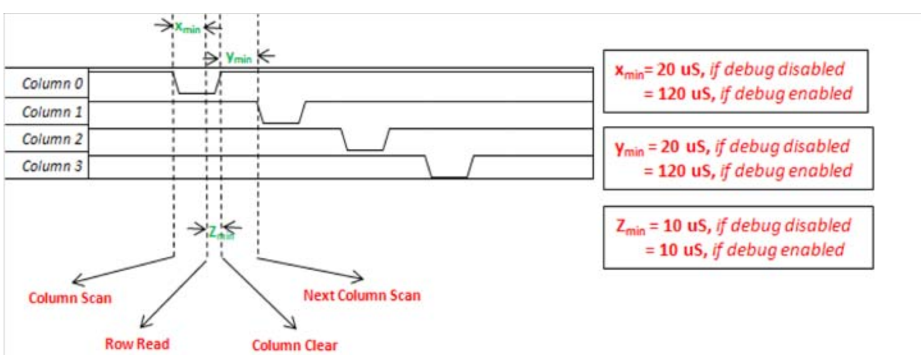


Figure 6. SCAN Line Waveform Details



Note

3. When finger moves from one button to other (FSS enabled).

Truth Table Output

- Another output interface providing matrix outputs.
- All pins are output pins - divided into ROW/COLUMN.
- Only one button can be reported at a time - cannot be used in conjunction with FSS disabled.
- Button status is reported in an encoded ROW/COLUMN fashion as shown in Figure 7.
- Each button has its own ROW-COLUMN code.
- Easy to integrate into a system requiring a simple interface with single key press requirement.
- OUT4 to OUT7 in the pin out form the ROW lines and OUT0 to OUT3 form the COLUMN lines.

Figure 7. Truth Table Output

4x4	Matrix Code							
Buttons	Rows 3	Rows 2	Rows 1	Rows 0	Columns 3	Columns 2	Columns 1	Columns 0
1				●				●
2				●			●	
3				●		●		
4				●	●			
5			●					●
6			●				●	
7			●			●		
8			●		●			
9		●						●
10		●					●	
11		●				●		
12		●			●			
13	●							●
14	●						●	
15	●					●		
16	●				●			

Encoded 4-bit Output

- Only 4 pins to report a button press out of 16 buttons.
- Each button has its own code.
- Only one button can be reported at a time using this interface.
- Table 4 defines the decode table.

Table 4. Encoded Output

Keypress Detected By CapSense	EO[3:0]	Interrupt Time
Key #1	0000	1
Key #2	0001	1
Key #3	0010	1
Key #4	0011	1
…	…	1
Key #16	1111	1
No keys pressed	XXXX	0

Buzzer Signal Output

- A dedicated pin for buzzer output is provided in the device.
- Buzzer output can be used to drive an p-type transistor driving a buzzer or directly a DC buzzer up to 10 mA sink current.

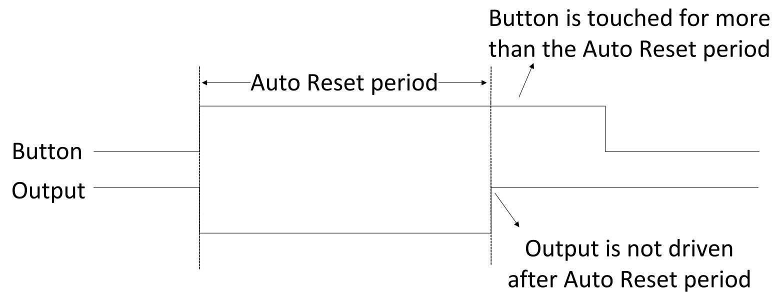
Interrupt Line

- An interrupt line to the host controller.
- On a button touch, the device pulls the INT line HIGH to indicate an interrupt to the host. The INT line remains HIGH as long as a button is touched.
- Can be used as a latch input at the host side to read the OUT lines.
- Can also be used as an interrupt line for the host controller to read the OUT lines.

Button Auto Reset

- Prevents button stuck, due to any conducting object placed close to a button.
- Useful when output to be kept ON only for a specific time.
- The Button Auto Reset period is controlled by the hardware configuration on the ARST pin. Refer Table 18 in Appendix on page 26 for pin configuration details.
- When touched, a button is treated active for a maximum of Button Auto Reset period (refer to Figure 8).
- After the button is released the CSx will be hold for 440 ms.

Figure 8. Button Auto Reset



Output Select

- One among the three output interfaces defined earlier in the section can be selected by the hardware configuration on the OUT_SEL pin. Refer Table 18 in Appendix on page 26 for pin configuration details.
- Only one of the three output interfaces can be used at a given time.

Scan Rate

- This defines the rate at which the device scans all the buttons and then sleeps, in the Low Power Sleep mode. For more details about Low Power Sleep mode, refer to Power Consumption and Device Operating Modes on page 15.
- The device scan rate is defined by the hardware configuration on the SCAN pin. Refer Table 18 in Appendix on page 26 for details.
- Device power consumption is dependent on Scan Rate. For a higher scan rate, the power consumption is less, and vice versa. Refer to the CY8CMBR2016 Design Guide, section 5 for power calculations.

Sensitivity

- Sensitivity is defined as the minimum change in capacitance which can be detected as a finger touch.
- Use higher sensitivity setting when the overlay thickness is higher, or the button diameter is small.
- Use a lower sensitivity setting when power consumption needs to be low.
- Possible sensitivity settings are “High”, “Medium”, and “Low”.
- Sensitivity can be controlled by the hardware configuration on the SENSITIVITY pin. For details, refer to Table 18 in Appendix on page 26.

System Diagnostics

A built-in power on self test (POST) mechanism detects the following at power on reset (POR), which can be useful in production testing. Any failure is reported on the OUT_6 and OUT_7 pins, as detailed below.

Button Shorted to Ground

If a button is disabled/found shorted to Ground (as shown in Figure 11), then the corresponding bit in the button mask is set, and the same is sent out serially through the OUT_6 pin, synchronised with a 2 kHz clock on OUT_7 pin.

If no clock is sensed on OUT_7 till 300 ms after power-on, then all the buttons have passed the System Diagnostics. If a clock is sensed, then starting from the first falling edge of the clock, each button takes up one clock slot. A high output on OUT_6 during a falling edge on OUT_7 indicates a failure of the button in that clock slot.

The clock output stops after indicating the last failed button. For instance, if Button 1, 3 and 5 are disabled, then the System Diagnostics data is transmitted as shown in Figure 9. CS1 failure is marked by a HIGH on OUT_6 in the 0.5 ms to 1 ms slot. CS3 failure is marked by a HIGH on OUT_6 in the 1.5 ms to 2 ms slot. CS5 failure is marked by a HIGH on OUT_6 in the 2.5 ms to 3 ms slot. After indicating the failure of CS5, clock output is ceased.

As an example, Figure 10 shows the System Diagnostics output when CS1, CS3 and CS15 fail the POST.

Figure 9. System Diagnostics of Disabled Button - Scenario 1

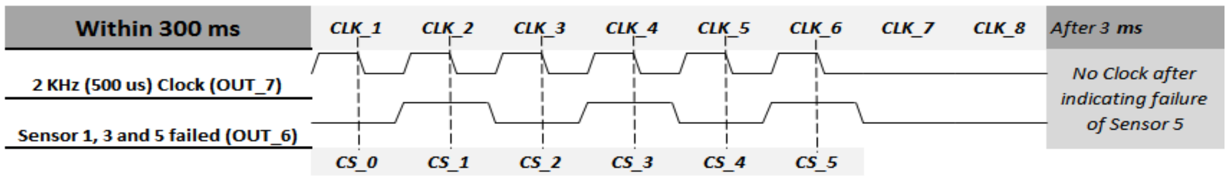


Figure 10. System Diagnostics of Disabled Button - Scenario 2

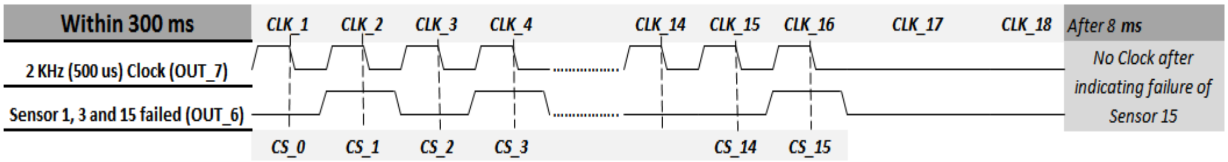
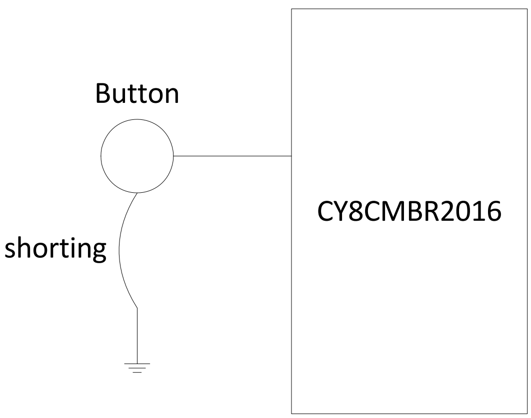


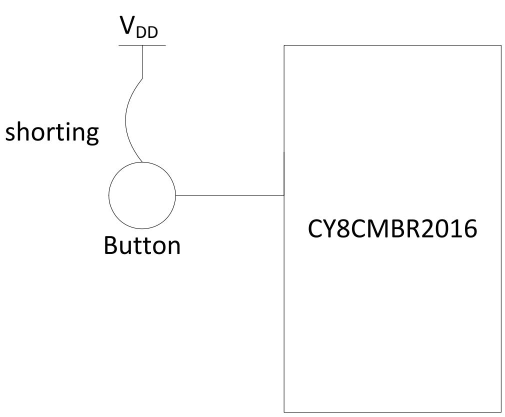
Figure 11. Button Shorted to GND



Button Shorted to V_{DD}

If any button is shorted to V_{DD} that button is disabled and the corresponding bit field is set and System Diagnostics data is sent as defined in button to GND short section.

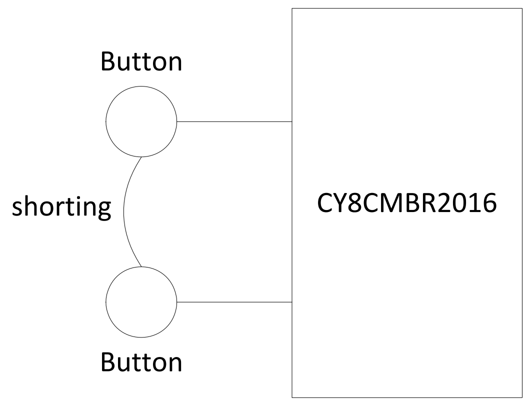
Figure 12. Button Shorted to V_{DD}



Button to Button Short

Any button that are shorted together are disabled and the corresponding bit field is set and System Diagnostics data is sent as defined in button to GND short section.

Figure 13. Button to Button Short



Improper Value of C_{MOD}

- Recommended value of C_{MOD} is 2 nF to 2.4 nF.
- If C_{MOD} of < 1 nF or > 4 nF is connected, all buttons are disabled and the status output will be logic high on all slots.

Button C_P > 40 pF

If the parasitic capacitance (C_P) of any button exceeds 40 pF that button is disabled and the corresponding bit field is set and System Diagnostics data is sent as defined in button to GND short section.

Serial Debug Data Out

- Used to see CapSense data through the Debug pin.
- To enable this feature, the DEBUG pin is pulled down with a 5.6 K resistor.
- The Cypress MultiChart tool can be used to view the debug data for each button
- Serial data is sent out at ~115,200 baud rate
- Firmware revision, CapSense status, baseline, raw counts, difference counts and parasitic capacitances of all sensors are sent out

For more information on Raw Count, Baseline, Difference Count, and Parasitic Capacitance, refer Getting Started with CapSense, section 2.

For more information on MultiChart tool, refer AN2397 - CapSense Data Viewing Tools, method 2.

- The MultiChart tool arranges the data in the format as shown in Table 5 on page 13.
- The Serial Debug Data is sent by the device in the order shown in Table 6 on page 13.

Table 5. Serial Debug Data Arranged in MultiChart

Sl. No.	Raw Count Array		Baseline Array		Difference Count array	
	MSB	LSB	MSB	LSB	MSB	LSB
0	CS0_RC		CS0_BL		CS0_DIFF	
1	CS1_RC		CS1_BL		CS1_DIFF	
2	CS2_RC		CS2_BL		CS2_DIFF	
3	CS3_RC		CS3_BL		CS3_DIFF	
4	CS4_RC		CS4_BL		CS4_DIFF	
5	CS5_RC		CS5_BL		CS5_DIFF	
6	CS6_RC		CS6_BL		CS6_DIFF	
7	CS7_RC		CS7_BL		CS7_DIFF	
8	CS8_RC		CS8_BL		CS8_DIFF	
9	CS9_RC		CS9_BL		CS9_DIFF	
10	CS10_RC		CS10_BL		CS10_DIFF	
11	CS11_RC		CS11_BL		CS11_DIFF	
12	CS12_RC		CS12_BL		CS12_DIFF	
13	CS13_RC		CS13_BL		CS13_DIFF	
14	CS14_RC		CS14_BL		CS14_DIFF	
15	CS15_RC		CS15_BL		CS15_DIFF	
16	0x00	F/W Rev	CS_Status		0x00	CS10_CP
17	0x00	CS0_CP	0x00	CS5_CP	0x00	CS11_CP
18	0x00	CS1_CP	0x00	CS6_CP	0x00	CS12_CP
19	0x00	CS2_CP	0x00	CS7_CP	0x00	CS13_CP
20	0x00	CS3_CP	0x00	CS8_CP	0x00	CS14_CP
21	0x00	CS4_CP	0x00	CS9_CP	0x00	CS15_CP

Table 6. Serial Data Output sent by CY8CMBR2016

BYTE	DATA	Notes
0	0x0D	Dummy variables for multi chart tool
1	0x0A	
2	CS0_RC	CS0 Raw counts, unsigned 16-bit integer
3		
4	CS1_RC	CS1 Raw counts, unsigned 16-bit integer
5		
6	CS2_RC	CS2 Raw counts, unsigned 16-bit integer
7		
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Table 6. Serial Data Output sent by CY8CMBR2016 *(continued)*

BYTE	DATA	Notes
32	CS15_RC	CS15 Raw counts, unsigned 16-bit integer
33		
34	0x00	–
35	FW_REV	Firmware revision
36	0x00	–
37	CS0_CP	Parasitic capacitance of CS0
38	0x00	–
39	CS1_CP	Parasitic capacitance of CS1
40	0x00	–
41	CS2_CP	Parasitic capacitance of CS2
42	0x00	–
43	CS3_CP	Parasitic capacitance of CS3
44	0x00	–
45	CS4_CP	Parasitic capacitance of CS4
46	CS0_BL	CS0 Baseline, unsigned 16-bit integer
47		
48	CS1_BL	CS1 Baseline, unsigned 16-bit integer
49		
50	CS2_BL	CS2 Baseline, unsigned 16-bit integer
51		
	------------	--
76	CS15_BL	CS15 Baseline, unsigned 16-bit integer
77		
78 79	CS_Status	CapSense Status, unsigned 16 bit integer –
80	0x00	–
81	CS5_CP	Parasitic capacitance of CS5
82	0x00	–
83	CS6_CP	Parasitic capacitance of CS6
84	0x00	–
85	CS7_CP	Parasitic capacitance of CS7
86	0x00	–
87	CS8_CP	Parasitic capacitance of CS8
88	0x00	–
89	CS9_CP	Parasitic capacitance of CS9
90	CS0_DIFF	CS0 difference counts, unsigned 16-bit integer
91 92	CS1_ DIFF	CS1 difference counts, unsigned 16-bit integer
93 94	CS2_ DIFF	CS2 difference counts, unsigned 16-bit integer
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Table 6. Serial Data Output sent by CY8CMBR2016 *(continued)*

BYTE	DATA	Notes
121	CS15_ DIFF	CS15 difference counts, unsigned 16-bit integer
122		
123	0x00	–
124	CS10_CP	Parasitic capacitance of CS10
125	0x00	–
126	CS11_CP	Parasitic capacitance of CS11
127	0x00	–
128	CS12_CP	Parasitic capacitance of CS12
129	0x00	–
130	CS13_CP	Parasitic capacitance of CS13
131	0x00	–
132	CS14_CP	Parasitic capacitance of CS14
133	0x00	–
134	CS15_CP	Parasitic capacitance of CS15
135	0x00	Dummy variable for multi chart tool
136	0xFF	
137	0xFF	

Power Consumption and Device Operating Modes

The CY8CMBR2016 is designed to meet the low power requirements of battery powered applications. To design for the lowest operating current -

- Ground all unused CapSense inputs
- Minimize Cp using the design guidelines in Getting Started with CapSense, section 3.7.1.
- Lower the supply voltage.
- Use a higher Button Scan Rate or Deep Sleep operating mode.

To know more about the steps to reduce power consumption, refer to CY8CMBR2016 Design Guide, section 5.

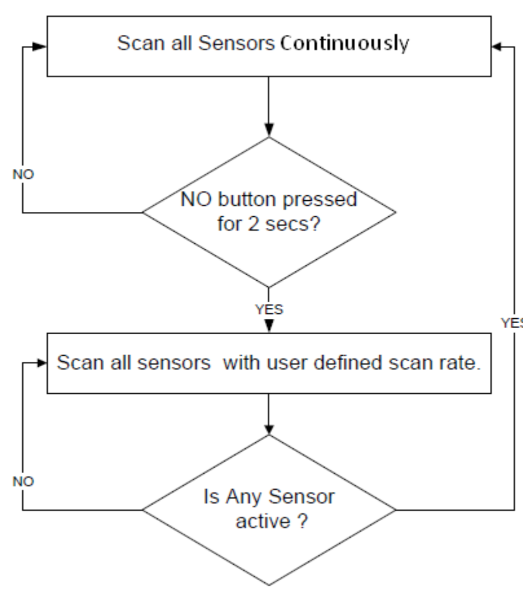
There are two device operating modes:

- Low power sleep mode
- Deep sleep mode

Low Power Sleep Mode

The following flow chart describes the low power sleep mode operation.

Figure 14. Low Power Sleep Mode Operation



For details on Low power sleep look at the Scan Rate on page 11 section.

Response Time

Response Time is the minimum amount of time the button should be touched for the device to detect as valid button touch.

It is given by the following equations -

RT_{FBT} =User defined Button Scan Rate + 40 ms

RT_{CBT} = 40 ms

Where,

RT_{FBT} is Response time for first button touch

RT_{CBT} is Response time for consecutive button touch after first button touch

Refer to Scan Rate on page 11 section for more details on the User defined Button Scan Rate.

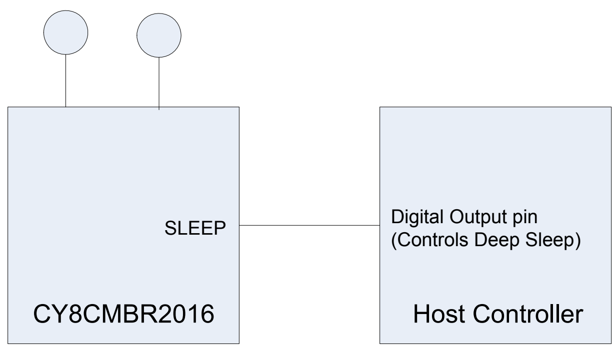
For example, consider a nine button design with the User defined Button Scan Rate set to Low (250 ms). The response time for such a design is given as:

RT_{FBT} =250+40=290 ms

RT_{CBT} = 40 ms

Deep Sleep Mode

Figure 15. SLEEP Pin Configuration to Enable Deep Sleep



- To enable the deep sleep mode, the hardware configuration pin Sleep should be connected to the master device.
- Master should pull the pin to V_{DD} for the device to go into deep sleep.
- The master output pin should be in strong drive mode, so that the Sleep pin is not left floating.
- In deep sleep mode, all blocks are turned off and the device power consumption is 0.1 µA.
- There is no CapSense scanning in deep sleep mode.
- Sleep pin should be pulled low for the device to wake up from deep sleep.
- When device comes out of deep sleep mode, the CapSense system is reinitialized. Typical time for re-initialization is 8 ms.Any button press within this time is not reported.
- After the device comes out of deep sleep, the device operates in low power sleep mode.
- If the Sleep pin is pulled high at power on, then the device does not go to deep sleep immediately. The device goes to deep sleep after initializing all internal blocks and scanning all sensors once.
- If the Sleep pin is pulled high at power on, then the scan rate is calculated when the device is taken out of Deep Sleep by the master.

Layout Guidelines and Best Practices

Table 7. Layout Guidelines

Sl. No.	Category	Min	Max	Recommendations/Remarks
1.	Button shape	–	–	Solid round pattern, Round with LED hole, rectangle with round corners
2.	Button size	5 mm	15 mm	Given in layout estimator sheet
3.	Button-Button spacing	equal to button ground clearance		8 mm
4.	Button ground clearance	0.5 mm	2 mm	Given in layout estimator sheet
5.	Ground flood - Top layer	–	–	Hatched ground 7 mil trace and 45 mil grid (15% filling)
6.	Ground flood - bottom layer	–	–	Hatched ground 7 mil trace and 70 mil grid (10% filling)
7.	Trace length from sensor to device pin	–	450	Given in layout estimator sheet
8.	Trace width	0.17 mm	0.20 mm	0.17 mm (7 mil)
9.	Trace routing	–	–	Traces should be routed on the non sensor side. If any non CapSense trace crosses CapSense trace, ensure that intersection is orthogonal.
10.	Via position for the sensors	–	–	Via should be placed near the edge of the button to reduce trace length thereby increasing sensitivity.
11.	Via hole size for sensor traces	–	–	10 mil
12.	No. of via on sensor trace	1	2	1

Table 7. Layout Guidelines *(continued)*

Sl. No.	Category	Min	Max	Recommendations/Remarks
13.	CapSense series resistor placement	–	10 mm	Place CapSense series resistors close to the device for noise suppression.CapSense resistors have highest priority compared to other resistors, so place them first.
14.	Distance between any CapSense trace to ground flood	10 mil	20 mil	20 mil
15.	Device placement	–	–	Mount the device on the layer opposite to sensor. The CapSense trace length between the device and sensors should be minimum (see trace length above)
16.	Placement of components in two layer PCB	–	–	Top layer-Sensors and bottom layer-device, other components and traces.
17.	Placement of components in four layer PCB	–	–	Top layer-Sensors, second layer – CapSense traces & Vdd and avoid the Vdd traces below the sensors, third layer-hatched ground, Bottom layer- device other components and non CapSense traces
18.	Overlay thickness	0 mm	5 mm	Use layout estimator sheet to decide on overlay, given maximum limit is for plastic overlay.
19.	Overlay material	–	–	Should to be non-conductive material. Glass, ABS Plastic, Formica, wood etc. No air gap should be there between PCB and overlay. Use adhesive to stick the PCB and overlay.
20.	Overlay adhesives	–	–	Adhesive should be non conductive and dielectrically homogenous. 467 MP and 468 MP adhesives made by 3 M are recommended.
21.	Board thickness	–	–	Standard board thickness for CapSense FR4 based designs is 1.6 mm.

Figure 16. CapSense Button Shapes

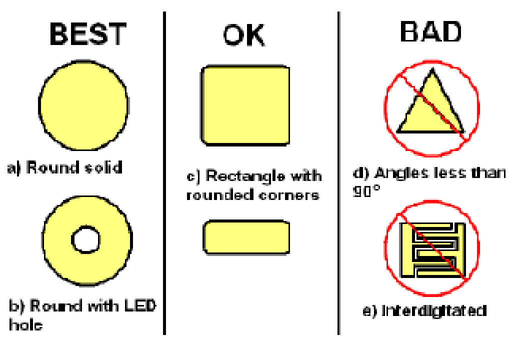
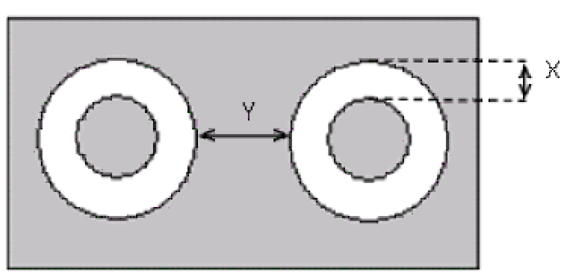


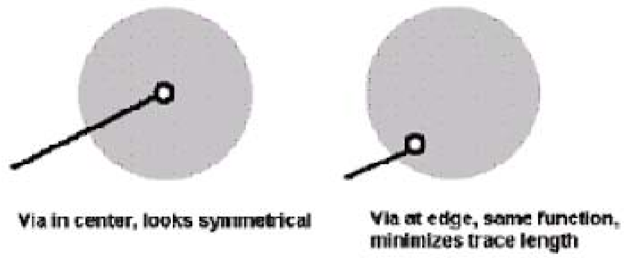
Figure 17. Button Layout Design



X: Button to ground clearance (Refer to Layout Guidelines and Best Practices on page 16)

Y: Button to button clearance (Refer to Layout Guidelines and Best Practices on page 16)

Figure 18. Recommended via Hole Placement



Sample Layout

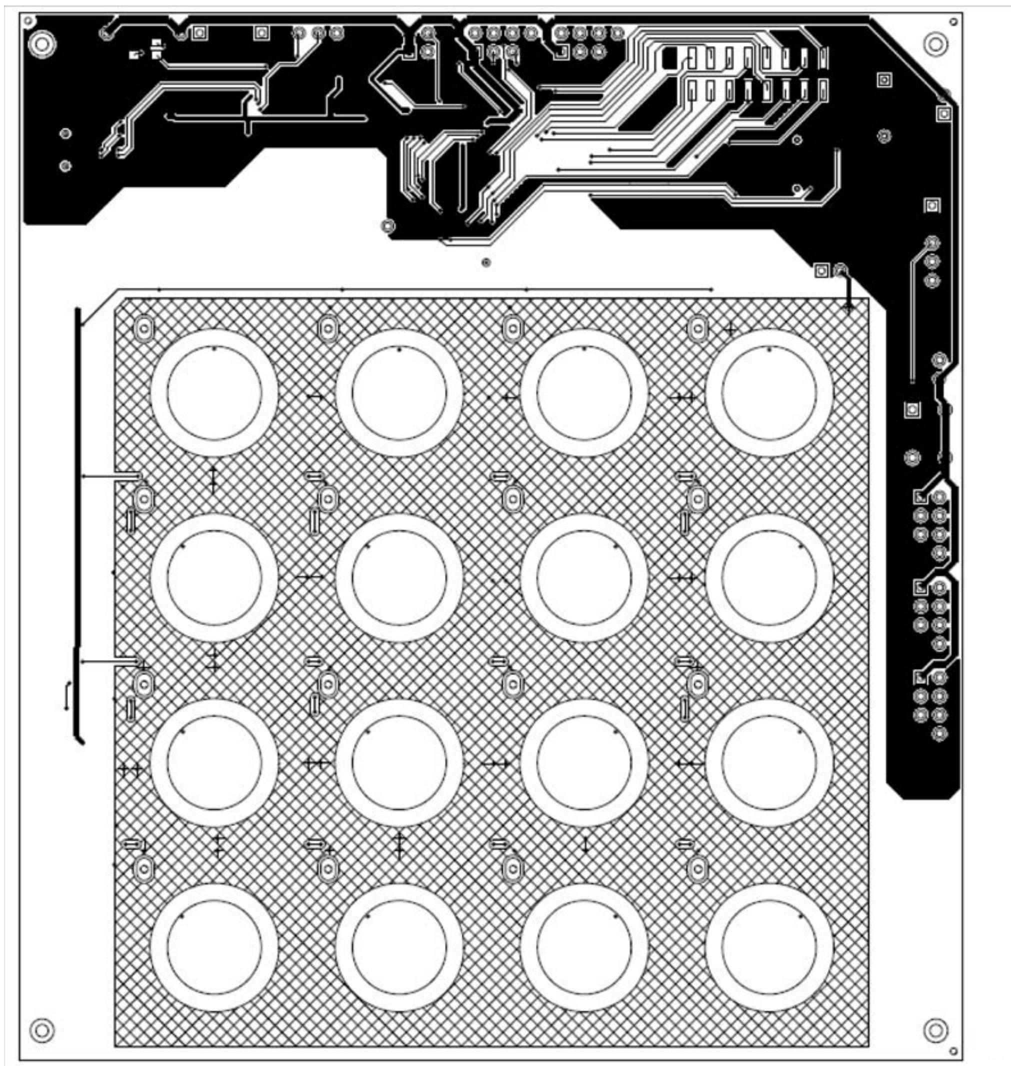
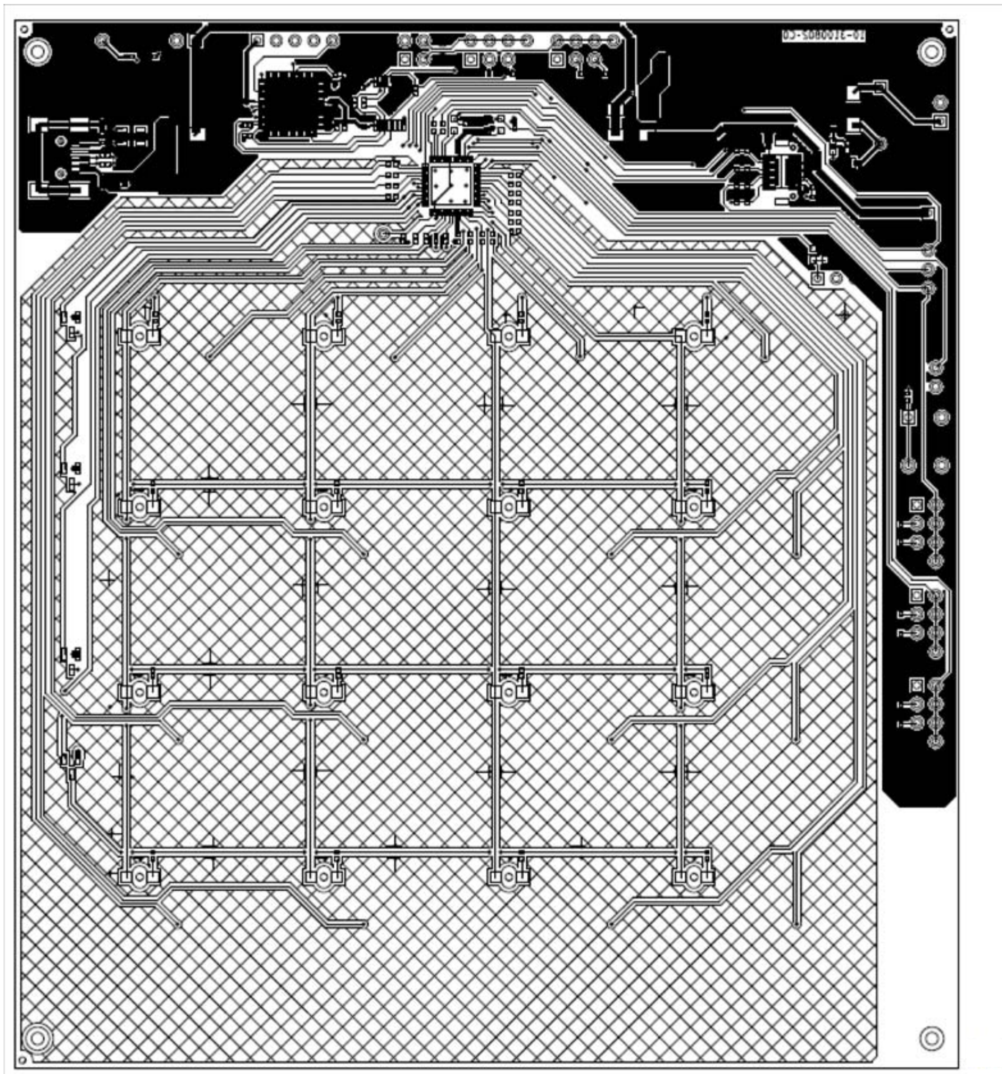


Figure 19. Top Layer

Figure 20. Bottom Layer



Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CMBR2044 device.

Table 8. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	25	+125	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrade reliability.
V_{DD}	Supply voltage relative to V_{SS}	–0.5	–	+6.0	V	–
V_{IO}	DC voltage on CapSense inputs and digital output pins	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
I_{MIG}	Maximum current into any GPO output pin	–25	–	+50	mA	–
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch up current	–	–	200	mA	In accordance with JESD78 standard

Table 9. Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_A	Ambient temperature	–40	–	+85	°C	–
T_C	Commercial temperature	0	–	+70	°C	–
T_J	Operational die temperature	–40	–	+100	°C	–

DC Electrical Characteristics

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 10. DC Chip Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}[4, 5, 6]	Supply voltage	1.71	–	5.5	V	–
I_{DD}	Supply current	–	3.3	4.0	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C
I_{DA}	Active current	–	3.3	4.0	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, continuous sensor scan
I_{DS}	Deep sleep current	–	0.1	0.5	µA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C
I_{AV1}	Average current	–	0.25	–	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C and 16 buttons used, with 0% touch time, C_P of all sensors < 19 pFand scan rate = 250 ms
I_{AV2}	Average current	–	2.13	–	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C and 16 buttons used, with 50% touch time, C_P of all sensors < 19 pFand scan rate = 250 ms, Key Scan mode enabled
I_{AV3}	Average current	–	0.42	–	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C and 16 buttons used, with 0% touch time, C_P of all sensors >19 pF and < 40 pF and scan rate = 250 ms
I_{AV4}	Average current	–	2.2	–	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C and 16 buttons used, with 50% touch time, C_P of all sensors >19 pF and < 40 pF and scan rate = 250 ms, Key Scan mode enabled

Notes

4. When V_{DD} remains in the range from 1.75 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.75 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs. This helps to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
5. After power down, ensure that V_{DD} falls below 100 mV before powering backup.
6. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V

DC General Purpose I/O Specifications

These tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 11. 3.0 V to 5.5 V DC General Purpose I/O Specification

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on all output pins	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, Maximum of 40 µA source in all I/Os
V_{OH2}	High output voltage on OUT pins	V_{DD} – 0.9	–	–	V	I_{OH} = 1 mA, Maximum of 2 mA source in all I/Os
V_{OH3}	High output voltage on INT and BUZZ pins	V_{DD} – 0.9	–	–	V	I_{OH} = 5 mA, Maximum of 10 mA source in all I/Os
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 25 mA/pin, V_{DD} > 3.3 V, Maximum of 60 mA source in all I/Os
V_{IL}	Input low voltage	–	–	0.80	V	–
V_{IH}	Input high voltage	2.00	–	–	V	–

Table 12. 2.4 V to 3.0 V DC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on all outputs	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, Maximum of 40 µA Source in all I/Os
V_{OH2}	High output voltage on OUT pins	V_{DD} – 0.4	–	–	V	I_{OH} = 0.2 mA, Maximum of 0.4 mA source in all I/Os
V_{OH3}	High output voltage on INT and BUZZ	V_{DD} – 0.5	–	–	V	I_{OH} = 2 mA, Maximum of 4 mA source in all I/Os
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 10 mA/pin, V_{DD} > 3.3 V, Maximum of 30 mA source in all I/Os
V_{IL}	Input low voltage	–	–	0.72	V	–
V_{IH}	Input high voltage	1.40	–	–	V	–

Table 13. 1.71 V to 2.4 V DC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH1}	High output voltage on OUT pins	V_{DD} – 0.2	–	–	V	I_{OH} =10 µA, maximum of 20 µA source in all I/Os
V_{OH2}	High output voltage on OUT pins	V_{DD} – 0.5	–	–	V	I_{OH} = 0.5 mA, maximum of 1 mA source in all I/Os
V_{OH3}	High output voltage on INT and BUZZ	V_{DD} – 0.2	–	–	V	I_{OH} =100 µA, maximum of 200 µA source in all I/Os
V_{OH4}	High output voltage on INT and BUZZ	V_{DD} – 0.5	–	–	V	I_{OH} = 2 mA, maximum of 4 mA source in all I/Os
V_{OL}	Low output voltage	–	–	0.4	V	I_{OL} = 5 mA/pin, V_{DD} > 3.3 V, maximum of 20 mA source in all I/Os
V_{IL}	Input low voltage	–	–	0.30 × V_{DD}	V	–
V_{IH}	Input high voltage	0.65 × V_{DD}	–	–	V	–

AC Electrical Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 14. AC Chip-Level Specifications

Parameter	Description	Min	Max	Unit	Notes
SR_{POWER_UP}	Power supply slew rate	–	250	V/ms	V_{DD}slew rate during power-up
T_{XRST}	External reset pulse width at power-up	1	–	ms	Applicable after device power supply is active
T_{XRST2}	External reset pulse width after power-up	10	–	ms	Applicable after device V_{DD} has reached maximum value

Table 15. AC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{Rise1}	Rise time on OUT pins, Cload = 50 pF	15	–	80	ns	VDD = 3.0 to 3.6 V, 10%–90%
T_{Rise2}	Rise time on INT and BUZZ pins, Cload = 50 pF	10	–	50	ns	VDD = 3.0 to 3.6 V, 10%–90%
T_{Rise3}	Rise time on OUT pins, Cload = 50 pF	15	–	80	ns	VDD = 1.71 to 3.0 V, 10%–90%
T_{Rise4}	Rise time on INT and BUZZ pins, Cload = 50 pF	10	–	80	ns	VDD = 1.71 to 3.0 V, 10%–90%
T_{Fall1}	Fall time, Cload = 50 pF all outputs	10	–	50	ns	VDD = 3.0 to 3.6 V, 90%–10%
T_{Fall2}	Fall time, Cload = 50 pF all outputs	10	–	70	ns	VDD = 1.71 to 3.0 V, 90%–10%

CapSense Specification

Parameter	Description	Min	Typ	Max	Unit	Notes
C_P	Parasitic capacitance	5.0	–	$(C_P+C_F)<40$	pF	C_P is the total capacitance seen by the pin when no finger is present. C_P is sum of C_sensor, C_trace, and Capacitance of the vias and C_{PIN}
C_F	Finger capacitance	0.25	–	$(C_P+C_F)<40$	pF	C_F is the capacitance added by the finger touch
C_{PIN}	Capacitive load on pins as input	0.5	1.7	7	pF	Mandatory for CapSense to work
C_{MOD}	External modulator capacitor	2	2.2	2.4	nF	Mandatory for CapSense to work
R_S	Series resistor between pin and the button	–	560	616	Ω	Reduces the RF noise

Package Information

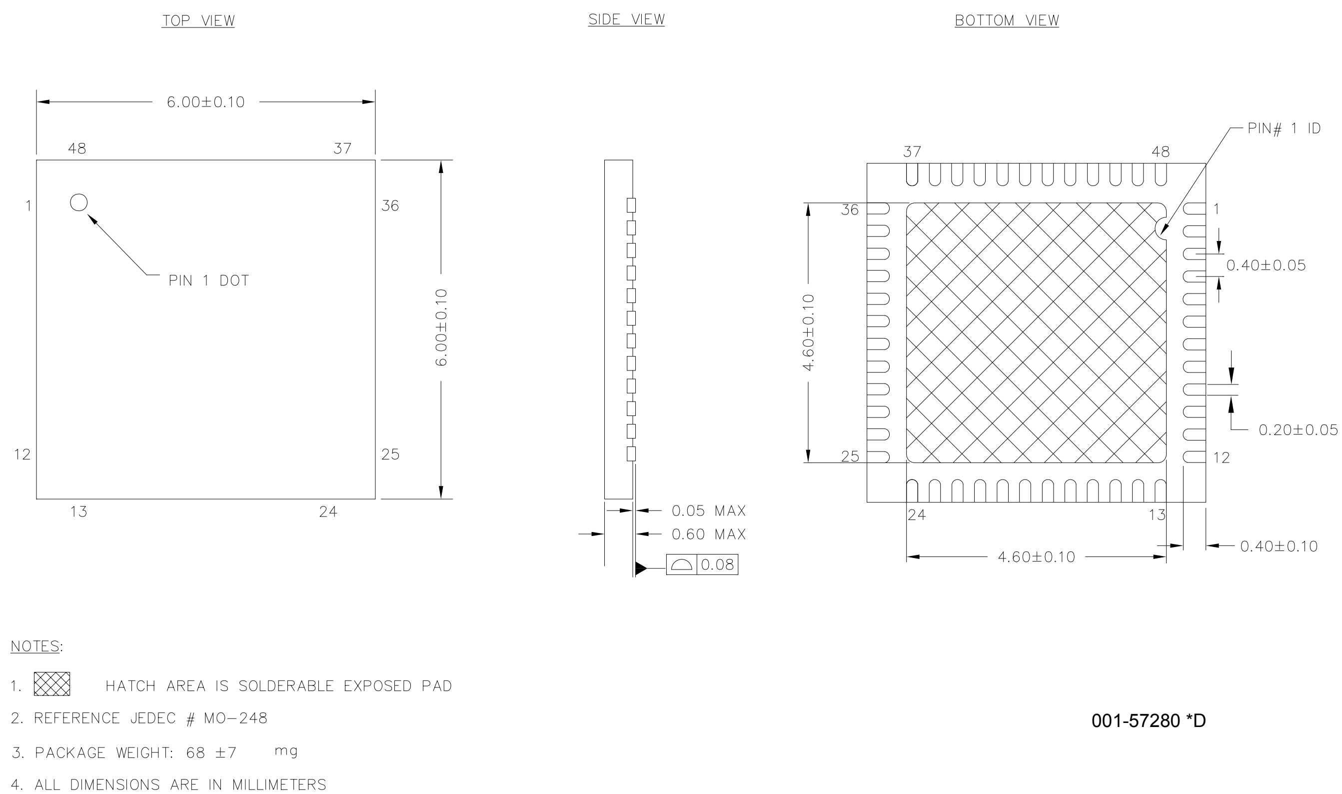
Table 16. Thermal Impedances by Package

Package	Typical θ_{JA} [7]
48-pin QFN [8]	19 °C/W

Table 17. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature [9]	Maximum Peak Temperature	Time at Max Temperature
48-pin QFN	240 °C	260 °C	30 s

Figure 21. 48-pin (6 × 6 × 0.6 mm) QFN



Notes
7. $T_J = T_A + \text{Power} \times \theta_{JA}$
8. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane
9. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications

Ordering Information

Ordering Code	Package Type	Operating Temperature	CapSense Inputs	Other I/Os	XRES pin
CY8CMBR2016-24LQXI	48-pin (6 × 6 × 0.6 mm) QFN	Industrial	17 [10]	17 [11]	Yes
CY8CMBR2016-24LQXIT	48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	Industrial	17 [10]	17 [11]	Yes

Ordering Code Definitions

CY 8 C MBR 2016 - 24 LQX I (T)

- **T** = Tape and Reel, Blank = Standard
- **Temperature Range:** I = Industrial
- **Package Code:** LQX = QFN Pb-free
- **Speed:** 24 MHz
- **Part Number:** 2016
- **MBR** = Mechanical Button Replacement
- **Technology Code:** C = CMOS
- **Marketing Code:** 8 = PSoC
- **Company ID:** CY = Cypress

Notes

10. 16 CapSense input + 1 C_{MOD} pin
11. 8 Configurable GPIOs + 1 buzzer output + 1 Sleep line + 1 Interrupt line + 1 Debug line + 5 configuration pins

Appendix

Table 18. Device Features versus Resistor Configuration Matrix

Features	Comments	Pin configuration	Device Pin Name
Flanking Sensor Suppression (FSS)	Disabled	Ground	FSS
	Enabled	VDD / Floating	
Button Auto Reset	Enabled, Auto Reset period = 5 ms	Ground	ARST
	Enabled, Auto Reset period = 20 ms	1.5 kΩ (±5%) to ground	
	Enabled, Auto Reset period = 40 ms	5 kΩ (±5%) to ground	
	Disabled	VDD / Floating	
Output Select	Truth Table I/F	Ground	OUT_SEL
	Encoded 4 bit output	1.5 kΩ (±5%) to ground	
	Keypad scanning interface output	VDD / Floating	
Scan Rate	Low, 250 ms	Ground	SCAN
	Medium, 150 ms	1.5 kΩ (±5%) to ground	
	High, 40 ms	5 kΩ (±5%) to ground	
	Continuous scan	VDD / Floating	
Sensitivity	Low	Ground	SENSITIVITY
	Medium	1.5 kΩ (±5%) to ground	
	High	VDD / Floating	
Deep Sleep Mode	Device out of Deep Sleep	Ground	SLEEP
	Device in Deep Sleep	VDD	

Acronyms

Acronym	Description
AC	alternating current
C_F	finger capacitance
C_{MOD}	modulator capacitor
C_P	parasitic capacitance
EO_x	Encoded Output - Bit ‘x’
FMEA	failure mode effect analysis
FSS	flanking sensor suppression
ODL	Open Drain Low
POR	power-on reset
POST	power on self test
QFN	quad flat no leads
RF	radio frequency
READ_x	KeyScan Interface - ‘x’th Read line
SCAN_x	KeyScan Interface - ‘x’th Scan line
SNR	signal-to-noise ratio
TT_COL_x	Truth Table Column output - ‘x’th Column
TT_ROW_x	Truth Table Row output - ‘x’th Row

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μF	microfarad
μs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
nF	nanofarad
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
s	second
V	volt
W	watt

Document History Page

Document Title: CY8CMBR2016, CapSense® Express™ 16 Button Matrix Controller Document Number: 001-67921				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3202566	MSUR	03/22/2011	New datasheet
*A	3387102	MSUR	10/10/2011	Changed status from Preliminary to Final. Added Char data into the table and some minor edits to the document.
*B	3473096	MSUR	12/22/2011	No technical updates.
*C	3633927	UDYG	10/31/2012	Updated title. Updated Features, Scan Rate, Sensitivity, and Button Shorted to Ground section. Added parameters V_{IL} and V_{IH} in Table 11, Table 12, and Table 13, and parameter T_C in Table 9. Added Figure 15 and section Response Time. Updated Package Information.

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