CYP15G0402DXB
CYV15G0402DXB

Quad HOTLink II™ SERDES

Features

- **Second-generation HOTLink® technology**
- **Fibre Channel- and Gigabit Ethernet-compliant**
- **ESCON®, DVB-ASI-compliant**
- **SMPTE-292M-, SMPTE-259M-compliant**
- **10-bit unencoded data transport**
  - **Aggregate throughput of 12 GBps**
- **Selectable parity check/generate**
- **Four independently controlled 10-bit channels**
- **Selectable input clocking options**
- **MultiFrame™ Receive Framer provides alignment to**
  - **Comma or full K28.5 detect**
  - **Single or multi-byte framer for byte alignment**
  - **Low-latency option**
- **Synchronous LVTTL parallel input interface**
- **Synchronous LVTTL parallel output interface**
- **195-to-1500 MBaud serial signaling rate**
- **Internal phase-locked loops (PLLs) with *no* external PLL components**
- **Differential PECL-compatible serial inputs**
- **Differential PECL-compatible serial outputs**
  - **Source matched for 50Ω transmission lines**
  - **No external resistors required**
  - **Signaling-rate controlled edge-rates**
- **Compatible with**
  - **Fiber-optic modules**
  - **Copper cables**
  - **Circuit board traces**
- **JTAG boundary scan**
- **Built-In Self-Test (BIST) for at-speed link testing**
- **Per-channel Link Quality Indicator**
  - **Analog signal detect**
  - **Digital signal detect**
- **Low-power 2.5W @3.3V typical**
- **Single 3.3V supply**
- **256-ball thermally enhanced BGA**
- **0.25µ BiCMOS technology**

Functional Description

The CYP(V)15G0402DXB Quad HOTLink II™ SERDES is a point-to-point communications building block allowing the transfer of preencoded data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at signaling speeds ranging from 195 to 1500 MBaud per serial link.

Each transmit channel accepts preencoded 10-bit transmission characters in an Input Register, serializes each character, and drives it out a PECL-compatible differential line driver. Each receive channel accepts a serial data stream at a differential line receiver, deserializes the stream into 10-bit characters, frames these characters to the proper 10-bit character boundaries and presents these characters to an Output register. *Figure 1* illustrates typical connections between independent systems and a CYP(V)15G0402DXB .

The CYV15G0402DXB satisfies the SMPTE-259M and SMPTE-292M compliance as per the EG34-1999 Pathological Test Requirements.

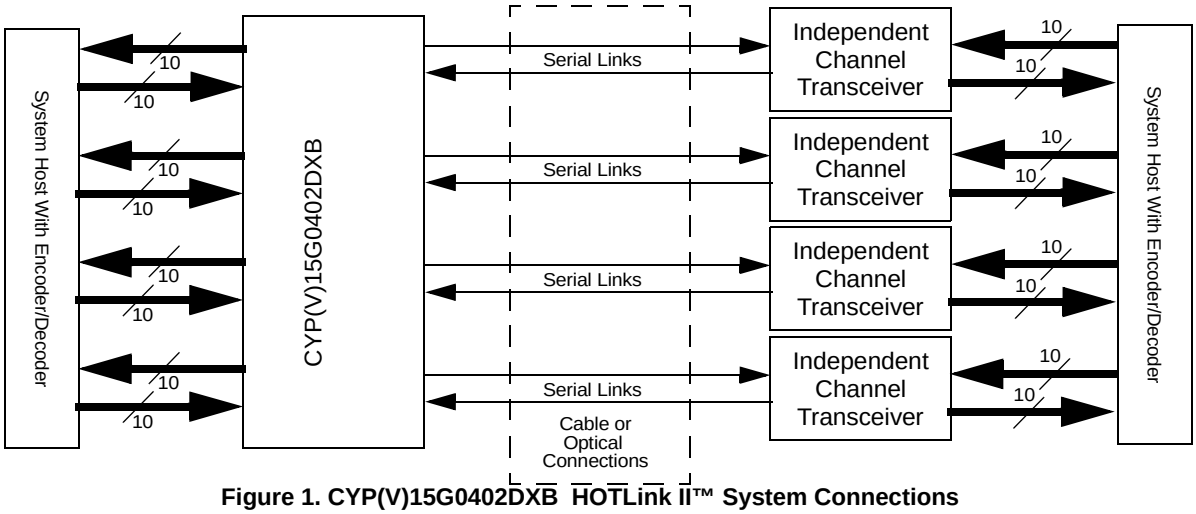


Figure 1. CYP(V)15G0402DXB HOTLink II™ System Connections

Note:

1. CYV15G0402DXB refers to the SMPTE compliant parts. CYP15G0402DXB refers to the non-video part. CYP(V)15G0402DXB corresponds to both the video and non-video parts of the transceiver.

As a second-generation HOTLink device, the CYP(V)15G0402DXB extends the HOTLink family to faster data rates, while maintaining serial link compatibility (data, command and BIST) with other HOTLink devices.The transmit (TX) section of the CYP(V)15G0402DXB Quad HOTLink II SERDES consists of four ten bit wide channels that accept a preencoded character on every clock cycle. Transmission characters are passed from the Transmit Input Register to a Serializer. The serialized characters are output from a differential transmission line driver at a bit-rate of 10 or 20 times the input reference clock.

The receive (RX) section of the CYP(V)15G0402DXB Quad HOTLink II SERDES consists of four ten bit wide channels. Each channel accepts a serial bit-stream from a PECL-compatible differential line receiver and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. Each recovered bit-stream is deserialized and framed into characters. Recovered characters are then passed to the receiver output register, along with a recovered character clock.

The parallel I/O interface may be configured for numerous forms of clocking to provide the highest flexibility in system architecture. In addition to clocking the transmit path, the receive interface may be configured to present data relative to a recovered clock or to a local reference clock.

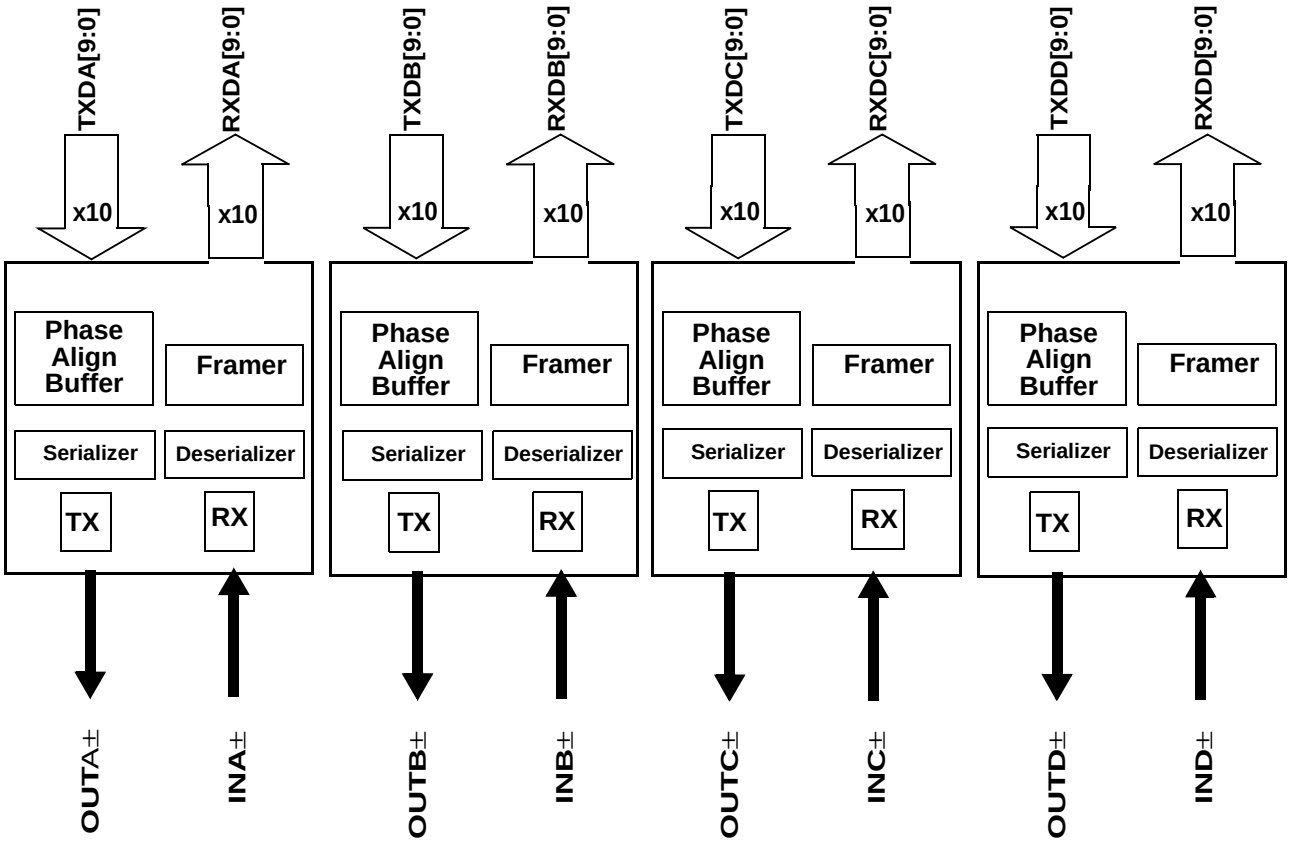
Each transmit and receive channel contains an independent BIST pattern generator and checker. This BIST hardware allows at-speed testing of the interface data path.

HOTLink II devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting backplanes on switches, routers, servers and video transmission systems

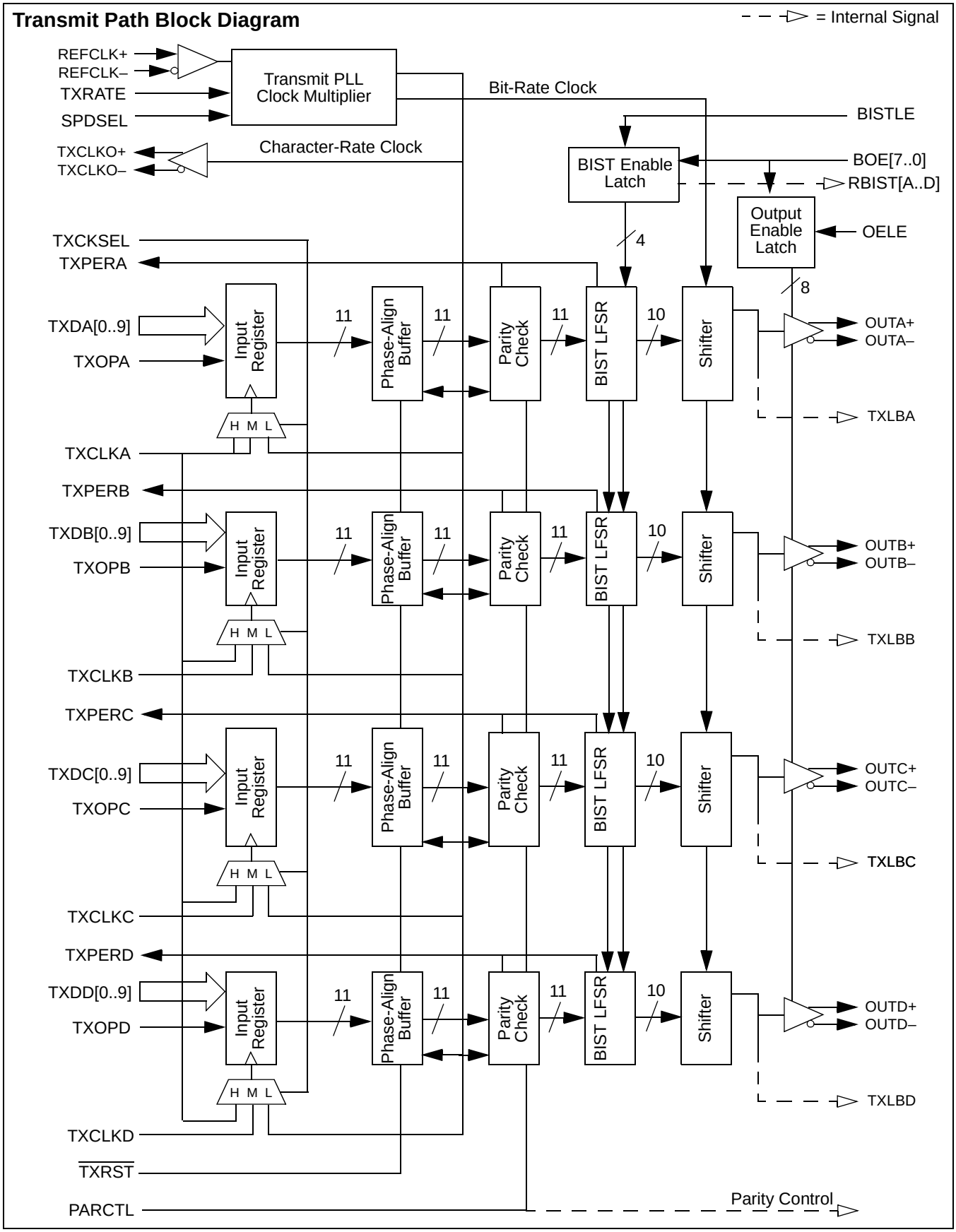
CYV15G0402DXB is tested for the pathological test patterns for SMPTE-259 and SMPTE-292M compliance as per the EG34-1999 Pathological Test Requirements. The test is done for the following patterns.

1. Screen parts at the required pattern of 20 high and 20 low bits continuously for burst of 20.
2. Screen parts at a single burst of 44 low or high periods.
3. Screen parts at a pattern of 19 high and 1 low or 19 low and 1 high bit for a pattern of 20.

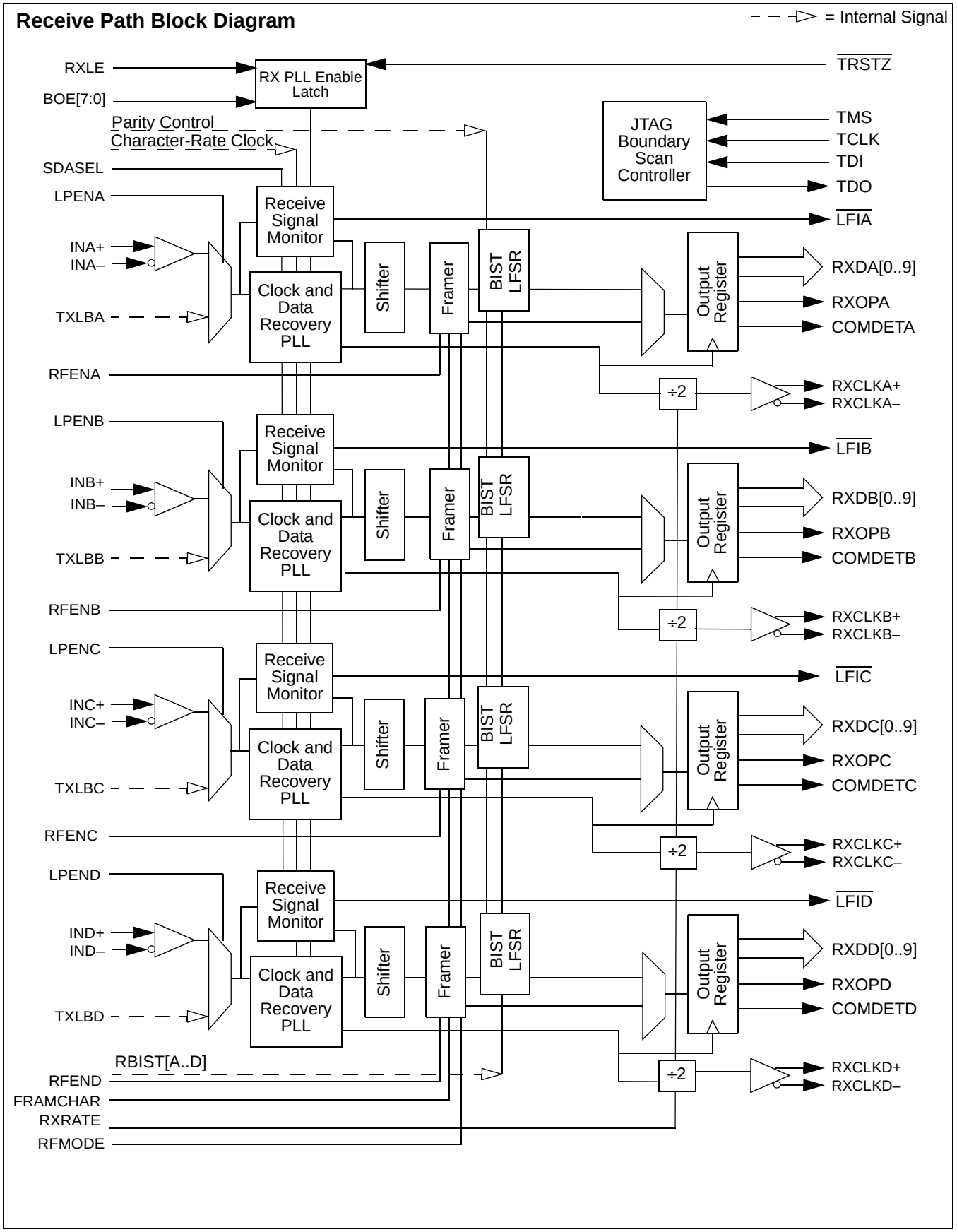
CYP(V)15G0402DXB Transceiver Logic Block Diagram



Transmit Path Block Diagram



Receive Path Block Diagram



Pin Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	INC-	OUTC-	N/C	N/C	**V_{CC}**	IND-	OUTD-	**GND**	N/C	N/C	INA-	OUTA-	**GND**	N/C	N/C	**V_{CC}**	INB-	OUTB-	N/C	N/C
B	INC+	OUTC+	N/C	N/C	**V_{CC}**	IND+	OUTD+	**GND**	N/C	N/C	INA+	OUTA+	**GND**	N/C	N/C	**V_{CC}**	INB+	OUTB+	N/C	N/C
C	TDI	TMS	LPENC	LPENB	**V_{CC}**	PARCTL	SDASEL	**GND**	BOE[7]	BOE[5]	BOE[3]	BOE[1]	**GND**	**GND**	**GND**	**V_{CC}**	TXRATE	RXRATE	N/C	TDO
D	TCLK	$\overline{\text{TRSTZ}}$	LPEND	LPENA	**V_{CC}**	RF MODE	SPDSEL	**GND**	BOE[6]	BOE[4]	BOE[2]	BOE[0]	**GND**	**GND**	**GND**	**V_{CC}**	N/C	RXLE	N/C	N/C
E	**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**
F	TXPERC	TXOPC	TXDC[0]	N/C													BISTLE	RXDB[0]	RXOPB	RXDB[1]
G	TXDC[7]	TXCKSEL	TXDC[4]	TXDC[1]													GND	OELE	FRAMCHAR	RXDB[3]
H	**GND**	**GND**	**GND**	**GND**													**GND**	**GND**	**GND**	**GND**
J	TXDC[9]	TXDC[5]	TXDC[2]	TXDC[3]													COMDETB	RXDB[2]	RXDB[7]	RXDB[4]
K	RXDC[4]	RXCLKC-	TXDC[8]	LFIC													RXDB[5]	RXDB[6]	RXDB[9]	RXCLKB+
L	RXDC[5]	RXCLKC+	TXCLKC	TXDC[6]													RXDB[8]	LFIB	RXCLKB-	TXDB[6]
M	RXDC[6]	RXDC[7]	RXDC[9]	RXDC[8]													TXDB[9]	TXDB[8]	TXDB[7]	TXCLKB
N	**GND**	**GND**	**GND**	**GND**													**GND**	**GND**	**GND**	**GND**
P	RXDC[3]	RXDC[2]	RXDC[1]	RXDC[0]													TXDB[5]	TXDB[4]	TXDB[3]	TXDB[2]
R	COMDETC	RXOPC	TXPERD	TXOPD													TXDB[1]	TXDB[0]	TXOPB	TXPERB
T	**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**
U	TXDD[0]	TXDD[1]	TXDD[2]	TXDD[9]	VCC	RXDD[4]	RXDD[3]	GND	RXOPD	RFENC	REFCLK-	TXDA[1]	GND	TXDA[4]	TXDA[8]	VCC	RXDA[4]	RXOPA	COMDETA	RXDA[0]
V	TXDD[3]	TXDD[4]	TXDD[8]	RXDD[8]	VCC	RXDD[5]	RXDD[1]	GND	COMDETD	RFEND	REFCLK+	RFENB	GND	TXDA[3]	TXDA[7]	VCC	RXDA[9]	RXDA[5]	RXDA[2]	RXDA[1]
W	TXDD[5]	TXDD[7]	LFID	RXCLKD–	VCC	RXDD[6]	RXDD[0]	GND	TXCLKO–	TXRST	TXOPA	RFENA	GND	TXDA[2]	TXDA[6]	VCC	LFIA	RXCLKA–	RXDA[6]	RXDA[3]
Y	TXDD[6]	TXCLKD	RXDD[9]	RXCLKD+	VCC	RXDD[7]	RXDD[2]	GND	TXCLKO+	N/C	TXCLKA	TXPERA	GND	TXDA[0]	TXDA[5]	VCC	TXDA[9]	RXCLKA+	RXDA[8]	RXDA[7]

Pin Configuration (Bottom View)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	N/C	N/C	OUTB-	INB-	**V_{CC}**	N/C	N/C	**GND**	OUTA-	INA-	N/C	N/C	**GND**	OUTD-	IND-	**V_{CC}**	N/C	N/C	OUTC-	INC-
B	N/C	N/C	OUTB+	INB+	**V_{CC}**	N/C	N/C	**GND**	OUTA+	INA+	N/C	N/C	**GND**	OUTD+	IND+	**V_{CC}**	N/C	N/C	OUTC+	INC+
C	TDO	N/C	RXRATE	TXRATE	**V_{CC}**	**GND**	**GND**	**GND**	BOE[1]	BOE[3]	BOE[5]	BOE[7]	**GND**	SDASEL	PARCTL	**V_{CC}**	LPENB	LPENC	TMS	TDI
D	N/C	N/C	RXLE	N/C	**V_{CC}**	**GND**	**GND**	**GND**	BOE[0]	BOE[2]	BOE[4]	BOE[6]	**GND**	SPDSEL	RFMODE	**V_{CC}**	LPENA	LPEND	TRSTZ	TCLK
E	**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**
F	RXDB[1]	RXOPB	RXDB[0]	BISTLE													N/C	TXDC[0]	TXOPC	TXPERC
G	RXDB[3]	FRAMCHAR	OELE	GND													TXDC[1]	TXDC[4]	TXCKSEL	TXDC[7]
H	GND	GND	GND	GND													GND	GND	GND	GND
J	RXDB[4]	RXDB[7]	RXDB[2]	COMDETB													TXDC[3]	TXDC[2]	TXDC[5]	TXDC[9]
K	RXCLKB+	RXDB[9]	RXDB[6]	RXDB[5]													LFIC	TXDC[8]	RXCLKC-	RXDC[4]
L	TXDB[6]	RXCLKB-	LFIB	RXDB[8]													TXDC[6]	TXCLKC	RXCLKC+	RXDC[5]
M	TXCLKB	TXDB[7]	TXDB[8]	TXDB[9]													RXDC[8]	RXDC[9]	RXDC[7]	RXDC[6]
N	GND	GND	GND	GND													GND	GND	GND	GND
P	TXDB[2]	TXDB[3]	TXDB[4]	TXDB[5]													RXDC[0]	RXDC[1]	RXDC[2]	RXDC[3]
R	TXPERB	TXOPB	TXDB[0]	TXDB[1]													TXOPD	TXPERD	RXOPC	COMDETC
T	**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**
U	RXDA[0]	COMDETA	RXOPA	RXDA[4]	**V_{CC}**	TXDA[8]	TXDA[4]	**GND**	TXDA[1]	REFCLK-	RFENC	RXOPD	**GND**	RXDD[3]	RXDD[4]	**V_{CC}**	TXDD[9]	TXDD[2]	TXDD[1]	TXDD[0]
V	RXDA[1]	RXDA[2]	RXDA[5]	RXDA[9]	**V_{CC}**	TXDA[7]	TXDA[3]	**GND**	RFENB	REFCLK+	RFEND	COMDETD	**GND**	RXDD[1]	RXDD[5]	**V_{CC}**	RXDD[8]	TXDD[8]	TXDD[4]	TXDD[3]
W	RXDA[3]	RXDA[6]	RXCLKA–	LFIA	**V_{CC}**	TXDA[6]	TXDA[2]	**GND**	RFENA	TXOPA	TXRST	TXCLKO–	**GND**	RXDD[0]	RXDD[6]	**V_{CC}**	RXCLKD–	LFID	TXDD[7]	TXDD[5]
Y	RXDA[7]	RXDA[8]	RXCLKA+	TXDA[9]	**V_{CC}**	TXDA[5]	TXDA[0]	**GND**	TXPERA	TXCLKA	N/C	TXCLKO+	**GND**	RXDD[2]	RXDD[7]	**V_{CC}**	RXCLKD+	RXDD[9]	TXCLKD	TXDD[6]

Pin Descriptions CYP(V)15G0402DXB Quad HOTLink II™ SERDES

Name	I/O Characteristics	Signal Description
Transmit Path Data Signals		
TXPERA TXPERB TXPERC TXPERD	LVTTL1 Output, changes relative to REFCLK↑[2]	**Transmit Path Parity Error**. Active HIGH. Asserted (HIGH) if parity checking is enabled and a parity error is detected at the shifter. This output is HIGH for one transmit character clock period to indicate detection of a parity error in the character presented to the shifter. If a parity error is detected, the character in error is replaced with a +C0.7 character to force a corresponding bad-character detection at the remote end of the link. This replacement takes place only when parity checking is enabled (PARCTL ≠ LOW). When BIST is enabled for the specific transmit channel, BIST progress is presented on these outputs. Once every 511 character times (plus a 16-character Word Sync Sequence when the receive channels are clocked by a common clock, i.e., RXCKSEL = LOW or HIGH), the associated TXPERx signal will pulse HIGH for one transmit-character clock period (if RXCKSEL= MID) or seventeen transmit- character clock periods (if RXCKSEL = LOW or HIGH) to indicate a complete pass through the BIST sequence. For RXCKSEL = LOW or HIGH, If TXMODE[1:0] = LL, then no word sync sequence is sent in BIST. Therefore, in this case TXPERx signal will pulse HIGH for one transmit-character clock period. These outputs also provide indication of a transmit Phase-Align Buffer underflow or overflow. When the transmit Phase-Align Buffers are enabled (TXCKSEL ≠ LOW, or TXCKSEL = LOW and TXRATE = HIGH), if an underflow or overflow condition is detected, TXPERx for the channel in error is asserted and remains asserted until either an atomic Word Sync Sequence is transmitted or $\overline{\text{TXRST}}$ is sampled LOW to re-center the transmit Phase-Align Buffers.
TXDA[9:0] TXDB[9:0] TXDC[9:0] TXDD[9:0]	LVTTL Input, synchronous, sampled by the respective TXCLKx↑ or REFCLK↑[2]	**Transmit Data Inputs**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL and passed to the transmit shifter. TXDx[9:0] specify the specific transmission character to be sent.
TXOPA TXOPB TXOPC TXOPD	LVTTL Input, synchronous, sampled by the respective TXCLKx↑ or REFCLK↑[2]	**Transmit Path Odd Parity**. When parity checking is enabled (PARCTL ≠ LOW), the ODD parity captured at these inputs is XORed with the bits on the associated TXDx bus to verify the integrity of the captured character.
Transmit Path Clock and Control		
TXCLKO±	LVTTL Output	**Transmit Clock Output**. This true and complement clock is synthesized by the transmit PLL and operates synchronous to the internal transmit character clock. It operates at either the same frequency as REFCLK(when TXRATE = LOW), or at twice the frequency of REFCLK (when TXRATE = HIGH). This output clock has no direct phase relationship to REFCLK or any recovered character clock.
TXCKSEL	Three-level Select[3] Static Control Input	**Transmit Clock Select**. Selects the clock source used to write data into the transmit Input Register of the transmit channel(s) When LOW, all four input registers are clocked by REFCLK↑. When TXCKSEL is MID, TXCLKx↑ is used as the input register clock for the associated TXDx[9:0] and TXOPx. When HIGH, TXCLKA↑ is used to clock data into the Input Register for all channels.
TXCLKA TXCLKB TXCLKC TXCLKD	LVTTL Clock Input asynchronous, internal pull-up	**Transmit Path Input Clocks**. These inputs are only used when TXCKSEL ≠ LOW. These clocks must be frequency-coherent to TXCLKO±, but may be offset in phase. The internal operating phase of each input clock (relative to REFLCK or TXCLKO±) is adjusted when $\overline{\text{TXRST}}$ = LOW and locked when $\overline{\text{TXRST}}$ = HIGH.

Note:
2. When REFCLK is configured for half-rate operation (TXRATE = HIGH), these inputs are sampled (or the outputs change) relative to both the rising and falling edges of REFCLK

Pin Descriptions CYP(V)15G0402DXB Quad HOTLink II™ SERDES (continued)

Name	I/O Characteristics	Signal Description
TXRATE	LVTTL Input, asynchronous, internal pull-up	**Transmit PLL Clock Rate Select**. When TXRATE = HIGH, the Transmit PLL multiplies REFCLK by 20 to generate the serial bit-rate clock. When TXRATE = LOW, the transmit PLL multiples REFCLK by 10 to generate the serial bit-rate clock. See *Table 3* for a list of operating serial rates. When REFCLK is selected for clocking of the receive parallel interfaces, the TXRATE input also determines if the clock on the RXCLKA± and RXCLKC± outputs is a full or half-rate clock. When TXRATE = HIGH, these clocks are half-rate clocks and follow the frequency and duty cycle of the REFCLK input. When TXRATE = LOW, these output clocks are full-rate clocks and follow the frequency and duty cycle of the REFCLK input.
$\overline{\text{TXRST}}$	LVTTL Input, asynchronous, internal pull-up, sampled by TXCLKA↑ or REFCLK↑ [2]	**Transmit Clock Phase Reset**. Active LOW. When sampled LOW the transmit Phase-Align Buffers are allowed to adjust their data-transfer timing (relative to the selected input clock) to allow clean transfer of data from the Input Register to the Transmit Shifter. When $\overline{\text{TXRST}}$ is sampled deasserted (HIGH), the internal phase relationship between the associated TXCLKx and the internal character-rate clock is fixed and the device operates normally. When configured for half-rate REFCLK sampling of the transmit character stream (TXCKSEL = LOW and TXRATE = HIGH), assertion of $\overline{\text{TXRST}}$ is only used to clear phase align buffer faults caused by highly asymmetric REFCLK periods or REFCLKs with excessive cycle-to-cycle jitter. During this alignment period, one or more characters may be added to or lost from all the associated transmit paths as the transmit Phase-Align Buffers are adjusted. $\overline{\text{TXRST}}$ must be sampled LOW by a minimum of two consecutive rising edges of TXCLKA (or one REFCLK↑) to ensure the reset operation is initiated correctly on all channels. This input is ignored when both TXCKSEL and TXRATE are LOW. In all other configurations, TXRST should be asserted during device initialization to ensure proper operation of the Phase-Align Buffers.
Receive Path Data Signals		
RXDA[9:0] RXDB[9:0] RXDC[9:0] RXDD[9:0]	LVTTL Output, synchronous to the selected RXCLKx↑ output or REFCLK↑ [2] input	**Receive Data Output**. These outputs change following the rising edge of the selected receive interface clock.
COMDETA COMDETB COMDETC COMDETD	LVTTL Output, synchronous to the selected RXCLKx↑ output or REFCLK↑ [2] input	**Frame Character Detected**. COMDETx = HIGH indicates the presence of a Framing character in that Output Register.
RXOPA RXOPB RXOPC RXOPD	Three-state, LVTTL Output, synchronous to the selected RXCLKx↑ output or REFCLK↑ [2] input	**Receive Path Odd Parity**. When parity generation is enabled (PARCTL ≠ LOW), the parity output at these pins is valid for the data on the associated RXDx bus bits. When parity generation is disabled (PARCTL = LOW) these output drivers are disabled (High-Z).
Receive Path Clock and Clock Control		
RFENA RFENB RFENC RFEND	LVTTL Input, asynchronous, internal pull-down	**Reframe Enable**. Active HIGH. When HIGH the framer for the associated channel is enabled to frame as per the presently enabled framing mode and selected framing character.

Note:

3. Three-level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC}. When not connected or allowed to float, a three-level select input will self-bias to the MID level.

Pin Descriptions CYP(V)15G0402DXB Quad HOTLink II™ SERDES (continued)

Name	I/O Characteristics	Signal Description
RXRATE	LVTTL Input Static Control Input	**Receive Clock Rate Select**. When LOW, the RXCLKx± recovered clock outputs are complementary clocks operating at the recovered character rate. Data for the associated receive channels should be latched on the rising edge of RXCLKx+ or falling edge of RXCLKx–. When HIGH, the RXCLKx± recovered clock outputs are complementary clocks operating at half the character rate. Data for the associated receive channels should be latched alternately on the rising edge of RXCLKx+ and RXCLKx–.
FRAMCHAR	Three-level Select [3] Static Control Input	**Framing Character Select**. Used to control the type of character used for framing the received data streams. When MID, the framer looks for both positive and negative disparity versions of the eight-bit Comma character. When HIGH, the framer looks for both positive and negative disparity versions of the K28.5 character. The LOW configuration is reserved for component test.
RXCLKA± RXCLKB± RXCLKC± RXCLKD±	LVTTL Output Clock	**Receive Character Clock Output**. These true and complement clocks are the Receive interface clocks which are used to control timing of data output transfers. These clocks are output continuously at either the dual-character rate (1/20th the serial bit-rate) or character rate (1/10th the serial bit-rate) of the data being received, as selected by RXRATE.
RFMODE	Three-level Select[3] Static Control Input	**Reframe Mode Select**. Used to control the type of character framing used to adjust the character boundaries (based on detection of one or more framing characters in the received serial bit stream). This signal operates in conjunction with the type of framing character selected. When LOW, the Low-Latency Framer is selected. This will frame on each occurrence of the selected framing character(s) in the received data stream. This mode of framing stretches the recovered clock for one or multiple cycles to align that clock with the recovered data. When MID, the Cypress-mode Multi-Byte parallel Framer is selected. This requires a pair of the selected framing character(s), on identical 10-bit boundaries, within a span of 50 bits, before the character boundaries are adjusted. The recovered character clock remains in the same phasing regardless of character offset. When HIGH, the alternate mode Multi-Byte parallel Framer is selected. This requires detection of the selected framing character(s) of the allowed disparities in the received serial bit stream, on identical 10-bit boundaries, on four directly adjacent characters. The recovered character clock remains in the same phasing regardless of character offset.
Device Control Signals		
PARCTL	Three-level Select[3], Static Control Input	**Parity Check/Generate Control**. Used to control the different parity check and generate functions. When LOW, parity checking is disabled, and the RXOPx outputs are all disabled (High-Z). When MID, theTXDx[9:0] inputs are checked (along with TXOPx) for valid ODD parity, and ODD parity is generated for the RXDx[9:0] outputs and presented on RXOPx. When HIGH, parity checking and generation are enabled. The TXDx[9:0] inputs are checked (along with TXOPx) for valid ODD parity, and ODD parity is generated for the RXDx[9:0] and COMDETx outputs and presented on RXOPx.
REFCLK±	Differential LVPECL or single-ended LVCMOS input clock	**Reference Clock**. This clock input is used as the timing reference for the transmit and receive PLLs. This input clock may also be selected to clock the transmit and receive parallel interfaces. When driven by a a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement REFCLK input and leave the alternate REFCLK input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs. When TXCKSEL = LOW, REFCLK is also used as the clock for the parallel transmit data (input) interface.

Pin Descriptions CYP(V)15G0402DXB Quad HOTLink II™ SERDES (continued)

Name	I/O Characteristics	Signal Description
SPDSEL	Three-level Select[3], Static Control Input	**Serial Rate Select**. This input specifies the operating bit-rate range of both transmit and receive PLLs. LOW = 195–400 MBd, MID = 400–800 MBd, HIGH = 800–1500 MBd.
Analog I/O and Control		
OUTA± OUTB± OUTC± OUTD±	CML Differential Output	**Differential Serial Data Outputs. These** PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules. These outputs must be AC-coupled for PECL-compatible connections.
INA± INB± INC± IND±	LVPECL Differential Input	**Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization. The INx± serial streams are passed to the receiver Clock and Data Recovery (CDR) circuits to extract the data content when INSELx = HIGH.
OELE	LVTTL Input, asynchronous, internal pull-up	**Serial Driver Output Enable Latch Enable**. When OELE = HIGH, the signals on the BOE[7:0] inputs directly control the OUTx± differential drivers. When the BOE[x] input is HIGH, the associated OUTx± differential driver is enabled. When the BOE[x] input is LOW, the associated OUTx± differential driver is powered down. When OELE returns LOW, the last values present on BOE[7:0] are captured in the internal Output enable Latch. The specific mapping of BOE[7:0] signals to transmit output enables is listed in *Table 2*. If the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable all outputs.
BISTLE	LVTTL Input, asynchronous, internal pull-up	**Transmit and Receive BIST Latch Enable**. Active HIGH. When BISTLE = HIGH, the signals on the BOE[7:0] inputs directly control the transmit and receive BIST enables. When the BOE[x] input is LOW, the associated transmit or receive channel is configured to generate or compare the BIST sequence. When the BOE[x] input is HIGH, the associated transmit or receive channel is configured for normal data transmission or reception. When BISTLE returns LOW the last values present on BOE[7:0] are captured in the internal BIST Enable Latch. The specific mapping of BOE[7:0] signals to transmit and receive BIST enables is listed in *Table 2*. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable BIST on all transmit and receive channels.
RXLE	LVTTL Input, asynchronous, internal pull-up	**Receive Channel Power-Control Latch Enable**. When RXLE = HIGH, the signals on the BOE[7:0] directly control the power enables for the receive PLLs and analog logic. When the BOE[7:0] input is HIGH, the all receive channels PLL's and analog logic are active. When the BOE[7:0] input is LOW, the receive channels are in a power-down mode. When RXLE returns LOW, the last values present on BOE[7:0] are captured in the internal RX PLL Enable Latch. The specific mapping of BOE[7:0] signals to the associated receive channel enables is listed in *Table 2*. When the device is reset ($\overline{\text{TRSTZ}}$ = LOW), the latch is reset to disable all receive channels.
BOE[7:0]	LVTTL Input, asynchronous, internal pull-up	**BIST, Serial Output, and Receive Channel Enables**. These inputs are passed to and through the Output Enable Latch when OELE is HIGH, and captured in this latch when OELE returns LOW. These inputs are passed to and through the BIST Enable Latch when BISTLE is HIGH, and captured in this latch when BISTLE returns LOW. These inputs are passed to and through the Receive Channel Enable Latch when RXLE is HIGH, and captured in this latch when RXLE returns LOW.
SDASEL	Three-level Select[3], static configuration input	**Signal Detect Amplitude Level Select**. Allows selection of one of three predefined amplitude trip points for a valid signal indication, as listed in *Table 4*.

Pin Descriptions CYP(V)15G0402DXB Quad HOTLink II™ SERDES (continued)

Name	I/O Characteristics	Signal Description
LPENA LPENB LPENC LPEND	LVTTL Input, asynchronous, internal pull-down	**Loop-Back-Enable**. Active HIGH. When asserted (HIGH), the transmit serial data from the associated channel is internally routed to its respective receiver clock and data recovery (CDR) circuit. The serial output for the channel where LPENx is active is forced to differential logic "1", and serial data inputs for that channel are ignored.
$\overline{\text{LFIA}}$ $\overline{\text{LFIB}}$ $\overline{\text{LFIC}}$ $\overline{\text{LFID}}$	LVTTL Output, synchronous to the selected RXCLKx↑ output or REFCLK↑[2] input, asynchronous to Receive channel enable/disable	**Link Fault Indication Output**. Active LOW. $\overline{\text{LFIx}}$ is the logical OR of four internal conditions: 1. Received serial data frequency outside expected range 2. Analog amplitude below expected levels 3. Transition density lower than expected 4. Receive Channel disabled.
$\overline{\text{TRSTZ}}$	LVCMOS Input, internal pull-up	**Device Reset**. Active LOW. Initializes all state machines and counters in the device. When sampled LOW by the rising edge of REFLCK, this input resets the internal state machines and sets the Elasticity Buffer pointers to a nominal offset. When the reset is removed ($\overline{\text{TRSTZ}}$ sampled HIGH by REFCLK↑), the status and data outputs will become deterministic in less than 16 REFCLK cycles. The BISTLE, OELE, and RXLE latches are reset by $\overline{\text{TRSTZ}}$. If the Elasticity Buffer or the Phase Align Buffer are used, $\overline{\text{TRSTZ}}$ should be applied after power up to initialize the internal pointers into these memory arrays.
JTAG Interface		
TMS	LVTTL Input, internal pull-up	**Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained high for ≥5 TCLK cycles, the JTAG test controller is reset. The TAP controller is also reset automatically upon application of power to the device.
TCLK	LVTTL Input, internal pull-down	**JTAG Test Clock**
TDO	Three-state LVTTL Output	**Test Data Out**. JTAG data output buffer which is High-Z while JTAG test mode is not selected.
TDI	LVTTL Input, internal pull-up	**Test Data In**. JTAG data input port.
Power		
V_{CC}		**+3.3V Power**
GND		**Signal and Power Ground for all internal circuits**.

CYP(V)15G0402DXB HOTLink II SERDES Operation

The CYP(V)15G0402DXB is a highly configurable device designed to support reliable transfer of large quantities of data, using high-speed serial links from one or multiple sources to multiple destinations. This device supports four character-wide channels.

CYP(V)15G0402DXB Transmit Data Path

Data Path

The transmit path of the CYP(V)15G0402DXB supports four character-wide data paths. These four data paths are internally unencoded and require input data that is encoded for reliable transport.

Input Register

The bits in the Input Register for each channel have fixed bit assignments, as listed in *Table 1*.

Table 1. Input Register Bit Mapping

Signal Name	Bus Weight	10B Name
TXDx[0] (LSB)	2^0	a[4]
TXDx[1]	2^1	b
TXDx[2]	2^2	c
TXDx[3]	2^3	d
TXDx[4]	2^4	e
TXDx[5]	2^5	i
TXDx[6]	2^6	f
TXDx[7]	2^7	g
TXDx[8]	2^8	h
TXDx[9] (MSB)	2^9	j
TXOPx[5]		

Notes:
4. LSB is shifted out first.
5. The TXOPx inputs are also captured in the associated Input Register, but their interpretation is under the separate control of PARCTL.

Each input register captures a minimum of 10 bits on each input clock cycle. When parity checking is enabled, the TXOPx parity input is also captured in the associated input register.

Input Register Clocking

The transmit Input Registers can be configured to accept data relative to different clock sources. The selection of the clock source is controlled by TXCKSEL.

When TXCKSEL = LOW, the Input Registers for all four transmit channels are clocked by REFCLK↑[2]. When TXCKSEL = HIGH, the Input Registers for all four transmit channels are clocked with TXCLKA↑.

When TXCKSEL is MID, TXCLKx↑ is used as the input register clock for the associated TXDx[9:0] and TXOPx.

Phase-Align Buffer

Data from the Input Registers is normally routed to the associated Phase-Align Buffer. When the transmit paths are operated synchronous to REFCLK↑ (TXCKSEL = LOW and TXRATE = LOW), the Phase-Align Buffers are bypassed and data is passed directly to the Parity Check and Serializer blocks to reduce latency.

When an Input-Register clock with an uncontrolled phase relationship to REFCLK is selected (TXCKSEL ≠ LOW) or if data is captured on both edges of REFCLK (TXRATE = HIGH), the Phase-Align Buffers are enabled. These buffers are used to absorb clock phase differences between the presently selected input clock and the internal character clock.

Initialization of these Phase-Align Buffers takes place when the $\overline{\text{TXRST}}$ input is sampled LOW by TXCLKA↑. When $\overline{\text{TXRST}}$ is returned HIGH, the present input clock phase relative to REFCLK is set. $\overline{\text{TXRST}}$ is an asynchronous input, but is sampled internally to synchronize it to the internal transmit path state machines. $\overline{\text{TXRST}}$ must be sampled LOW by a minimum of two consecutive TXCLKA↑ clocks to ensure the reset operation is initiated correctly on all channels.

Once set, the input clocks are allowed to skew in time up to half a character period in either direction relative to REFCLK; i.e., ±180°. This time shift allows the delay paths of the character clocks (relative to REFCLK) to change due to operating voltage and temperature, while not affecting the design operation.

If the phase offset, between the initialized location of the input clock and REFCLK↑, exceeds the skew handling capabilities of the Phase-Align Buffer, an error is reported on the associated TXPERx output. This output indicates a continuous error until the Phase-Align Buffer is reset. While the error remains active, the transmitter for the associated channel will output a continuous C0.7 character to indicate to the remote receiver that an error condition is present in the link.

Parity Support

In addition to the ten data bits that are captured at each channel, a TXOPx input is also available on each channel. This allows the CYP(V)15G0402DXB to support ODD parity checking for each channel. When PARCTL = LOW, parity checking is disabled. When PARCTL = MID or HIGH, parity is checked on the TXDx[9:0] and TXOPx bits.

If parity checking is enabled (PARCTL ≠ LOW) and a parity error is detected, the 10-bit character in error is replaced with the 1001111000 pattern (an invalid character) regardless of the running disparity of the previous character.

Transmit BIST

The transmitter interfaces contain internal pattern generators that can be used to validate both device and link operation. These generators are enabled by the associated BOE[x] signals listed in *Table 2* (when the BISTLE latch enable input is HIGH). When enabled, a register in the associated transmit channel becomes a signature pattern generator by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to identical LFSR in the attached Receiver(s).

When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator in the associated transmit channel (or the BIST checker in the associated receive channel). When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned HIGH to open the latch. A device reset ($\overline{\text{TRSTZ}}$ sampled LOW) presets the BIST Enable Latch to disable BIST on all channels.

All data and data-control information present at the associated TXDx[9:0] inputs are ignored when BIST is active on that channel.

Table 2. Output Enable, BIST, and Receive Channel Enable Signal Map

BOE Input	Output Controlled (OELE)	BIST Channel Enable (BISTLE)	Receive PLL Channel Enable (RXLE)
BOE[7]	X	Transmit D	X
BOE[6]	OUTD±	Receive D	Receive D
BOE[5]	X	Transmit C	X
BOE[4]	OUTC±	Receive C	Receive C
BOE[3]	X	Transmit B	X
BOE[2]	OUTB±	Receive B	Receive B
BOE[1]	X	Transmit A	X
BOE[0]	OUTA±	Receive A	Receive A

Serial Output Drivers

The serial interface Output Drivers use differential CML (Current Mode Logic) to provide a source-matched driver for the transmission lines. These drivers accept data from the Transmit Shifters. These outputs have signal swings equivalent to that of standard PECL drivers and are capable of driving AC-coupled optical modules or transmission lines.

When configured for local loopback (LPENx = HIGH), the output drivers for all enabled ports are configured to drive a static differential logic-1.

Each output can be enabled or disabled separately through the BOE[7:0] inputs, as controlled by the OELE latch-enable signal. When OELE is HIGH, the signals present on the BOE[7:0] inputs are passed through the Serial Output Enable Latch to control the Serial Output Drivers. The BOE[7:0] input associated with a specific OUTx± driver is listed in *Table 2*.

When OELE is HIGH and BOE[x] is HIGH, the associated Serial Driver is enabled. When OELE is HIGH and BOE[x] is LOW, the associated driver is disabled and internally powered down, the associated internal logic for that channel is also powered down. When OELE returns LOW, the values present on the BOE[7:0] inputs are latched in the Output Enable Latch, and remain there until OELE returns HIGH to enable the latch. A device reset (TRSTZ sampled LOW) clears this latch and disables all output drivers.[6]

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the REFCLK input, and multiples that clock by 10 or 20 (as selected by TXRATE) to generate a bit-rate clock for use by the Transmit Shifter. It also provides a character-rate clock used by the transmit paths.

The clock multiplier PLL can accept a REFCLK input between 19.5 MHz and 150 MHz, however, this clock range is limited by the operating mode of the CYP(V)15G0402DXB clock multiplier (controlled by TXRATE) and by the level on the SPDSEL input.

SPDSEL is a three-level select[3] (ternary) input that selects one of three operating ranges for the serial data outputs and inputs. The operating serial signalling-rate and allowable range of REFCLK frequencies is listed in *Table 3*.

Table 3. Operating Speed Settings

SPDSEL	TXRATE	REFCLK Frequency (MHz)	Signaling Rate (MBaud)
LOW	1	reserved	195-400
	0	19.5–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500
	0	80–150	

The REFCLK± input is a differential input with each input internally biased to 1.4V. If the REFCLK+ input is connected to a TTL, LVTTL, or LVCMOS clock source, the input signal is recognized when it passes through the internally biased reference point.

When both the REFCLK+ and REFCLK– inputs are connected, the clock source must be a differential clock. This can be either a differential LVPECL clock that is DC- or AC-coupled, or a differential LVTTL or LVCMOS clock.

By connecting the REFCLK– input to an external voltage source or resistive voltage divider, it is possible to adjust the reference point of the REFCLK+ input for alternate logic levels. When doing so it is necessary to ensure that the input differential crossing point remains within the parametric range supported by the input.

CYP(V)15G0402DXB Receive Data Path

Serial Line Receivers

A differential line receiver, INx±, is available on each channel for accepting a serial bit stream. The Serial Line Receiver inputs are differential, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB. For normal operation, these inputs should receive a signal of at least VI_{DIFF} > 100 mV, or 200 mV peak-to-peak differential. Each Line Receiver can be DC- or AC-coupled to +3.3V powered fiber-optic interface modules (any ECL/PECL family, not limited to 100K PECL) or AC-coupled to +5V powered optical modules. The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages. Each receiver provides internal DC-restoration, to the center of the receiver's common mode range, for AC-coupled signals.

The local loopback inputs (LPENx) for each channel allows the serial transmit data outputs to be routed internally back to the Clock and Data Recovery circuit associated with that channel. When configured for local loopback, all transmit Serial Driver outputs are forced to output a differential logic-1. This prevents local diagnostic patterns from being broadcast to attached remote receivers.

Signal Detect/ Link Fault

Each selected Line Receiver (i.e., that routed to the clock and data recovery PLL) is simultaneously monitored for

- analog amplitude
- transition density
- CDR tracking data within expected frequency range as defined by REFCLK and TXRATE.
- receive channel enabled

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the LFIx (Link Fault Indicator) output associated with each receive channel, which changes synchronous to the selected receive interface clock.

Table 4. Analog Amplitude Detect Valid Signal Levels

SDASEL	Typical Signal with Peak Amplitudes Above
LOW	140 mV p-p differential
MID (Open)	280 mV p-p differential
HIGH	420 mV p-p differential

Analog Amplitude

While most signal monitors are based on fixed constants, the analog amplitude level detection is adjustable. This allows operation with highly attenuated signals, or in high-noise environments. This adjustment is made through the SDASEL signal, a three-level select[3] input, which sets the trip point for the detection of a valid signal at one of three levels, as listed in *Table 4*. This control input affects the analog monitors for all receive channels.

When a particular channel is configured for local loopback (LPENx = HIGH), no line receivers are selected, and the LFIx output for each channel reports only the receive VCO frequency out-of-range and transition density status of the associated transmit signal. When local loopback is active, the Analog Signal Detect Monitors are disabled.

Note:

6. When a disabled transmit channel (i.e., both outputs disabled) is reenabled, the data on the serial outputs may not meet all timing specifications for up to 10 ms.

Transition Density

The Transition Detection logic checks for the absence of any transitions spanning greater than six transmission characters (60 bits). If no transitions are present in the data received on a channel, the Transition Detection logic for that channel will assert LFIx. The LFIx output remains asserted until at least one transition is detected in each of three adjacent received characters.

Range Controls

The Clock/Data Recovery (CDR) circuit includes logic to monitor the frequency of the Phase Locked Loop (PLL) Voltage Controlled Oscillator (VCO) used to sample the incoming data stream. This logic ensures that the VCO operates at, or near the rate of the incoming data stream for two primary cases:

- when the incoming data stream resumes after a time in which it has been "missing"
- when the incoming data stream is outside the acceptable frequency range

To perform this function, the frequency of the VCO is periodically sampled and compared to the frequency of the REFCLK input. If the VCO is running at a frequency beyond ±400ppm as defined by the refclock frequency, it is periodically forced to the correct frequency (as defined by REFCLK, SPDSEL, and TXRATE) and then released in an attempt to lock to the input data stream. The sampling and relock period of the Range Control is calculated as follows: RANGE CONTROL SAMPLING PERIOD = (REFCLKPERIOD) * (16000).

During the time that the Range Control forces the PLL VCO to run at the REFCLK*N rate, the LFIx output will be asserted LOW. While the PLL is attempting to re-lock to the incoming data stream, LFIx may be either HIGH or LOW (depending on other factors such as transition density and amplitude detection) and the recovered byte clock (RCXCLKx) may run at an incorrect rate (depending on the quality or existence of the input serial data stream). After a valid serial data stream is applied, it may take up to one RANGE CONTROL SAMPLING PERIOD before the PLL locks to the input data stream, after which LFIx should be HIGH.

Receive Channel Enabled

The CYP(V)15G0402DXB contains four receive channels that can be independently enabled and disabled. Each channel can be enabled or disabled separately through the BOE[7:0] inputs, as controlled by the RXLE latch-enable signal. When RXLE is HIGH, the signals present on the BOE[7:0] inputs are passed through the Receive Channel Enable Latch to control the PLLs and logic of the associated receive channel. The BOE[7:0] input associated with a specific receive channel is listed in *Table 2*.

When RXLE is HIGH and BOE[x] is HIGH, the associated receive channel is enabled to receive and decode a serial stream. When RXLE is HIGH and BOE[x] is LOW, the associated receive channel is disabled and powered down. Any disabled channel will indicate an asserted LFIx output. When RXLE returns LOW, the values present on the BOE[7:0] inputs are latched in the Receive Channel Enable Latch, and remain there until RXLE returns HIGH to opened the latch again.[8]

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from each received serial stream is performed by a separate Clock/Data Recovery (CDR) block within each receive channel. The clock extraction function is performed by embedded phase-locked loops (PLLs) that track the frequency of the transitions in the incoming bit streams and align the phase of their internal bit-rate clocks to the transitions in the selected serial data streams.

Each CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit-rate ÷ 20) reference clock from the REFCLK input. This REFCLK input is used to

- ensure that the VCO (within the CDR) is operating at the correct frequency. (rather than a harmonic of the bit-rate)
- to reduce PLL acquisition time
- and to limit unlocked frequency excursions of the VCO when there is no input data present at the selected Serial Line Receiver.

Regardless of the type of signal present, the CDR will attempt to recover a data stream from it. If the frequency of the recovered data stream is outside the limits set by the range control monitors, the CDR will switch to track REFCLK instead of the data stream. Once the CDR output (RXCLKx) frequency returns back close to REFCLK frequency, the CDR input will be switched back to the input data stream to check its frequency. In case no data is present at the input this switching behavior may result in brief RXCLKx frequency excursions from REFCLK. However, the validity of the input data stream is indicated by the LFIx output. The frequency of REFCLK is required to be within ±200 ppm of the frequency of the clock that drives the REFCLK input of the *remote* transmitter to ensure a lock to the incoming data stream.

Deserializer/Framer

Each CDR circuit extracts bits from the associated serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream looking for one or more Comma or K28.5 characters at all possible bit positions. The location of this character in the data stream is used to determine the character boundaries of all following characters.

Framing Character

The CYP(V)15G0402DXB allows selection of one of two combinations of framing characters to support requirements of different interfaces. The selection of the framing character is made through the FRAMCHAR input.

Notes:

7. The standard definition of a Comma contains only seven bits. However, since all valid Comma characters within the 8B/10B character set also have the eighth bit as an inversion of the seventh bit, the compare pattern is extended to a full eight bits to reduce the possibility of a framing error.
8. When a disabled receive channel is reenabled, the status of the associated LFIx output and data on the parallel outputs for the associated channel may be indeterminate for up to 10 ms.

Table 5. Framing Character Selector

FRAMCHAR	Bits Detected in Framer	
	Character Name	Bits Detected
MID (Open)	Comma+ or Comma-	00111110XX[7] or 11000001XX
HIGH	+K28.5 or -K28.5	0011111010 or 1100000101

The specific bit combinations of these framing characters are listed in *Table 5*. When the specific bit combination of the selected framing character is detected by the Framer, the boundaries of the characters present in the received data stream are known.

Framer

The Framer on each channel operates in one of three different modes, as selected by the RFMODE input. In addition, the Framer for each channel may be enabled or disabled through the RFENx input. When RFENx = LOW, the framer in that receive path is disabled, and no combination of bits in a received data stream will alter the character boundaries. When RFENx = HIGH, the Framer selected by RFMODE is enabled for that channel.

When RFMODE = LOW, the Low-Latency Framer is selected. This Framer operates by stretching the recovered character clock until it aligns with the received character boundaries. In this mode the Framer starts its alignment process on the first detection of the selected framing character. To reduce the impact on external circuits that make use of a recovered clock, the clock period is not stretched by more than two bit-periods in any one clock cycle. When operated in with a character-rate output clock (RXRATE = LOW), the output of properly framed characters may be delayed by up to nine character-clock cycles from the detection of the selected framing character. When operated with a half-character-rate output clock (RXRATE = HIGH), the output of properly framed characters may be delayed by up to 14 character-clock cycles from the detection of the selected framing character.[8]

When RFMODE is MID (open) the Cypress-mode Multi-Byte Framer is selected. The required detection of multiple framing characters makes the associated link much more robust to incorrect framing due to aliased SYNC characters in the data stream. In this mode, the Framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. This ensures that the recovered clock will not contain any significant phase changes or hops during normal operation or framing, and allows the recovered clock to be replicated and distributed to other external circuits or components using PLL-based clock distribution elements. In this framing mode the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

When RFMODE = HIGH, the Alternate-mode Multi-Byte Framer is enabled. Like the Cypress-mode Multi-Byte Framer, multiple framing characters must be detected before the character boundary is adjusted. In this mode, the data stream must contain a minimum of four of the selected framing characters, received as consecutive characters, on identical 10-bit boundaries, before character framing is adjusted.

Framing is enabled for a channel when the associated RFENx input is HIGH. When RFENx is LOW, the framer for the associated channel is disabled. When a framer is disabled, no changes are made to the recovered character boundaries on that channel, regardless of the presence of framing characters in the data stream.

Receive BIST Operation

The Receiver interfaces contain internal pattern generators that can be used to validate both device and link operation. These generators are enabled by the associated BOE[x] signals listed in *Table 2* (when the BISTLE latch enable input is HIGH). When enabled, a register in the associated receive channel becomes a pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter(s). When synchronized with the received data stream, the associated Receiver checks each character in the Decoder with each character generated by the LFSR and indicates compare errors and BIST status at the COMDETx and RXDx[1:0] bits of the Output Register.

When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator/checker in the associated Receive channel (or the BIST generator in the associated Transmit channel). When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned HIGH. All captured signals in the BIST Enable Latch are set HIGH (i.e., BIST is disabled) following a device reset ($\overline{\text{TRSTZ}}$ is switched LOW).

When BIST is first recognized as being enabled in the Receiver, the LFSR is preset to the BIST-loop start-code of D0.0. This code D0.0 is sent only once per BIST loop. The status of the BIST progress and any character mismatches is presented on the COMDETx and RXDx[1:0] status outputs.

Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. COMDETx, RXDOx[1:0] indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress. The specific status reported by the BIST state machine are listed in *Table 6*.

The specific patterns checked by each receiver are described in detail in the Cypress application note “HOTLink Built-In Self-Test.” The sequence compared by the CYP(V)15G0402DXB is identical to that in the CY7B933 and CY7C924DX, allowing interoperable systems to be built when used at compatible serial signaling rates.

Note:

9. When Receive BIST is enabled on a channel, the Low-Latency Framer must not be enabled. The BIST sequence contains an aliased K28.5 framing character, which causes the Receiver to update its character boundaries incorrectly.

If the number of invalid characters received ever exceeds the number of valid characters by 16, the receive BIST state machine aborts the compare operations and resets the LFSR to the D0.0 state to look for the start of the BIST sequence again.

The BIST state machine requires the characters to be correctly framed for it to detect the BIST sequence. If the Low Latency Framer is enabled (RFMODE = LOW), the Framer will misalign to an aliased SYNC character within the BIST sequence. If the Alternate Multi-Byte Framer is enabled (RFMODE = HIGH), it is generally necessary to frame the receiver before BIST is enabled.

Table 6. BIST Status Bits

Status			Priority	Description
COMDETx	RXDx[0]	RXDx[1]		BIST Mode
0	0	0	7	**BIST Data Compare**. Data Character compared correctly.
0	0	1	7	**BIST Command Compare**. Command Character compared correctly.
0	1	0	2	**BIST Last Good**. Last Character of BIST sequence detected and valid.
0	1	1	5	Reserved
1	0	0	4	**BIST Last Bad**. Last Character of BIST sequence was detected invalid.
1	0	1	1	**BIST Start**. RXBISTEN recognized on this channel, but character compares have not yet commenced. Also presented when the receive PLL is tracking REFCLK instead of the selected data stream.
1	1	0	6	**BIST Error**. While comparing characters, a mismatch was found in one or more of the decoded character bits.
1	1	1	3	**BIST Wait**. The receiver is comparing characters. but has not yet found the start of BIST character to enable the LFSR.

Power Control

The CYP(V)15G0402DXB supports user control of the powered up or down state of each transmit and receive channel. The receive channels are controlled by the RXLE signal and the values present on the BOE[7:0] bus. The transmit channels are controlled by the OELE signal and the values present on the BOE[7:0] bus. Powering down unused channels will save power and reduce system heat generation. Controlling system power dissipation will improve the system performance.

Receive Channels

When RXLE is HIGH, the signals on the BOE[7:0] inputs directly control the power enables for the receive PLLs and analog circuits. When a BOE[7:0] input is HIGH, the associated receive channel [A through D] PLL and analog logic are active. When a BOE[7:0] input is LOW, the associated receive channel [A through D] PLL and analog circuits are powered down. When RXLE returns LOW, the last values present on the BOE[7:0] inputs are captured. The specific BOE[7:0] input signal associated with a receive channel is listed in *Table 2*.

Any disabled receive channel will indicate a constant $\overline{\text{LFIx}}$ output.

When a disabled receive channel is re-enabled, the status of the associated $\overline{\text{LFIx}}$ output and data on the parallel outputs for the associated channel may be indeterminate for up to 10 ms.

Transmit Channels

When OELE is HIGH, the signals on the BOE[7:0] inputs directly control the power enables for the Serial Drivers. When a BOE[x] input is HIGH, the associated Serial Driver is enabled. When a BOE[x] input is LOW, the associated Serial Driver is disabled and powered down. If the Serial Drivers of a channel are disabled, the internal logic for that channel is powered down. When OELE returns LOW, the values present on the BOE[7:0] inputs are latched in the Output Enable Latch.

Device Reset State

When the CYP(V)15G0402DXB is reset by assertion of $\overline{\text{TRSTZ}}$, the Transmit Enable and Receive Enable Latches are both cleared, and the BIST Enable Latch is preset. In this state, all transmit and receive channels are disabled, and BIST is disabled on all channels.

Following a device reset, it is necessary to enable the transmit and receive channels used for normal operation. This can be done by sequencing the appropriate values on the BOE[7:0] inputs while the OELE and RXLE signals are raised and lowered. For systems that do not require dynamic control of power, or want the part to power up in a fixed configuration, it is also possible to strap the RXLE and OELE control signals HIGH to permanently enable their associated latches. Connection of the associated BOE[7:0] signals HIGH will then enable the respective transmit and receive channels as soon as the $\overline{\text{TRSTZ}}$ signal is deasserted.

Table 7. Output Register Bit Assignment

Signal Name	Bus Weight	10B Name
RXOPx[10]		
COMDET[10]		
RXDx[0] (LSB)	2^0	a
RXDx[1]	2^1	b
RXDx[2]	2^2	c
RXDx[3]	2^3	d
RXDx[4]	2^4	e
RXDx[5]	2^5	i
RXDx[6]	2^6	f
RXDx[7]	2^7	g
RXDx[8]	2^8	h
RXDx[9] (MSB)	2^9	j

Note:
10. The RXOPx and COMDETx outputs are also driven from the associated output register, but their generation and interpretation are separate from the data bus.

Output Bus

Each receive channel presents a 12-signal output bus consisting of:

- a 10-bit data bus
- a COMMA detect indicator
- a parity bit.

The signals present on this output bus are shown in *Table 7*.

The framed 10-bit value is presented to the associated Output Register, along with a status output indicating if the character in the output register matches the selected framing characters.

The COMDETx status outputs operate the same regardless of the bit combination selected for character framing by the FRAMCHAR input. They are HIGH when the character in the Output Register of the associated channel contains the selected framing character at the proper character boundary, and LOW for all other bit combinations.

When the Low-Latency Framer and half-rate receive port clocking are also enabled (RFMODE = LOW, RXRATE = HIGH), the Framer will stretch the recovered clock to the nearest 20-bit boundary such that the rising edge of RXCLKx+ occurs when COMDETx is present on the associated output bus.

When the Cypress or Alternate Mode Framer is enabled and half-rate receive port clocking are also enabled (RFMODE ≠ LOW and RXRATE = HIGH), the output clock is not modified when framing is detected, but a single pipeline stage may be added or subtracted from the data stream by the Framer logic such that the rising edge of RXCLKx+ occurs when COMDETx is present on the associated output bus.

This adjustment only occurs when the Framer is enabled (RFEN = HIGH). When the Framer is disabled, the clock boundaries are not adjusted, and COMDETx may be asserted during the rising edge of RXCLK– (if an odd number of characters were received following the initial framing).

Parity Generation

In addition to the 10 data and COMDETx status bit that are output on each channel, an RXOPx output is also available on that channel. This allows the CYP(V)15G0402DXB to supports ODD parity generation for each channel. To handle a wide range of system environments, the CYP(V)15G0402DXB supports two different forms of parity and no parity. Parity can be generated on

- the RXDx[9:0] character
- RXDx[9:0] character and COMDETx status bit.

These modes differ in the number bits which are included in the parity calculation. Only ODD parity is provided which ensures that at least one bit of the data bus is always a logic-1. Those bits covered by parity generation are listed in *Table 8*.

Parity generation is enabled through the three-level select PARCTL input. When PARCTL = LOW, parity checking is disabled, and the RXOPx outputs are all disabled (High-Z).

When PARCTL is MID, ODD parity is generated for the RXDx[9:0] bits.

When PARCTL is HIGH, ODD parity is generated for both the RXDx[9:0] bits and the associated COMDETx signal.

Table 8. Output Register Parity Generation

Signal Name	Receive Parity Generate Mode (PARCTL)		
	LOW[11]	MID	HIGH
COMDETx			X[12]
RXDx[0]		X	X
RXDx[1]		X	X
RXDx[2]		X	X
RXDx[3]		X	X
RXDx[4]		X	X
RXDx[5]		X	X
RXDx[6]		X	X
RXDx[7]		X	X
RXDx[8]		X	X
RXDx[9]		X	X

JTAG Support

The CYP(V)15G0402DXB contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, only boundary scan is supported. This capability is present only on the LVTTL inputs and outputs and REFCLK± input. The high-speed serial signals are not part of the JTAG test chain.

BIST Status State Machine

When a receive path is enabled to look for and compare the received data stream with the BIST pattern, the COMDETx and RXDx[1:0] bits identify the present state of the BIST compare operation.

The BIST state machine has multiple states, as shown in *Figure 2* and *Table 6*. When the receive PLL detects an out-of-lock condition, the BIST state is forced to the Start-of-BIST state, regardless of the present state of the BIST state machine. If the number of detected errors ever exceeds the number of valid matches by greater than 16, the state machine is forced to the WAIT_FOR_BIST state where it monitors the interface for the first character (D0.0) of the next BIST sequence. Also, if the Elasticity Buffer ever hits an overflow/underflow condition, the status is forced to the BIST_START until the buffer is re centered (approximately nine character periods).

JTAG ID

The JTAG device ID for the CYP(V)15G0402DXB is ‘1C801069’hex.

Three-level Select Inputs

Each three-level select input reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11, respectively.

Notes:

11. Receive path parity output drivers are disabled when PARCTL is low
12. When BIST is not enabled,COMDETx is usually driven to a logic 0, but will be driven high when the character in the output buffer is the selected framing character.

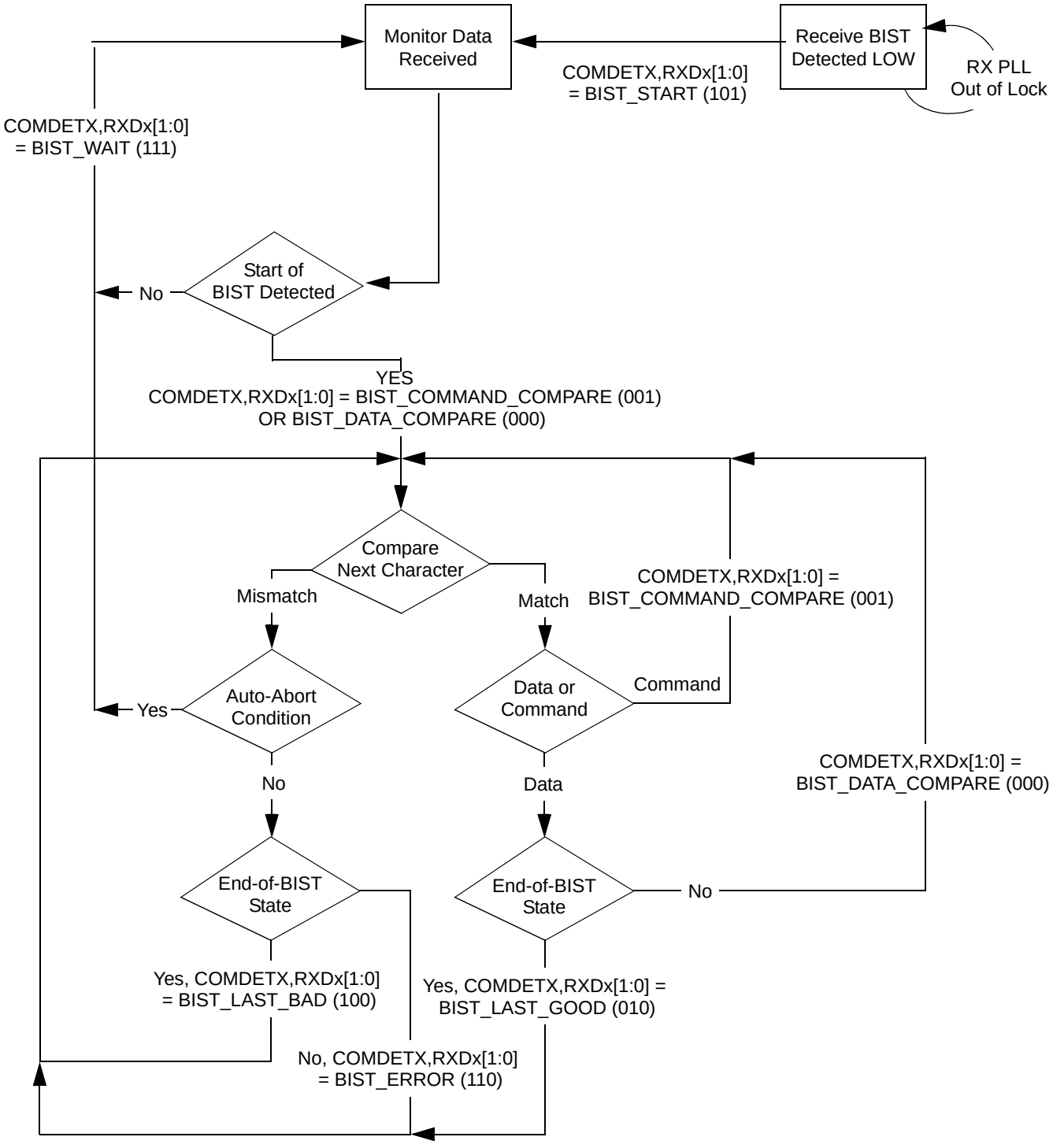


Figure 2. Receive BIST State Machine

Maximum Ratings

(Above which the useful life may be impaired. User guidelines only, not tested.

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

DC Voltage Applied to LVTTL Outputs in High-Z State .....–0.5V to V_{CC} + 0.5V

Supply Voltage to Ground Potential ..... –0.5V to +3.8V

Output Current into LVTTL Outputs (LOW).....60 mA

DC Input Voltage.....–0.5V to V_{CC} + 0.5V

Static Discharge Voltage.....> 2000 V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

Power-up Requirements

The CYP(V)15G0402DXB contains one power supply. The voltage on any input or I/O pin cannot exceed the power pin during power-up.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 5%
Industrial	–40°C to +85°C	3.3V ± 5%

CYP(V)15G0402DXB DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
LVTTL-compatible Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = –4 mA, V_{CC} = Min.	2.4	V_{CC}	V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA, V_{CC} = Min.	0	0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0V[13]	–20	–100	mA
I_{OZL}	High-Z Output Leakage Current		–20	20	mA
LVTTL-compatible Inputs					
V_{IHT}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLK Input, V_{IN} = V_{CC}		+1.5	mA
		Other Inputs, V_{IN} = V_{CC}		+40	µA
I_{ILT}	Input LOW Current	REFCLK Input, V_{IN} = 0.0V		–1.5	mA
		Other Inputs, V_{IN} = 0.0V		–40	µA
I_{IHPDT}	Input HIGH Current with internal pull-down	V_{IN} = V_{CC}		+200	µA
I_{ILPUT}	Input LOW Current with internal pull-up	V_{IN} = 0.0V		–200	µA
LVDIFF Inputs: REFCLK±					
V_{DIFF}[14]	Input Differential Voltage		400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage		1.2	V_{CC}	V
V_{ILLP}	Lowest Input LOW voltage		0.0	V_{CC}/2	V
V_{COMREF}[15]	Common Mode Range		1.0	V_{CC} – 1.2V	V
Three-level Inputs					
V_{IHH}	Three-level Input HIGH Voltage	Min. ≤ V_{CC} ≤ Max.	0.87 * V_{CC}	V_{CC}	V
V_{IMM}	Three-level Input MID Voltage	Min. ≤ V_{CC} ≤ Max.	0.47 * V_{CC}	0.53 * V_{CC}	V
V_{ILL}	Three-level Input LOW Voltage	Min. ≤ V_{CC} ≤ Max.	0.0	0.13 * V_{CC}	V
I_{IHH}	Input High Current	Vin = Vcc		200	µA
I_{IMM}	Input MID Current	Vin = Vcc/2	–50	50	µA
I_{ILL}	Input LOW Current	Vin = GND		–200	µA
Differential CML Serial Outputs: OUTA±, OUTB±, OUTC±, OUTD±			**Typ.**	**Max.**	**Unit**
V_{OHC}	Output HIGH Voltage	100Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
		150Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V

Notes:

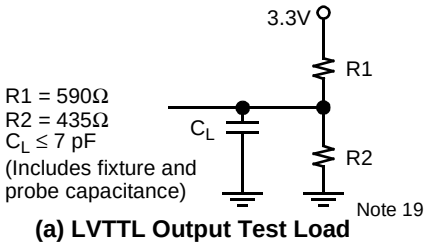
13. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
14. This is the minimum difference in voltage between the true and complement inputs required to ensure detection of a logic-1 or logic-0. A logic-1 exists when the true (+) input is more positive than the complement (–) input. A logic-0 exists when the complement (-) input is more positive than true (+) input.
15. The common mode range defines the allowable range of REFCLK+ and REFCLK– when REFCLK+ = REFCLK–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.

CYP(V)15G0402DXB DC Electrical Characteristics Over the Operating Range (continued)

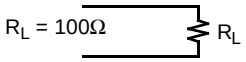
Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OLC}	Output LOW Voltage	100Ω differential load	V_{CC} – 1.1	V_{CC} – 0.7	V
		150Ω differential load	V_{CC} – 1.1	V_{CC} – 0.7	V
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	100Ω differential load	450	900	mV
		150Ω differential load	560	1000	mV
Differential Serial Line Receiver Inputs: INA±, INB±, INC±, IND±					
VI_{DIFFS}[14]	Input Differential Voltage |(IN+) – (IN-)|		100	1200	mV
V_{IHE}	Highest Input HIGH Voltage			V_{CC}	V
V_{ILE}	Lowest Input LOW Voltage		V_{CC} – 2.0		V
I_{IHE}	Input HIGH Current	$V_{IN} = V_{IHH}$ Max.		1350	mA
I_{ILE}	Input LOW Current	$V_{IN} = V_{ILL}$ Min.	–700		mA
V_{COM}[16]	Common mode input range	((V_{CC} – 2.0) + 0.05)Min., (MinV_{CC} – 0.005)Max.	+1.25	+3.1	V

Power Supply			Typ.[18]	Max.[17]	Unit
I_{CC}	Power Supply Current REFCLK = Max.	Commercial	760	1060	mA
		Industrial		1100	mA
I_{CC}	Power Supply Current REFCLK = 125 MHz	Commercial	750	1060	mA
		Industrial		1100	mA

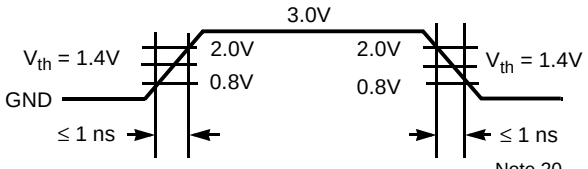
Test Loads and Waveforms



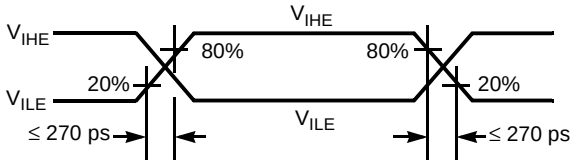
(a) LVTTL Output Test Load



(b) CML Output Test Load Note 19



(c) LVTTL Input Test Waveform



(d) CML/LVPECL Input Test Waveform

Notes:

16. The common mode range defines the allowable range of INPUT+ and INPUT– when INPUT+ = INPUT–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.
17. Maximum I_{CC} is measured with V_{CC} = MAX, RFEN = LOW with all channels and Serial Line Drivers enabled, sending a continuous alternating 01 pattern, and outputs unloaded.
18. Typical I_{CC} is measured under similar conditions except with V_{CC} = 3.3V, T_A = 25°C, RFEN = LOW, with all channels enabled and one Serial Line Driver per transmit channel sending a continuous alternating 01 pattern.
19. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only. 5-pF differential load reflects tester capacitance, and is recommended at low data rates only.
20. The LVTTL switching threshold is 1.4V. All timing references are made relative to the point where the signal edges crosses the threshold voltage.

CYP(V)15G0402DXB AC Characteristics

Over the Operating Range

CYP(V)15G0402DXB Transmitter LVTTL Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{TS}	TXCLKx Clock Frequency	19.5	150	MHz
t_{TXCLK}	TXCLKx Period	6.66	51.28	ns
t_{TXCLKH} [21]	TXCLKx HIGH Time	2.2		ns
t_{TXCLKL} [21]	TXCLKx LOW Time	2.2		ns
t_{TXCLKR} [21, 22, 23]	TXCLKx Rise Time	0.2	1.7	ns
t_{TXCLKF} [21, 22, 23]	TXCLKx Fall Time	0.2	1.7	ns
t_{TXDS}	Transmit Data Set-up Time to TXCLKx↑ (TXCKSEL ≠ LOW)	1.7		ns
t_{TXDH}	Transmit Data Hold Time from TXCLKx↑ (TXCKSEL ≠ LOW)	0.8		ns
f_{TOS}	TXCLKO Clock Frequency = 1x or 2x REFCLK Frequency	19.5	150	MHz
t_{TXCLKO}	TXCLKO Period	6.66	51.28	ns
$t_{TXCLKOD+}$	TXCLKO+ Duty Cycle with 60% HIGH time	–1.0	+0.5	ns
$t_{TXCLKOD–}$	TXCLKO– Duty Cycle with 40% HIGH time	–0.5	+1.0	ns

CYP(V)15G0402DXB Receiver LVTTL Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{RS}	RXCLKx Clock Output Frequency	9.75	150	MHz
t_{RXCLKP}	RXCLKx Period	6.66	102.56	ns
t_{RXCLKH}	RXCLKx HIGH Time (RXRATE = LOW)	2.33[21]	26	ns
	RXCLKx HIGH Time (RXRATE = HIGH)	5.66	52	ns
t_{RXCLKL}	RXCLKx LOW Time (RXRATE = LOW)	2.33[21]	26	ns
	RXCLKx LOW Time (RXRATE = HIGH)	5.66	52	ns
t_{RXCLKD}	RXCLKx Duty Cycle centered at 50%	–1.0	+1.0	ns
t_{RXCLKR} [21]	RXCLKx Rise Time	0.3	1.2	ns
t_{RXCLKF} [21]	RXCLKx Fall Time	0.3	1.2	ns
$t_{RXDV–}$ [24]	Status and Data Valid Time to RXCLKx (RXCKSEL HIGH or MID)	5UI – 1.5		ns

CYP(V)15G0402DXB REFCLK Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{REF}	REFCLK Clock Frequency	19.5	150	MHz
t_{REFCLK}	REFCLK Period	6.6	51.28	ns
t_{REFH}	REFCLK HIGH Time (TXRATE = HIGH)	5.9		ns
	REFCLK HIGH Time (TXRATE = LOW)	2.9[21]		ns
t_{REFL}	REFCLK LOW Time (TXRATE = HIGH)	5.9		ns
	REFCLK LOW Time (TXRATE = LOW)	2.9[21]		ns
t_{REFD} [25]	REFCLK Duty Cycle	30	70	%
t_{REFR} [21, 22, 23]	REFCLK Rise Time (20% – 80%)		2	ns
t_{REFF} [21, 22, 23]	REFCLK Fall Time (20% – 80%)		2	ns
t_{TREFDS}	Transmit Data Setup Time to REFCLK (TXCKSEL = LOW)	1.7		ns
t_{TREFDH}	Transmit Data Hold Time from REFCLK (TXCKSEL = LOW)	0.8		ns

Notes:

21. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
22. The ratio of rise time to falling time must not vary by greater than 2:1.
23. For a given operating frequency, neither rise or fall specification can be greater than 20% of the clock-cycle period or the data sheet maximum time.
24. Parallel data output specifications are only valid if all inputs or outputs are loaded with similar DC and AC loads.
25. The duty cycle specification is a simultaneous condition with the t_{REFH} and t_{REFL} parameters. This means that at faster character rates the REFCLK duty cycle cannot be as large as 30% – 70%.

CYP(V)15G0402DXB REFCLK Switching Characteristics Over the Operating Range (continued)

Parameter	Description	Min.	Max.	Unit
t_{RREFDA}	Receive Data Access Time from REFCLK (RXCKSEL = LOW)		9.5	ns
t_{RREFDV}	Receive Data Valid Time from REFCLK (RXCKSEL = LOW)	4.0		ns
$t_{REFADV–}$	Received Data Valid Time to RXCLKA (RXCKSEL = LOW)	10UI – 4.7		ns
$t_{REFADV+}$	Received Data Valid Time from RXCLKA (RXCKSEL = LOW)	1.5		ns
$t_{REFCDV–}$	Received Data Valid Time to RXCLKC (RXCKSEL = LOW)	10UI – 4.3		ns
$t_{REFCDV+}$	Received Data Valid Time from RXCLKC (RXCKSEL = LOW)	0.2		ns
t_{REFRX} [26]	REFCLK Frequency Referenced to Received Clock Period	–0.02	+0.02	%

CYP(V)15G0402DXB Transmit Serial Outputs and TX PLL Characteristics Over the Operating Range

Parameter	Description	Condition	Min.	Max.	Unit
t_B	Bit Time		5100	660	ps
t_{RISE} [21]	CML Output Rise Time 20% – 80% (CML Test Load)	SPDSEL = HIGH	50	270	ps
		SPDSEL = MID	100	500	ps
		SPDSEL = LOW	180	1000	ps
t_{FALL} [21]	CML Output Fall Time 80% – 20% (CML Test Load)	SPDSEL = HIGH	50	270	ps
		SPDSEL = MID	100	500	ps
		SPDSEL = LOW	180	1000	ps
t_{DJ} [21, 27, 29]	Deterministic Jitter (peak-peak)	IEEE 802.3z		25	ps
t_{RJ} [21, 28, 29]	Random Jitter (σ)	IEEE 802.3z		11	ps
t_{TXLOCK}	Transmit PLL lock to REFCLK			200	us

CYP(V)15G0402DXB Receive Serial Inputs and CDR PLL Characteristics Over the Operating Range

t_{RXLOCK}	Receive PLL lock to input data stream (cold start)			376K	UI
	Receive PLL lock to input data stream			376K	UI
$t_{RXUNLOCK}$	Receive PLL Unlock Rate			46	UI
t_{JTOL}	Total Jitter Tolerance	IEEE 802.3z	600		ps
t_{DJTOL}	Deterministic Jitter Tolerance	IEEE 802.3z	370		ps

Capacitance [21]

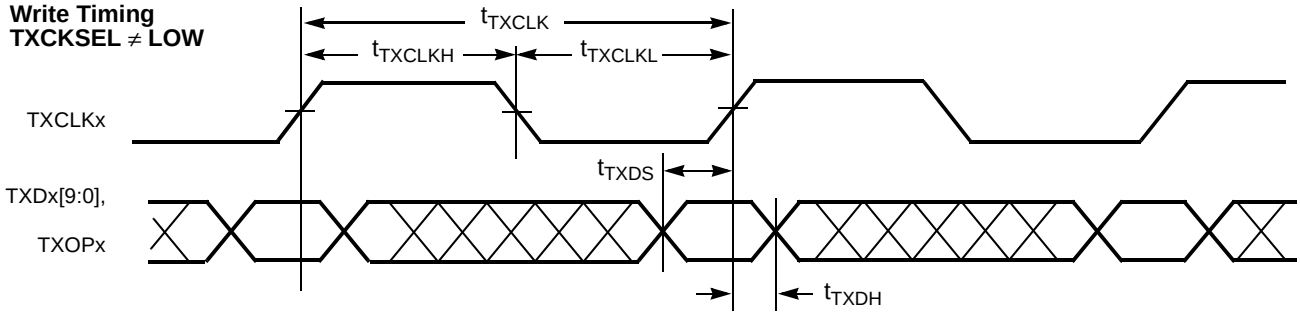
Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	7	pF
C_{INPECL}	PECL input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	4	pF

Notes:

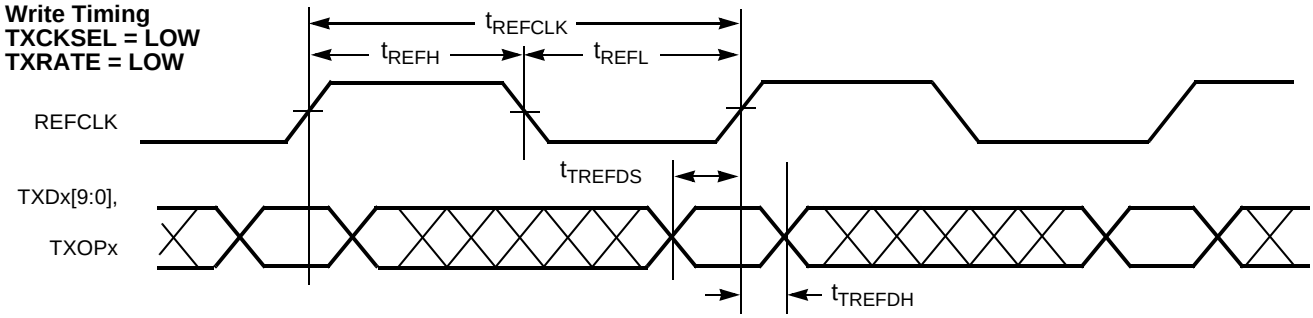
26. REFCLK has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within ±200 PPM (±0.02%) of the transmitter PLL reference (REFCLK) frequency, necessitating a ±100-PPM crystal.
27. While sending continuous K28.5s, outputs loaded to a balanced 100Ω load, measured at the cross point of differential outputs, over the operating range.
28. While sending continuous K28.7s, after 100,000 samples measured at the cross point of differential outputs, time referenced to REFCLK input, over the operating range.
29. Total jitter is calculated at an assumed BER of 1E –12. Hence: total jitter (t_J) = (t_{RJ} * 14) + t_{DJ}.
30. Receiver UI (Unit Interval) is calculated as 1 / (f_{REF} * 20) (when RXRATE = HIGH) or 1 / (f_{REF} * 10) (when RXRATE = LOW) if no data is being received, or 1 / (f_{REF} * 20) (when RXRATE = HIGH) or 1 / (f_{REF} * 10) (when RXRATE = LOW) of the remote transmitter if data is being received. In an operating link this is equivalent to t_B.

CYP(V)15G0402DXB HOTLink II Transmitter Switching Waveforms

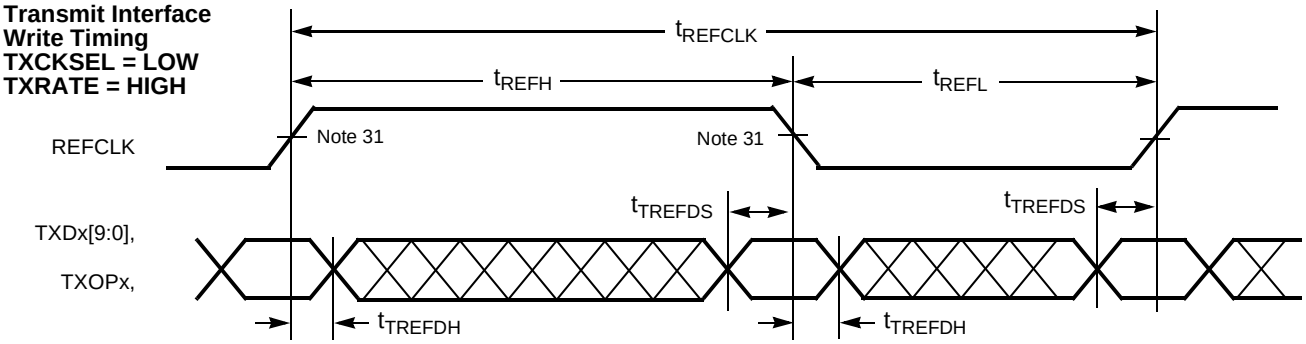
Transmit Interface Write Timing TXCKSEL ≠ LOW



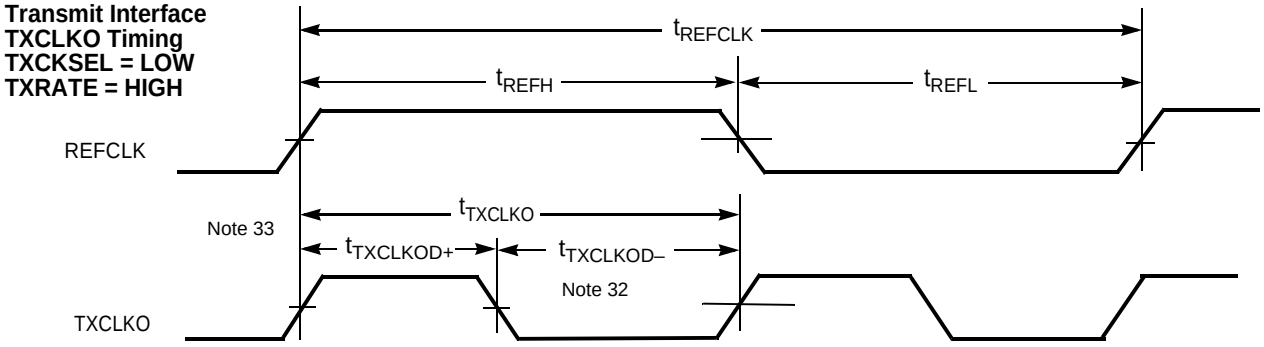
Transmit Interface Write Timing TXCKSEL = LOW TXRATE = LOW



Transmit Interface Write Timing TXCKSEL = LOW TXRATE = HIGH



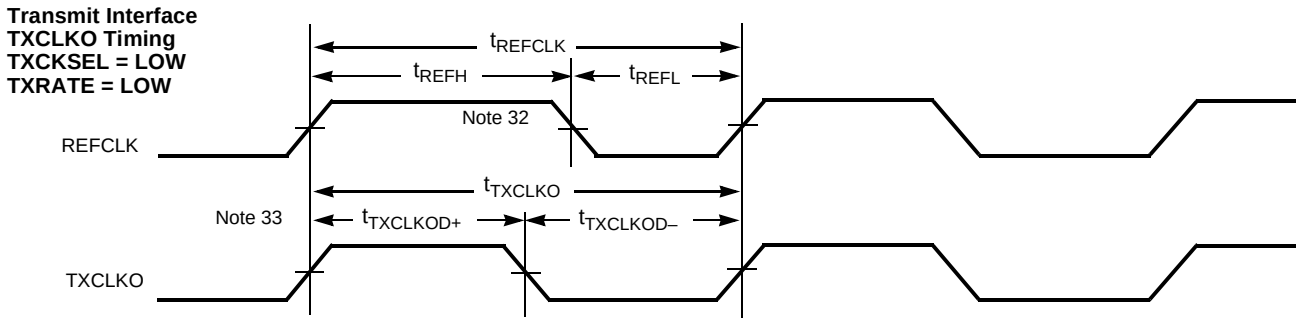
Transmit Interface TXCLKO Timing TXCKSEL = LOW TXRATE = HIGH



Notes:

31. When REFCLK is configured for half-rate operation (TXRATE = HIGH) and data is captured using REFCLK instead of a TXCLKx clock (TXCKSEL = LOW), data is captured using both the rising and falling edges of REFCLK.
32. The TXCLKO output remains at the character rate regardless of the state of TXRATE and does not follow the duty cycle of REFCLK.
33. The rising edge of TXCLKO output has no direct phase relationship to the REFCLK input.

CYP(V)15G0402DXB HOTLink II Transmitter Switching Waveforms (continued)



Switching Waveforms for the CYP(V)15G0402DXB HOTLink II Receiver

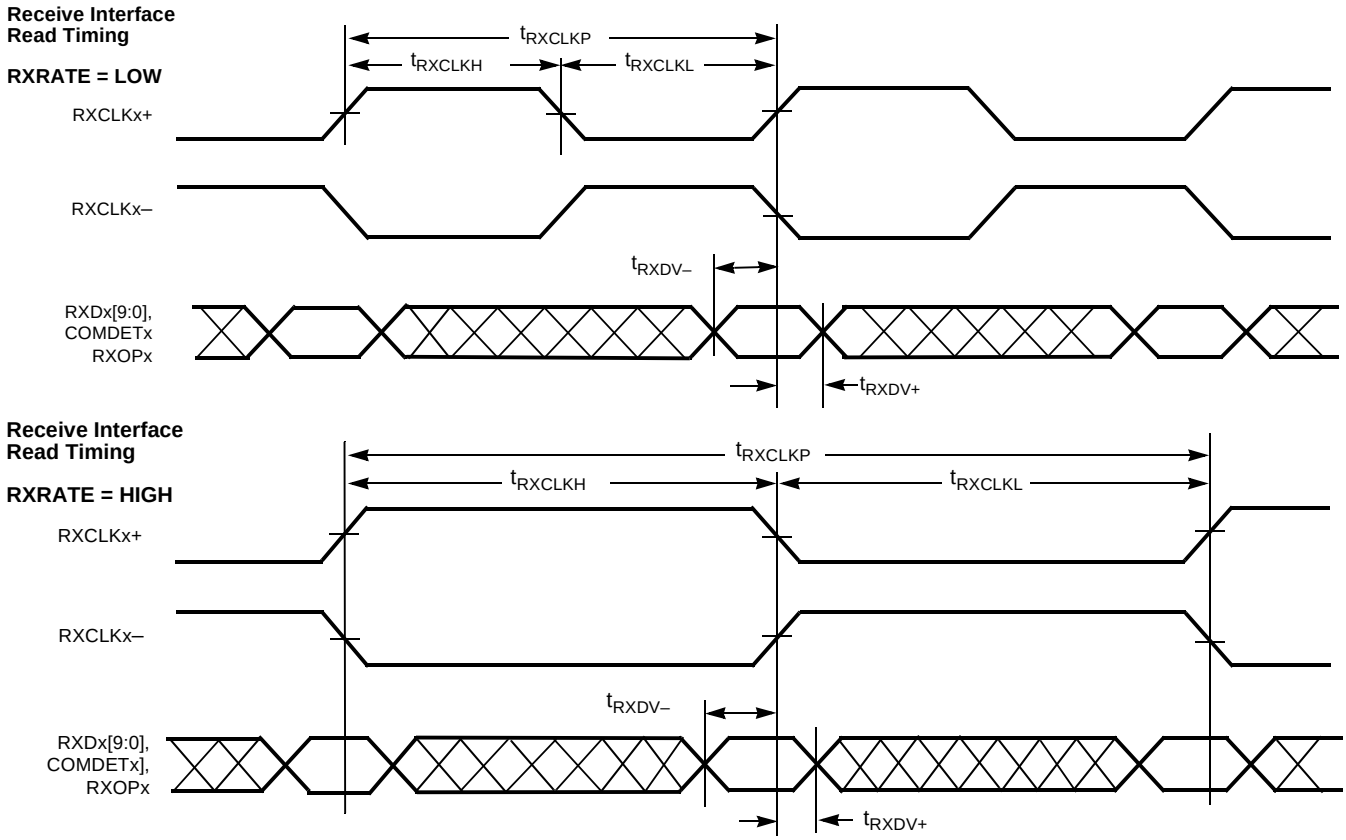


Table 9. Package Coordinate Signal Allocation

Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type
A01	INC–	CML IN	C04	LPENB	LVTTL IN	E19	VCC	POWER
A02	OUTC–	CML OUT	C05	VCC	POWER	E20	VCC	POWER
A03	N/C	NO CONNECT	C06	PARCTL	3-LEVEL SEL	F01	TXPERC	LVTTL OUT
A04	N/C	NO CONNECT	C07	SDASEL	3-LEVEL SEL	F02	TXOPC	LVTTL IN PU
A05	VCC	POWER	C08	GND	GROUND	F03	TXDC[0]	LVTTL IN
A06	IND–	CML IN	C09	BOE[7]	LVTTL IN PU	F04	N/C	NO CONNECT
A07	OUTD–	CML OUT	C10	BOE[5]	LVTTL IN PU	F17	BISTLE	LVTTL IN PU
A08	GND	GROUND	C11	BOE[3]	LVTTL IN PU	F18	RXDB[0]	LVTTL OUT
A09	N/C	NO CONNECT	C12	BOE[1]	LVTTL IN PU	F19	RXOPB	LVTTL 3-S OUT
A10	N/C	CML OUT	C13	GND	GROUND	F20	RXDB[1]	LVTTL OUT
A11	INA–	CML IN	C14	GND	GROUND	G01	TXDC[7]	LVTTL IN
A12	OUTA–	CML OUT	C15	GND	GROUND	G02	TXCKSEL	3-LEVEL SEL
A13	GND	GROUND	C16	VCC	POWER	G03	TXDC[4]	LVTTL IN
A14	N/C	NO CONNECT	C17	TXRATE	LVTTL IN PD	G04	TXDC[1]	LVTTL IN
A15	N/C	NO CONNECT	C18	RXRATE	LVTTL IN PD	G17	GND	GROUND
A16	VCC	POWER	C19	N/C	NO CONNECT	G18	OELE	LVTTL IN PU
A17	INB–	CML IN	C20	TDO	LVTTL 3-S OUT	G19	FRAMCHAR	3-LEVEL SEL
A18	OUTB–	CML OUT	D01	TCLK	LVTTL IN PD	G20	RXDB[3]	LVTTL OUT
A19	N/C	NO CONNECT	D02	$\overline{\text{TRSTZ}}$	LVTTL IN PU	H01	GND	GROUND
A20	N/C	NO CONNECT	D03	LPEND	LVTTL IN	H02	GND	GROUND
B01	INC+	CML IN	D04	LPENA	LVTTL IN	H03	GND	GROUND
B02	OUTC+	CML OUT	D05	VCC	POWER	H04	GND	GROUND
B03	N/C	NO CONNECT	D06	RFMODE	3-LEVEL SEL	H17	GND	GROUND
B04	N/C	NO CONNECT	D07	SPDSEL	3-LEVEL SEL	H18	GND	GROUND
B05	VCC	POWER	D08	GND	GROUND	H19	GND	GROUND
B06	IND+	CML IN	D09	BOE[6]	LVTTL IN PU	H20	GND	GROUND
B07	OUTD+	CML OUT	D10	BOE[4]	LVTTL IN PU	J01	TXDC[9]	LVTTL IN
B08	GND	GROUND	D11	BOE[2]	LVTTL IN PU	J02	TXDC[5]	LVTTL IN
B09	N/C	NO CONNECT	D12	BOE[0]	LVTTL IN PU	J03	TXDC[2]	LVTTL IN
B10	N/C	NO CONNECT	D13	GND	GROUND	J04	TXDC[3]	LVTTL IN
B11	INA+	CML IN	D14	GND	GROUND	J17	COMDETB	LVTTL OUT
B12	OUTA+	CML OUT	D15	GND	GROUND	J18	RXDB[2]	LVTTL OUT
B13	GND	GROUND	D16	VCC	POWER	J19	RXDB[7]	LVTTL OUT
B14	N/C	NO CONNECT	D17	N/C	NO CONNECT	J20	RXDB[4]	LVTTL OUT
B15	N/C	NO CONNECT	D18	RXLE	LVTTL IN PU	K01	RXDC[4]	LVTTL OUT
B16	VCC	POWER	D19	N/C	NO CONNECT	K02	RXCLKC–	LVTTL OUT
B17	INB+	CML IN	D20	N/C	NO CONNECT	K03	TXDC[8]	LVTTL IN
B18	OUTB+	CML OUT	E01	VCC	POWER	K04	$\overline{\text{LFIC}}$	LVTTL OUT
B19	N/C	NO CONNECT	E02	VCC	POWER	K17	RXDB[5]	LVTTL OUT
B20	N/C	NO CONNECT	E03	VCC	POWER	K18	RXDB[6]	LVTTL OUT
C01	TDI	LVTTL IN PU	E04	VCC	POWER	K19	RXDB[9]	LVTTL OUT
C02	TMS	LVTTL IN PU	E17	VCC	POWER	K20	RXCLKB+	LVTTL I/O PD
C03	LPENC	LVTTL IN	E18	VCC	POWER	L01	RXDC[5]	LVTTL OUT

Table 9. Package Coordinate Signal Allocation (continued)

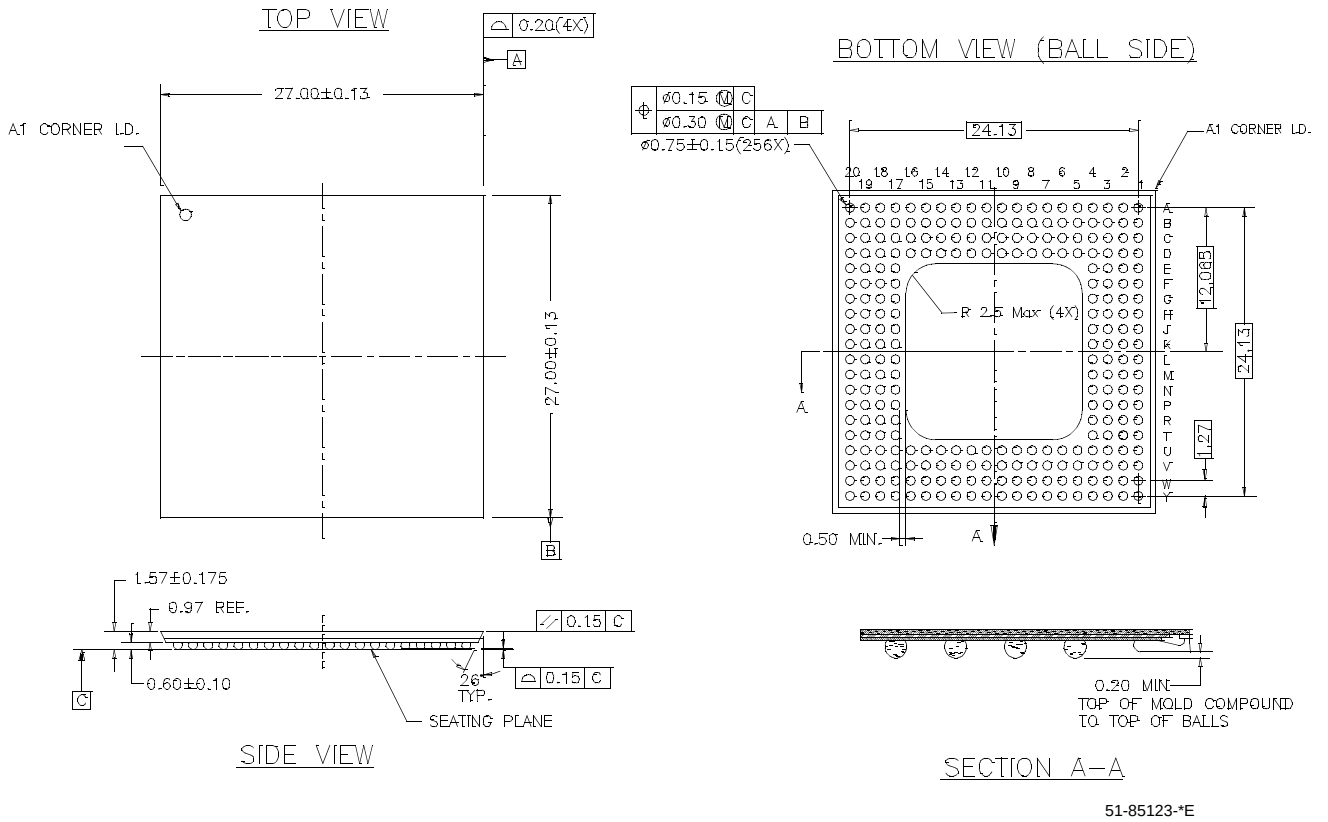
Ball ID	Signal Name	Signal Type
L02	RXCLKC+	LVTTL I/O PD
L03	TXCLKC	LVTTL IN PD
L04	TXDC[6]	LVTTL IN
L17	RXDB[8]	LVTTL OUT
L18	$\overline{\text{LFIB}}$	LVTTL OUT
L19	RXCLKB–	LVTTL I/O PD
L20	TXDB[6]	LVTTL IN
M01	RXDC[6]	LVTTL OUT
M02	RXDC[7]	LVTTL OUT
M03	RXDC[9]	LVTTL OUT
M04	RXDC[8]	LVTTL OUT
M17	TXDB[9]	LVTTL IN
M18	TXDB[8]	LVTTL IN
M19	TXDB[7]	LVTTL IN
M20	TXCLKB	LVTTL IN PD
N01	GND	GROUND
N02	GND	GROUND
N03	GND	GROUND
N04	GND	GROUND
N17	GND	GROUND
N18	GND	GROUND
N19	GND	GROUND
N20	GND	GROUND
P01	RXDC[3]	LVTTL OUT
P02	RXDC[2]	LVTTL OUT
P03	RXDC[1]	LVTTL OUT
P04	RXDC[0]	LVTTL OUT
P17	TXDB[5]	LVTTL IN
P18	TXDB[4]	LVTTL IN
P19	TXDB[3]	LVTTL IN
P20	TXDB[2]	LVTTL IN
R01	COMDETC	LVTTL OUT
R02	RXOPC	LVTTL 3-S OUT
R03	TXPERD	LVTTL OUT
R04	TXOPD	LVTTL IN PU
R17	TXDB[1]	LVTTL IN
R18	TXDB[0]	LVTTL IN
R19	TXOPB	LVTTL IN PU
R20	TXPERB	LVTTL OUT
T01	VCC	POWER
T02	VCC	POWER
T03	VCC	POWER
T04	VCC	POWER
T17	VCC	POWER
T18	VCC	POWER
T19	VCC	POWER
T20	VCC	POWER
U01	TXDD[0]	LVTTL IN
U02	TXDD[1]	LVTTL IN
U03	TXDD[2]	LVTTL IN
U04	TXDD[9]	LVTTL IN
U05	VCC	POWER
U06	RXDD[4]	LVTTL OUT
U07	RXDD[3]	LVTTL OUT
U08	GND	GROUND
U09	RXOPD	LVTTL 3-S OUT
U10	RFENC	LVTTL IN PD
U11	REFCLK–	PECL IN
U12	TXDA[1]	LVTTL IN
U13	GND	GROUND
U14	TXDA[4]	LVTTL IN
U15	TXDA[8]	LVTTL IN
U16	VCC	POWER
U17	RXDA[4]	LVTTL OUT
U18	RXOPA	LVTTL OUT
U19	COMDETA	LVTTL OUT
U20	RXDA[0]	LVTTL OUT
V01	TXDD[3]	LVTTL IN
V02	TXDD[4]	LVTTL IN
V03	TXDD[8]	LVTTL IN
V04	RXDD[8]	LVTTL OUT
V05	VCC	POWER
V06	RXDD[5]	LVTTL OUT
V07	RXDD[1]	LVTTL OUT
V08	GND	GROUND
V09	COMDETD	LVTTL OUT
V10	RFEND	LVTTL IN PD
V11	REFCLK+	PECL IN
V12	RFENB	LVTTL IN PD
V13	GND	GROUND
V14	TXDA[3]	LVTTL IN
V15	TXDA[7]	LVTTL IN
V16	VCC	POWER
V17	RXDA[9]	LVTTL OUT
V18	RXDA[5]	LVTTL OUT
V19	RXDA[2]	LVTTL OUT
V20	RXDA[1]	LVTTL OUT
W01	TXDD[5]	LVTTL IN
W02	TXDD[7]	LVTTL IN
W03	$\overline{\text{LFID}}$	LVTTL OUT
W04	RXCLKD–	LVTTL OUT
W05	VCC	POWER
W06	RXDD[6]	LVTTL OUT
W07	RXDD[0]	LVTTL OUT
W08	GND	GROUND
W09	TXCLKO–	LVTTL OUT
W10	$\overline{\text{TXRST}}$	LVTTL IN PU
W11	TXOPA	LVTTL IN PU
W12	RFENA	LVTTL IN PD
W13	GND	GROUND
W14	TXDA[2]	LVTTL IN
W15	TXDA[6]	LVTTL IN
W16	VCC	POWER
W17	$\overline{\text{LFIA}}$	LVTTL OUT
W18	RXCLKA–	LVTTL OUT
W19	RXDA[6]	LVTTL OUT
W20	RXDA[3]	LVTTL OUT
Y01	TXDD[6]	LVTTL IN
Y02	TXCLKD	LVTTL IN
Y03	RXDD[9]	LVTTL OUT
Y04	RXCLKD+	LVTTL I/O PD
Y05	VCC	POWER
Y06	RXDD[7]	LVTTL OUT
Y07	RXDD[2]	LVTTL OUT
Y08	GND	GROUND
Y09	TXCLKO+	LVTTL OUT
Y10	N/C	NO CONNECT
Y11	TXCLKA	LVTTL IN PD
Y12	TXPERA	LVTTL OUT
Y13	GND	GROUND
Y14	TXDA[0]	LVTTL IN
Y15	TXDA[5]	LVTTL IN
Y16	VCC	POWER
Y17	TXDA[9]	LVTTL IN
Y18	RXCLKA+	LVTTL I/O PD
Y19	RXDA[8]	LVTTL OUT
Y20	RXDA[7]	LVTTL OUT

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
Standard	CYP15G0402DXB-BGC	BL256	256-ball Thermally Enhanced Ball Grid Array	Commercial
Standard	CYP15G0402DXB-BGI	BL256	256-ball Thermally Enhanced Ball Grid Array	Industrial
Standard	CYV15G0402DXB-BGC	BL256	256-ball Thermally Enhanced Ball Grid Array	Commercial
Standard	CYV15G0402DXB-BGI	BL256	256-ball Thermally Enhanced Ball Grid Array	Industrial

Package Diagram

256-lead L2 Ball Grid Array (27 x 27 x 1.57 mm) BL256



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Document History Page

Document Title:CYP(V)15G0402DXB Quad HOTLink II™ SERDES Document Number: 38-02057				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	116285	07/16/02	SDR	New Data Sheet
*A	118985	09/30/02	LNM	Changed TXCLKO description Changed TXPERx description introduced SMPTE pathological test clause Removed the LOW setting for FRAMCHAR and related references Changed V_{ODIF} and V_{OLC} for CML output Changed the I_{OST} boundary values Changed the t_{TXCLKR} and t_{TXCLKF} min values Changed t_{TXDS} and t_{TXDH} and t_{TREFDS} and t_{TREFDH} Changed $t_{REFADV-}$ and $t_{REFCDV-}$ and $t_{REFCDV+}$ Changed the JTAG ID from 0C801069 to 1C801069
*B	122545	12/09/02	CGX	Changed Minimum tRISE/tFALL for CML Changed tTXCLKOD+, tTXCLKOD- for LVTTL Changed tRXLOCK Changed tDJ, tRJ Changed tJTOL Changed tTXLOCK Changed tRXCLKH, tRXCLKL Changed Power Specs Changed verbiage...Paragraph: Clock/Data Recovery Changed verbiage...Paragraph: Range Control Updated differences to pin configuration and pin table Added Power-up Requirements
*C	122211	12/28/02	RBI	Minor change Document Control corrected Document History Page
*D	124992	04/15/03	POT	Changed CYP15G0402DXB to CYP(V)15G0402DXB type corresponding to Video-compliant parts . Reduced the lower limit of the serial signaling rate from 200 Mbaud to 195 Mbaud and changed the associated specifications accordingly.