WirelessUSB™ EX Baseband IC

1.0 Features

- **Low cost, low power, 2.4-GHz WirelessUSB™ EX baseband IC**
- **Frequency-hopping, spread-spectrum (FHSS)**
- **Coexists with other 2.4-GHz systems**
- **Low latency, high throughput**
- **Bidirectional communication**
- **Forward Error Correction (FEC) and automatic packet retry**
- **Low battery power detection**
- **Supports up to seven peripherals (multi-drop)**
- **Direct support of optical mouse**
- **Direct support of 18 x 8 keyboard scan matrix**
- **Direct support of Cypress *enCoRe*™ IC for USB bridge applications**
- **Wide operating voltage (2.7 to 3.6V)**
- **Commercial temperature range (0°C to +70°C)**
- **Low power/sleep mode (I_{SB} ≤ 1.0 µA typical)**
- **Small package 100-pin TQFP (14 x 14 x1.6 mm)**

2.0 Applications

The CYWUSB6942 is targeted for a variety of wireless HID applications, including

- **Mice**
- **Keyboards**
- **USB bridges**
- **Game controllers**

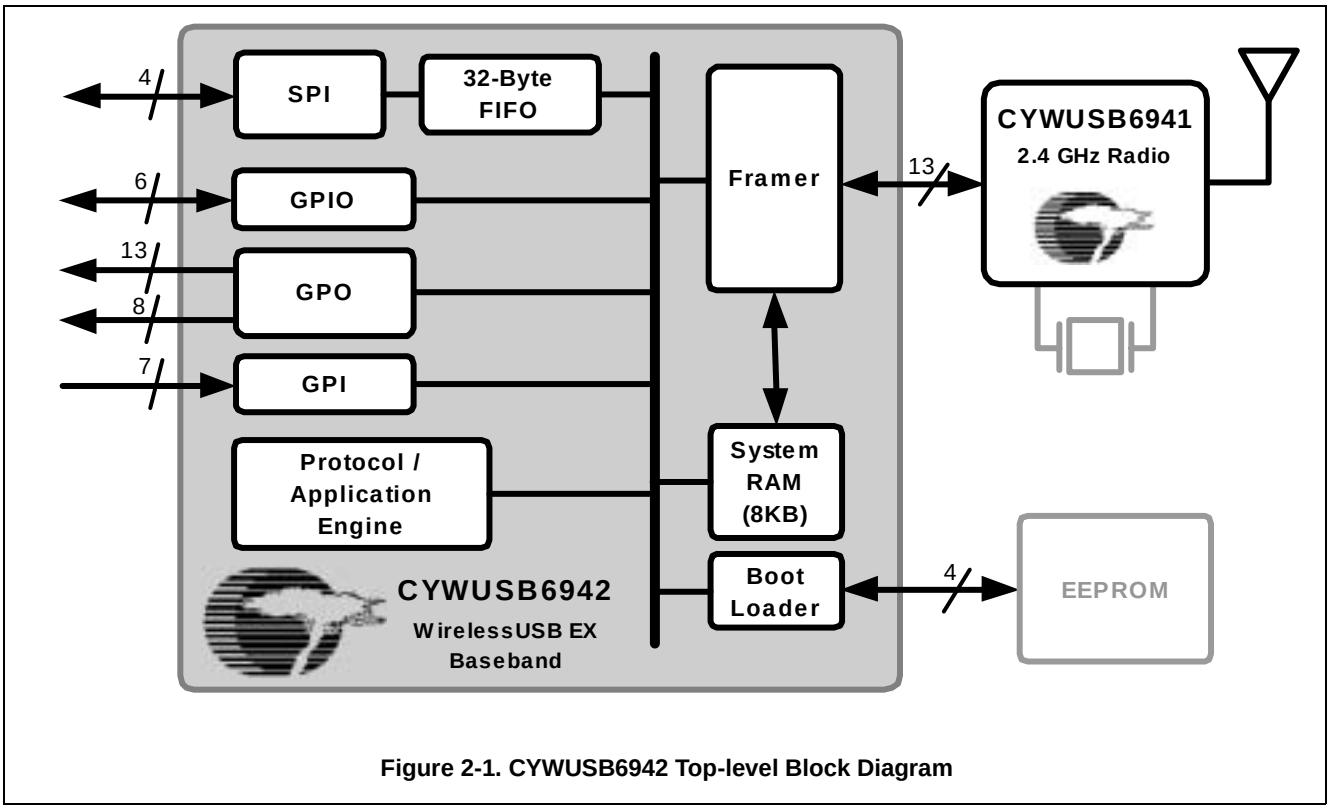

Figure 2-1. CYWUSB6942 Top-level Block Diagram

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3.0 General Description

3.1 Functional Overview

WirelessUSB EX enables low-cost, low-power WirelessHID™ solutions using 2.4-GHz Industrial Scientific Medical (ISM) band and frequency-hopping spread-spectrum (FHSS) technology. The CYWUSB6942 supports wireless peripheral applications such as optical mice, keyboards, and game controllers by transferring data between the peripherals and the host over the air through the WirelessUSB EX protocol.

The CYWUSB6942 WirelessUSB EX Baseband IC is part of a two-device chipset for implementing a WirelessUSB-based application. The CYWUSB6941 WirelessUSB Radio IC is also needed to complete the WirelessUSB EX chipset.

When used with a Cypress *enCoRe*™ chip, the WirelessUSB EX chipset also acts as a USB bridge to allow wireless peripherals using the CYWUSB6942 devices to communicate with the host via a low-speed USB link. Data received by the WirelessUSB EX chipset from a peripheral device is transferred to the *enCoRe* chip and then sent upstream to the USB host device. Downstream data is transferred from the *enCoRe* to the WirelessUSB EX chipset and then sent to the peripheral over the air. Each WirelessUSB EX chipset acting as a USB bridge can support up to seven peripherals.

For more information on the WirelessUSB EX system, protocol and internal operations, see our application note entitled *WirelessUSB EX Theory of Operation*.

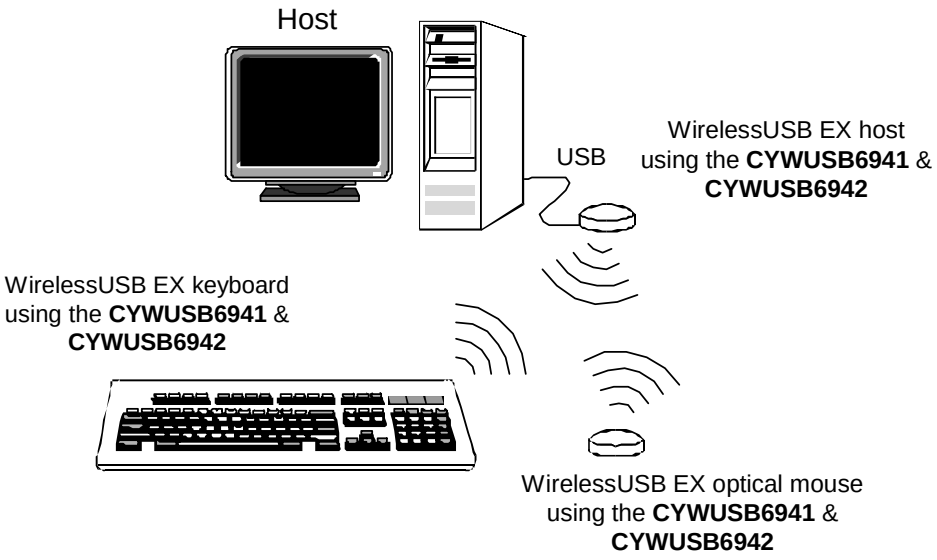


Figure 3-1. CYWUSB6942 Device Family Usage Scenario

3.1.1 Efficient and Reliable Datagram Delivery

The WirelessUSB EX chipset implements a highly-efficient, bidirectional wireless protocol designed to reliably and quickly send and receive data packets between devices with a high throughput of 1 Mbps raw data rate. The WirelessUSB EX Baseband device contains a framer, which handles all bit-level operations, maximizing available processing bandwidth in the Protocol and Application Engines for embedded applications. It also ensures reliable and secure datagram delivery by applying algorithms such as CRC, encryption, data whitening, and Forward Error Correction (FEC).

HID datagrams are delivered over the air using a low power 2.4-GHz FHSS radio that can coexist with other 2.4 GHz systems (e.g., Bluetooth™, IEEE 802.11b, analog cordless phones).

3.1.2 Direct Support for Wireless Peripherals

The CYWUSB6942 device provides direct support for an optical mouse, an 18 × 8 keyboard scan matrix, and a USB host bridge applications when used with the Cypress enCoRe chip. As a result, low cost solutions can be implemented with a minimal number of external components required.

3.1.3 Input/Output Interfaces

The CYWUSB6942 offers up to six general purpose input/output (GPIO) pins, twenty-one GPO pins, seven GPI pins, and a Serial Peripheral Interface (SPI), allowing the implementation of a wide variety of wireless HID applications including mice, keyboards, game controllers, and USB bridges.

3.1.4 Power Management

The CYWUSB6942 provides power management, including a low battery power detection and low-power mode.

3.1.4.1 Low Battery Power Detection

A DC-DC converter can be used to provide the required operating voltage to the system as well as a low battery warning signal via the PFO pin. When the voltage levels provided by the batteries are below a preset threshold, the PFO signal should be asserted, allowing the CYWUSB6942 to take appropriate action.

3.1.4.2 Low-Power Standby/Sleep Mode

The CYWUSB6942 provides support for a very low power mode (ISB < 1.0 µA typical). For details, please refer to *Section 5.4*.

3.1.5 Wide Operating Range

The CYWUSB6942 device is offered with wide operating voltage (2.7 to 3.6V), commercial temperature range (0°C to +70°C), and small package (14 x 14 mm TQFP), providing the flexibility for the implementation of a wide variety of wireless HID applications.

4.0 Architecture Overview

From a top-level, the CYWUSB6942 device consists of the WirelessUSB EX Framer, the Protocol and Application Engines, and a Radio Interface that allows communication with the CYWUSB6941 external 2.4-GHz radio.

4.1 Framer.

The Framer (*Figure 4-1*) handles all bit-wise data packet operations. It retrieves transmit packet header information from the Protocol Engine, payload data from the System RAM, and processes them for transmission by the radio. Data received from the radio is processed into packets, and handed over to the Protocol Engine and System RAM. Functions include error correction, encryption/decryption, whitening/dewhitening, encoding/decoding, channel selection, correlation, synchronization, and data clock recovery. The Framer is controlled by the Protocol Engine, and directly DMAs data to and from the System RAM.

4.2 GPIO/GPO/GPI Blocks.

The GPIO (*Figure 2-1*) block contains up to six independently configurable I/O pins. The General Purpose Output (GPO) block contains up to twenty-one output pins. The General Purpose Input (GPI) block contains up to seven input pins.

4.3 SPI Block

The SPI Block (*Figure 2-1*) is a slave mode serial interface block. Data is not returned to a tri-state mode after SS is de-asserted.

4.4 System RAM

The 8-KB System RAM acts as the data interface between the Protocol Engine and the WirelessUSB EX Framer for transmitting and receiving HID datagrams.

4.5 Protocol/Application Engine

The Protocol Engine is used to implement the link control protocol. It manages low level packet traffic, link set-up and breakdown, and transfers data between the HID and the WirelessUSB EX Packet Engine.

The Application Engine executes application-specific functions for a variety of HIDs, such as mice, keyboards, and gamepads.

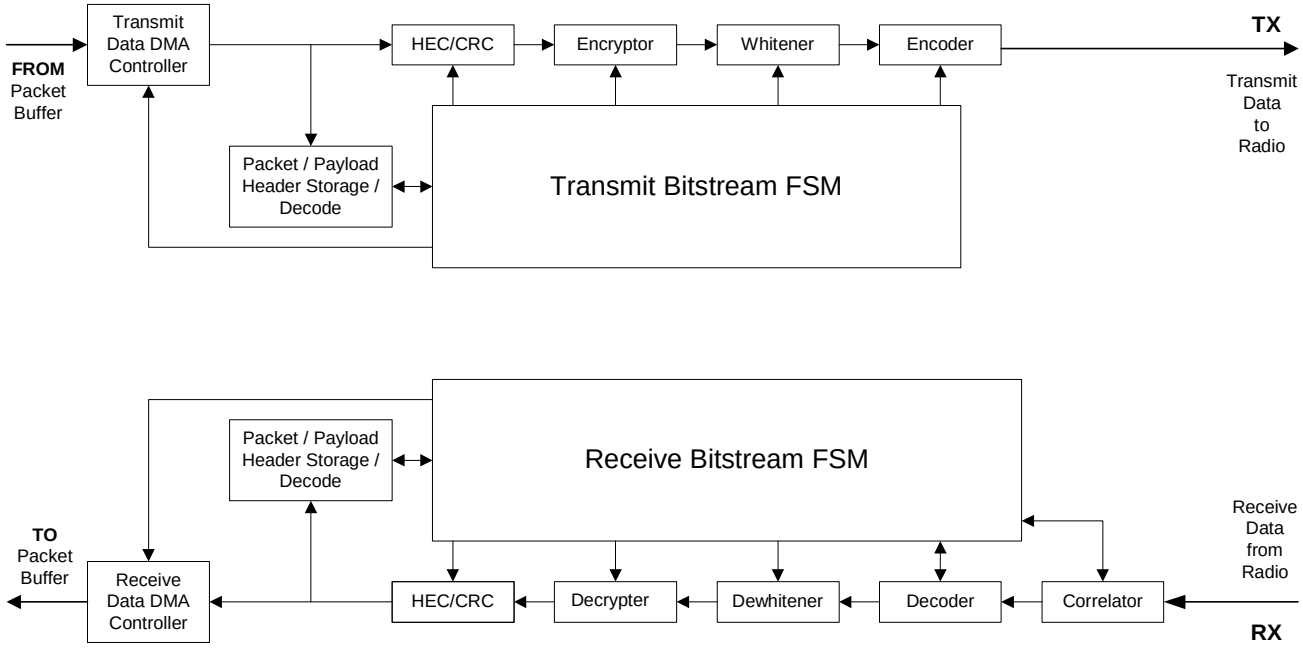


Figure 4-1. CYWUSB6942 Framer Block Diagram

5.0 INTERFACE

5.1 The Radio Control Interface

The CYWUSB6942 radio control interface is the communication interface between the WirelessUSB EX baseband and the CYWUSB6941 WirelessUSB EX Radio. It consists of a data interface and a control interface for transmitting and receiving data, and a serial interface for programming the internal registers of the CYWUSB6941.

There are four subsections of the interface:

- RF data
- Control interface
- Register control interface (serial).
- Master clock.

There are two data lines in the RF data interface and seven signals that are used in the RF control interface, four signals in the serial register control interface, and one system clock. All of the signals are unidirectional. Direction is oriented to/from the CYWUSB6942 baseband IC.

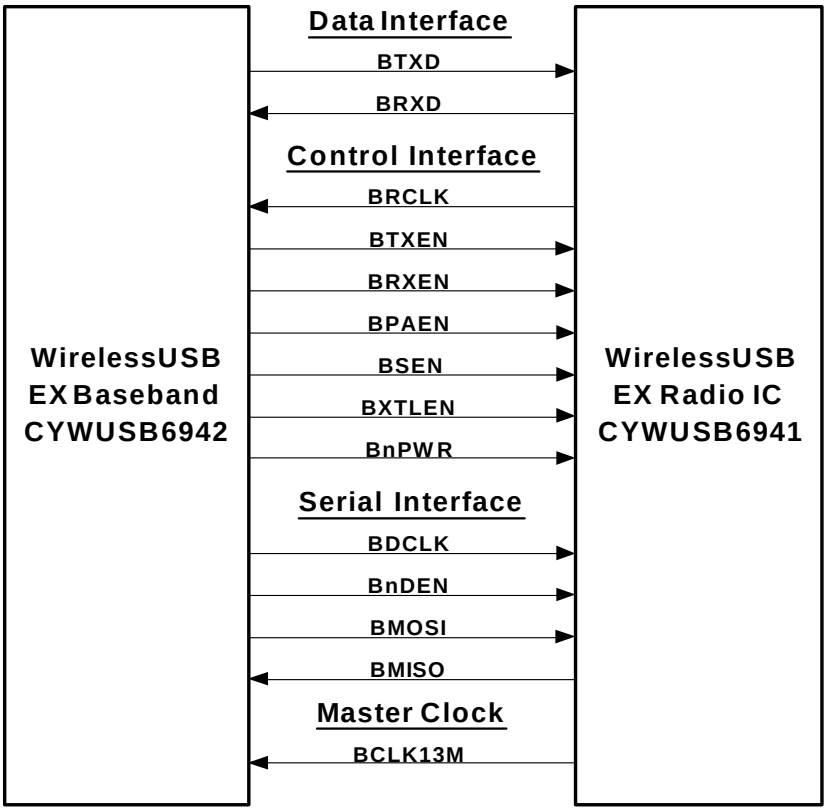


Figure 5-1. CYWUSB6942 Radio Control Interface Diagram

5.2 The SPI Interface

5.2.1 Overview

The SPI is a four-pin serial interface that the CYWUSB6942 uses to communicate with external devices. The SPI is a master/slave interface with the CYWUSB6942 always acting as a slave. The pins used are the SS (Slave Select), SCK (Serial Clock), MOSI (Master-Out/Slave-In), and MISO (Master-In/Slave-Out) pins.

5.2.2 SPI Signaling

The SS, SCK, and MOSI signals are all driven by the master while the CYWUSB6942 drives only the MISO signal. To initiate a byte transfer, the master asserts the SS signal and provides the SCK signal as a clock for the interface. The MOSI data is driven out by the master on the rising edge of SCK and sampled by the CYWUSB6942 on the falling edge of SCK. The MISO data is driven out by the CYWUSB6942 on the rising edge of SCK and sampled by the master on the falling edge of SCK. One bit is transferred per clock cycle, and one byte is transferred in a total of eight clock cycles. Once the transfer is complete, the master can deassert the SS, SCK, and MOSI pins.

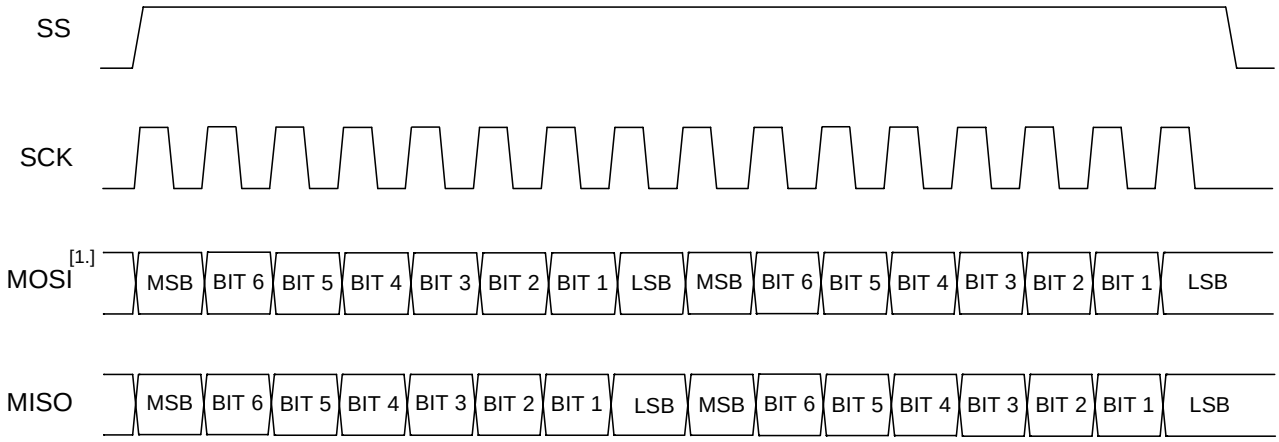


Figure 5-2. SPI Timing

Note:
1. Data lines do not three-state.

5.3 Serial EPROM Interface

5.3.1 Functional Description

When the CYWUSB6942 powers up, the firmware is loaded by the internal boot loader via a serial EPROM interface with the CYWUSB6942 being the master and the EPROM being the slave.

This is a four-pin interface that includes the $\overline{\text{EECS}}$ (Chip Select), EESCK (Serial Clock), EEMOSI (EPROM Serial output), and EEMISO (EPROM Serial input) pins.

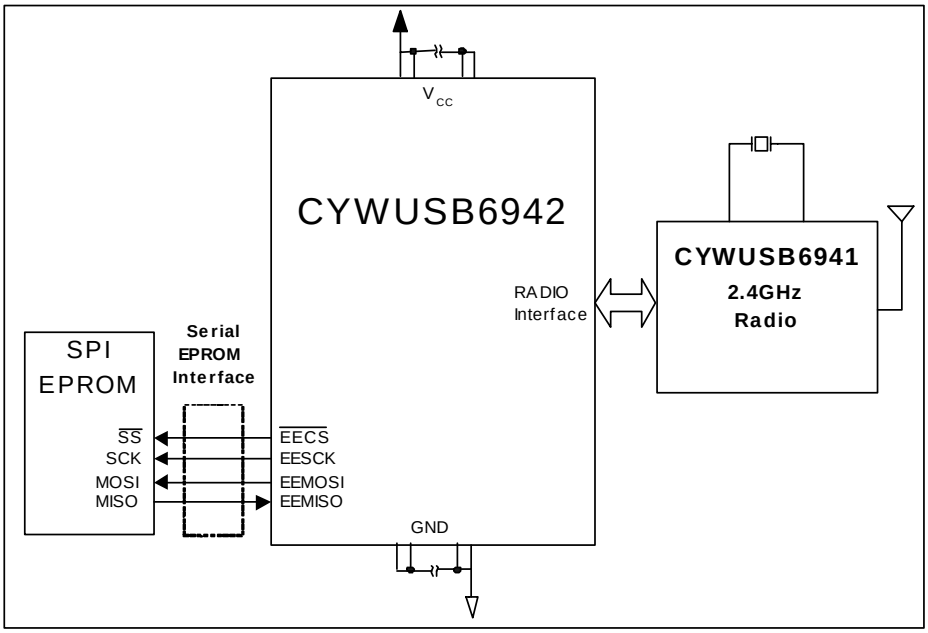
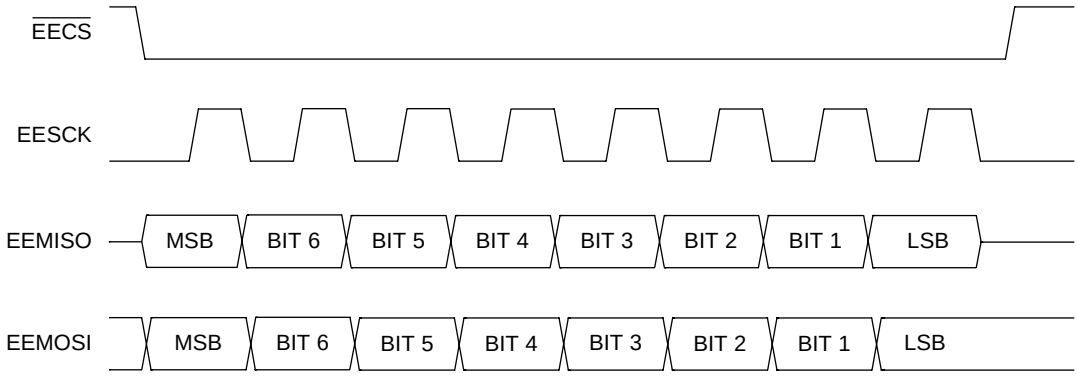


Figure 5-3. CYWUSB6942 Serial EPROM Interface Diagram

5.3.2 Serial EPROM Interface Signaling

The $\overline{\text{EECS}}$, EESCK, and EEMOSI signals are all driven by the CYWUSB6942 acting as a master, while the EPROM (slave) drives only the EEMISO signal. To initiate a byte transfer, the CYWUSB6942 asserts the $\overline{\text{EECS}}$ signal and provides the EESCK signal as a clock for the interface. The EEMOSI data is driven out by the CYWUSB6942 on the falling edge of $\overline{\text{SCK}}$ (the MSB is available on the falling edge of $\overline{\text{EECS}}$) and sampled by the EPROM on the rising edge of $\overline{\text{SCK}}$. The EEMISO data is driven out by the EPROM on the falling edge of EESCK and sampled by the CYWUSB6942 on the rising edge of EESCK. One bit is transferred per clock cycle, and one byte is transferred in a total of eight clock cycles. Once the transfer is complete, the CYWUSB6942 will drive the $\overline{\text{EECS}}$ pin high.



5.4 Interface for Wakeup and Sleep

Power management is crucial to preserving battery life for WirelessHID applications, and the CYWUSB6942 provides the flexibility of power control at the hardware level, offering a low-power standby/sleep mode.

To enable the low-power mode of this device, the external signal XTLEN must first be driven low. This will set up the low-power condition. Once the chip has set itself in a condition for low power, it will set the output signal BXTLEN to a low condition. This signals the chip is ready to have its clock stopped. The clock should then be stopped at a logic low.

6.0 CYWUSB6942 Pin Description

Table 6-1. Pin Description Table

Pin	Name	Type	Default	Description
Control Interface				
32	$\overline{\text{RESET}}$	Input	Z	**Active LOW Reset**. Resets the entire chip. This pin is normally tied to V_{CC} through a 10K resistor, and to GND through a 1-µF capacitor.
51	CLKOUT	O/Z	N/A	**CLKOUT** needs to be connected to **MODESEL**.
33	MODESEL	Input	Z	**MODESEL** must to be connected to either the input clock: **BCLK13M** or be driven by the base band's output clock: **CLKOUT**.
19	BCLK13M	Input	Z	**System Clock**. 13-MHz system clock.
35	XTLEN	Input	Z	**Crystal Oscillator Enable**. Enable signal for the clock. When XTLEN is deasserted the device goes into sleep mode.
Port A				
94	PA0	I/O/Z	Z	**Port A [5:0]** is a bidirectional I/O bus.
93	PA1	I/O/Z	Z	
88	PA2	I/O/Z	Z	
87	PA3	I/O/Z	Z	
84	PA4	I/O/Z	Z	
83	PA5	I/O/Z	Z	
Port B				
59	PB0	Output	Z	**Port B [12:0]**. This bus can be used to drive large pin-count applications (e.g., keyboard scan matrix).
58	PB1	Output	Z	
57	PB2	Output	Z	
56	PB3	Output	Z	
55	PB4	Output	Z	
54	PB5	Output	Z	
47	PB6	Output	Z	
46	PB7	Output	Z	
45	PB8	Output	Z	
44	PB9	Output	Z	
43	PB10	Output	Z	
42	PB11	Output	Z	
41	PB12	Output	Z	
Port C				
65	PC0	Output	0	**Port C[4:0]**. This bus can be used to drive large pin-count applications (e.g., keyboard scan matrix or control signal for optical mouse)
66	PC1	Output	0	
67	PC2	Output	0	
81	PC3	Output	0	
82	PC4	Output	0	
General Purpose Inputs/Slave Peripheral Interface (four wires)				
90	GPI0/SS	Input	Z	**GPI0**. General Purpose Input. **(Slave Select) Sync Clock**. Provides clock synchronization for the serial data transfer.
89	GPI1/$\overline{\text{SCK}}$	Input	Z	**GPI1**. General Purpose Input. **Serial Bit Clock**. Driven by the Serial interface master device.
91	MISO	Output	0	**MISO**. MISO is for a slave device to transmit data to a Serial Interface master device. On this bus, this chip is the slave device.

Table 6-1. Pin Description Table (continued)

Pin	Name	Type	Default	Description
92	MOSI	Input	Z	**MOSI**. MOSI is for a slave device to receive data from the Serial Interface master device. On this bus, this chip is the slave device.
38	GPI2	Input	Z	**GPI2**. General Purpose Input.
36	GPI3	Input	Z	**GPI3**. General Purpose Input.
37	GPI4	Input	Z	**GPI4**. General Purpose Input.
31	GPI5	Input	Z	**GPI5**. General Purpose Input.
Serial EPROM Interface				
60	$\overline{\text{EECS}}$ / PC5	Output	0	**Chip Select**. Chip select for EEPROM interface. **PC5**. Part of GPO block after reset boot process.
61	EESCK / PC6	Output	0	**Serial Clock**. Serial clock for EEPROM interface. **PC6**. Part of GPO block after reset boot process.
64	EEMISO / GPI6	Input	Z	**Serial Input**. Serial input for EEPROM interface. On this bus, this chip is the master device and the EEPROM is the slave device. **GPI6**. Part of GPI block after reset boot process.
34	EEMOSI / PC7	Output	0	**Serial Output**. Serial output for EEPROM interface. On this bus, this chip is the master device and the EEPROM is the slave device. **PC7**. Part of GPO block after reset boot process.
Radio Control Interface				
21	BTXD	Output	0	**Transmit Data**. Transmit data output port.
18	BRXD	Input	Z	**Receive Data**. Demodulated and sliced digital receive data.
17	BRCLK	Input	Z	**Transmit Clock**. 1 MHz clock associated with the transmit data.
15	BPAEN	Output	0	**Power Amplifier Enable**. Enables the PA in transmit mode. Active HIGH.
9	BRXEN	Output	Z	**Receive Circuitry Enable**. This signal enables the receive circuitry. Active HIGH.
22	BTXEN	Output	0	**Transmit Circuitry Enable**. This signal enables the transmit circuitry. Active HIGH.
20	BSEN	Output	0	**Synthesizer Enable**. This signal enables the hop synthesizer. Active HIGH.
14	$\overline{\text{BnPWR}}$	Output	$\overline{\text{RESET}}$	**Power On Reset**. This signal is active LOW.
24	BXTLEN	Output	1	**Crystal Oscillator Enable**. This signal enables the crystal oscillator or the external 13 MHz clock, if provided. Active HIGH.
16	Reserved	NC	N/A	No connect
Radio Serial Interface Pins				
12	BMOSI	Output	0	**Output Data**. This is the serial data output pin. On this bus, this chip is the master device.
11	BMISO	Input	Z	**Input Data**. This is the serial data input pin. On this bus, this chip is the master device.
10	BDCLK	Output	Z	**Output Clock**. This is the serial register clock.
13	BnDEN	Output	Z	**Enable**. This signal enables the serial communication.
Reserved Pins				
28	Reserved	Must be tied to GND.		
23	Reserved	NC	N/A	No connect
V_{CC} and GND pins				
8	V_{CC}	Power	N/A	**V_{CC} pins**. Power supply for digital logic.
29				
39				
52				
62				
85				
95				

Table 6-1. Pin Description Table (continued)

Pin	Name	Type	Default	Description
25	GND	Ground	N/A	**Ground pins**.
30				
40				
53				
63				
86				
96				
1	NC		N/A	**Not connected pins**.
2				
3				
4				
5				
6				
7				
26				
27				
48				
49				
50				
68				
69				
70				
71				
72				
73				
74	NC		N/A	**Not connected pins**.
75				
76				
77				
78				
79				
80				
97				
98				
99				
100				

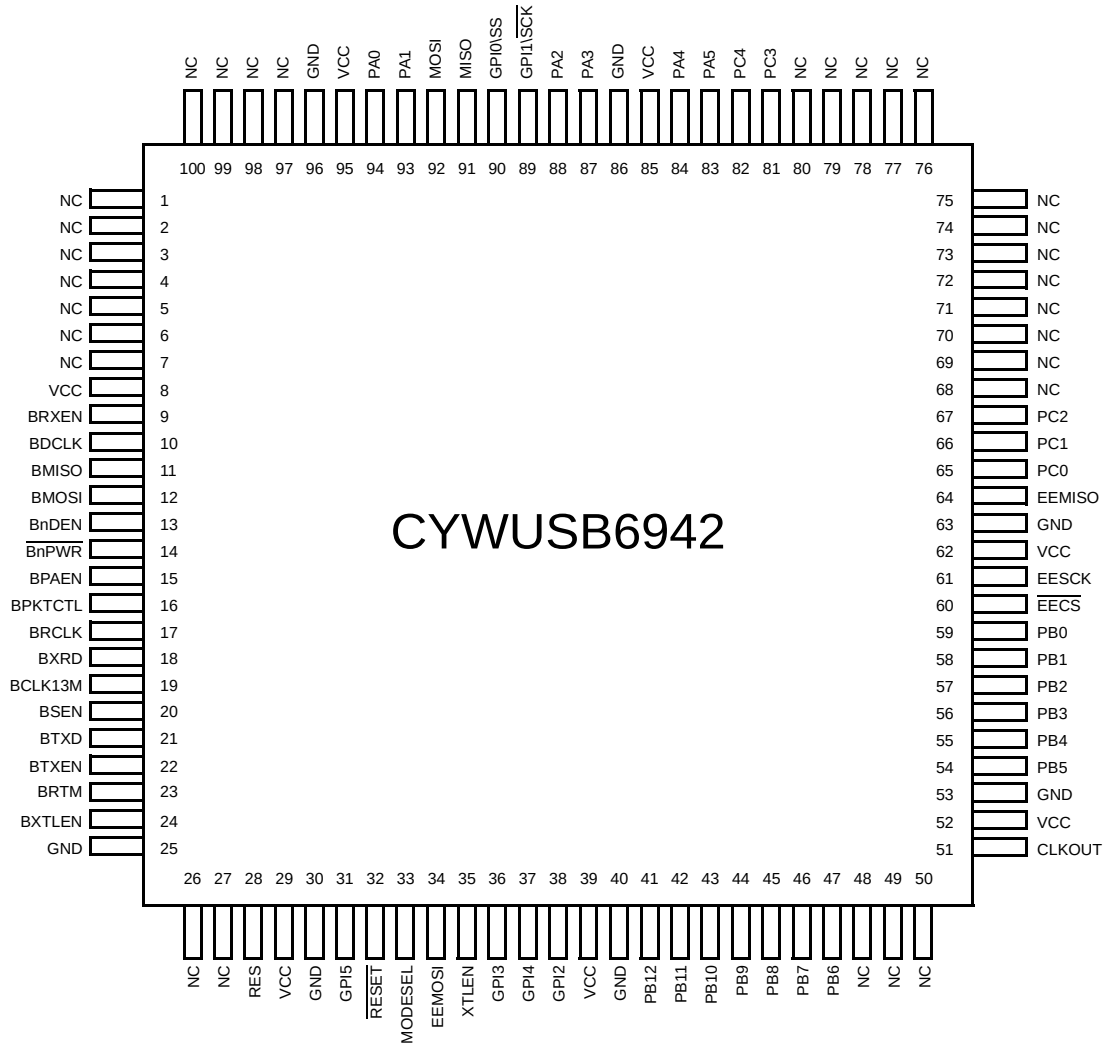


Figure 6-1. CYWUSB6942 100-pin TQFP Top View

7.0 Absolute Maximum Ratings

Storage Temperature .....–65°C to +150°C
Ambient Temperature with Power Applied.....–55°C to +125°C
Supply Voltage on V_{CC} relative to V_{SS}.....–0.3V to +3.9V
DC Input Voltage ..... –0.3V to V_{CC} + 0.3V
DC Voltage Applied to Outputs in High-Z State ..... –0.3V to V_{CC} + 0.3V
Static Discharge voltage (Digital)[2] ..... > 2000V
Latch-up current..... ± 200 mA

8.0 Operating Conditions

V_{CC} (Supply Voltage).....2.7V to 3.6V
T_A (Ambient Temperature Under Bias) .....0°C to +70°C
Ground Voltage..... 0V
F_{CLK} (BCLK13M)..... 13 MHz ± 20 ppm
..... duty cycle: 40% to 60%

9.0 DC Characteristics

DC Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		2.7		3.6	V
I_{CC}	Operating Supply Current			38	50	mA
I_{SB}	Low-power Mode Current			1.0	10.0	µA
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage		–0.3		0.8	V
I_I	Input Leakage Current	$0< V_{IN} < V_{CC}$	–1		+1	µA
V_{OH1}	Output Voltage High	I_{OH} = –100 µA	V_{CC} – 0.2			V
V_{OH2} [3.]	Output Voltage High	I_{OH} = –1.6 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL}= 1.6 mA			0.4	V
I_{OZ}	Output Leakage Current	$0 <= V_O <= V_{CC}$ Output Disabled	–1		+1	µA
C_{PIN}	Pin Capacitance				8	pF

Note:
2. Rating measured using the Human Body Model (HBM).
3. V_{OH2} applies to pins PC[4:0], EESI, EESCK, EECS_N, and X13OUT. All other output pins use V_{OH1}

10.0 Switching Characteristics

Table 10-1. CYWUSB6942 Switching Characteristics (Over the Operating Range)[4]

Parameter	Description	Min.	Typ.	Max.	Unit
SPI					
t_{SCK}	$\overline{SCK}$ frequency			1	MHz
t_{SCKH}	Minimum pulse width HIGH for $\overline{SCK}$	310			ns
t_{SCKL}	Minimum pulse width LOW for $\overline{SCK}$	155			ns
T_{SSS}	Slave Select Set-up Time before first positive edge of $\overline{SCK}$ edge	0			ns
T_{SSH}	Slave Select Hold Time after last negative edge of $\overline{SCK}$ edge	0			ns
T_{SSU}	Slave Input Data Set-up Time, data stable (on MOSI) before negative edge of $\overline{SCK}$	10			ns
T_{SHD}	Slave Input Data Hold Time, data stable (on MOSI) after negative edge of $\overline{SCK}$	5			ns
T_{SDO}	Slave Data Output Time from positive edge of $\overline{SCK}$ to data valid (on MISO)	285			ns
Serial EPROM Interface					
t_{EESCK}	$\overline{SCK}$ frequency			1	MHz
t_{EESCKH}	Minimum pulse width HIGH for EESCK	535			ns
t_{EESCKL}	Minimum pulse width LOW for EESCK	458			ns
T_{EESSS}	Slave Select Set-up Time before first EESCK edge	455			ns
T_{EESSH}	Slave Select Hold Time after last EESCK edge	-2			ns
T_{EESSU}	Slave Input Data Set-up Time, data stable (on EEMOSI) before positive edge of EESCK	12			ns
T_{EESHD}	Slave Input Data Hold Time, data stable (on EEMOSI) after positive edge of EESCK	0			ns
T_{EESDO}	Slave Data Output Time from positive edge of $\overline{SCK}$ to data valid (on EEMISO)	10			ns
Radio Serial Interface Pins					
t_{BDCLK}	Clock period	157			ns
t_{BDCLKH}	Clock minimum pulse width HIGH	73			
t_{BDCLKL}	Clock minimum pulse width LOW	73			
$t_{BMISOSU}$	Input Data Setup Time, data stable on BMISO to positive edge of BDCLK	55			
$t_{BMISOHD}$	Input Data Hold Time, data stable on BMISO from positive edge of BDCLK	0			
$t_{BnDENSDO}$	Data Output Time from negative edge of BDCLK to BnDEN Valid	5			
$t_{BMOSISDO}$	Data Output Time from negative edge of BDCLK to BMOSI Valid	5			
Power Management timing					
t_{R1C1}	Minimum $\overline{RESET}$ length (BCLK13M valid during this time)	100			µs

Note:
4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of10-pF load capacitance to ground.

11.0 Switching Waveforms

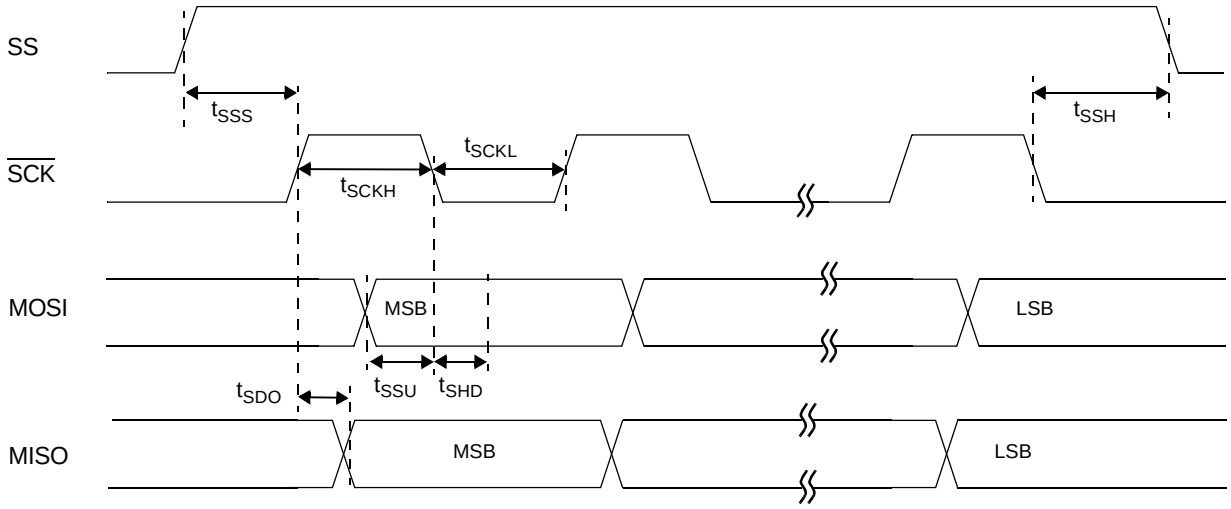


Figure 11-1. SPI Waveforms

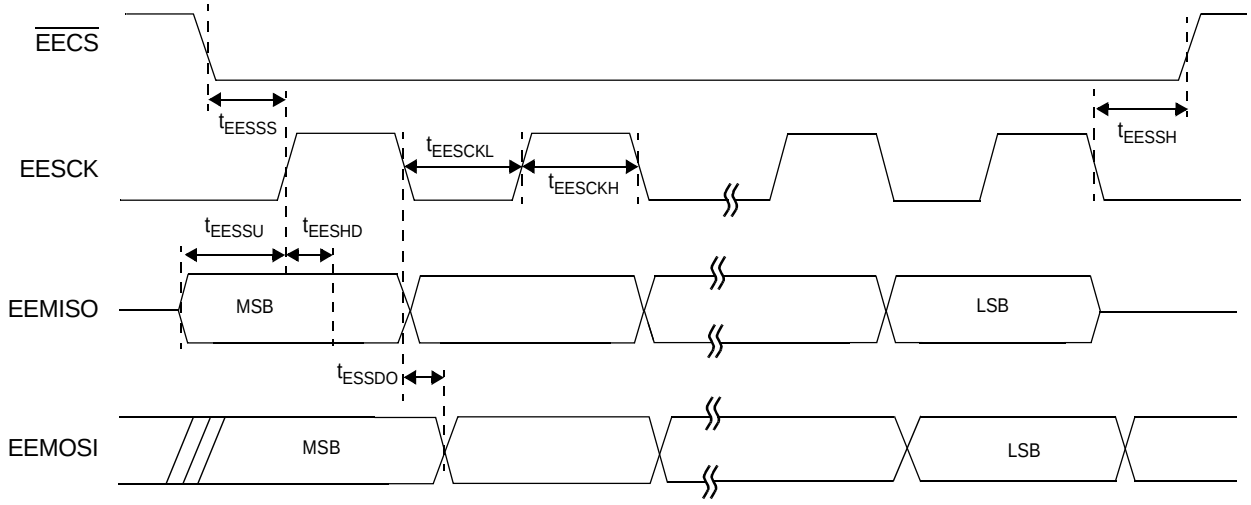


Figure 11-2. Serial EPROM Interface Waveforms

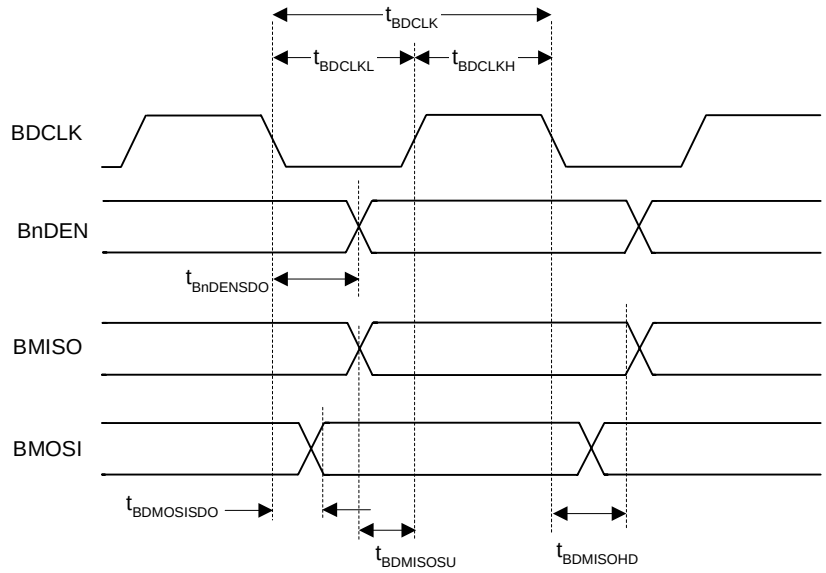


Figure 11-3. Radio Serial Interface

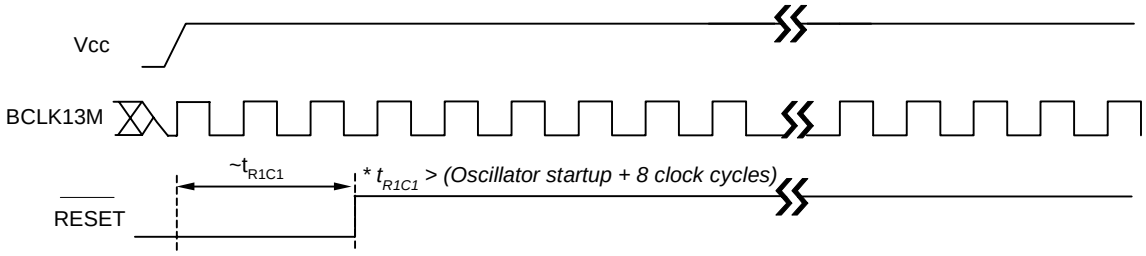
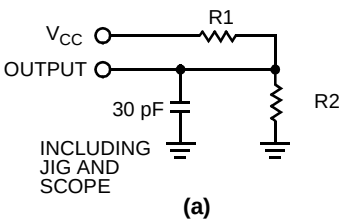
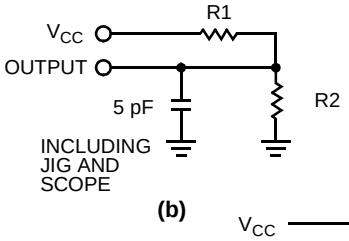


Figure 11-4. CYWUSB6942 Reset Timing

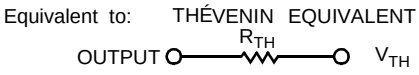
12.0 AC Test Loads and Waveforms for Digital Pins

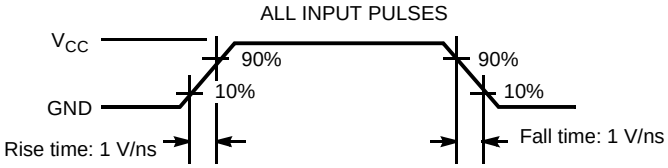


(a)



(b)





Parameter		Unit
R1	1071	Ω
R2	937	Ω
R_{TH}	500	Ω
V_{TH}	1.4	V
V_{CC}	3.00	V

13.0 Ordering Information

Part Number	Package Name	Package Type	Operating Range
CYWUSB6942-100AC	TQFP-A100	100-pin Thin Plastic Quad Flat Pack (14 × 14 × 1.0 mm)	Commercial

14.0 Package Diagrams

100-pin Thin Plastic Quad Flat Pack (TQFP) A100

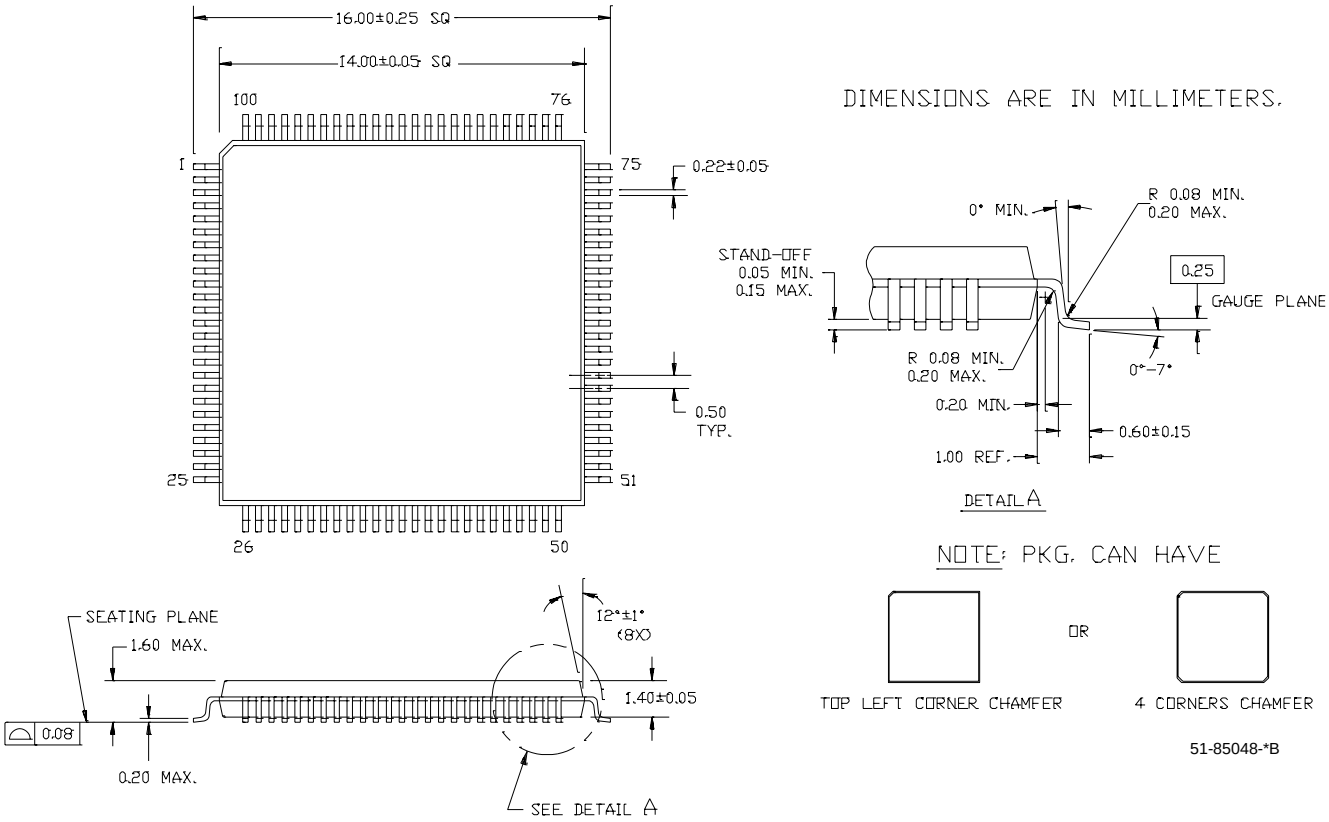


Figure 14-1. CYWUSB6942 100-pin TQFP Package Diagram

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Document History Page

Document Title: CYWUSB6942 WirelessUSB™ EX Baseband IC Document Number: 38-16005				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	122945	12/11/02	LXA	New Data Sheet
**A	124456	05/09/03	KKU	Removed application note material. Updated block diagrams, signal names, timing and characterization data.