



DAC0800/DAC0801/DAC0802 8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 V_{p-p} with simple resistor loads as shown in Figure 1. The reference-to-full-scale current matching of better than ± 1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than $\pm 0.1\%$ over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC} , grounded. Changing the V_{LC} potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full $\pm 4.5V$ to $\pm 18V$ power supply range; power dissipation is only 33 mW with $\pm 5V$ supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C, DAC0801C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, DAC-08E and DAC-08H, respectively.

Features

- Fast settling output current 100 ns
- Full scale error ± 1 LSB
- Nonlinearity over temperature $\pm 0.1\%$
- Full scale current drift ± 10 ppm/ $^{\circ}C$
- High output compliance $-10V$ to $+18V$
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range $\pm 4.5V$ to $\pm 18V$
- Low power consumption 33 mW at $\pm 5V$
- Low cost

Typical Applications

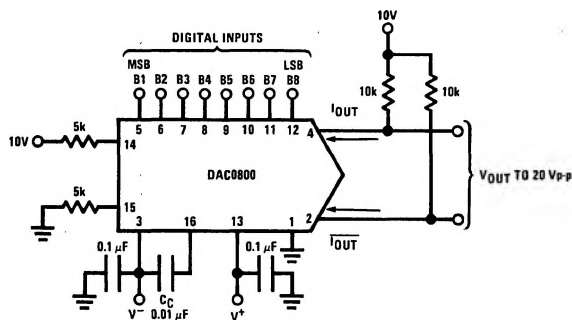


FIGURE 1. ± 20 V_{p-p} Output Digital-to-Analog Converter (Note 4)

TL/H/5686-1

Ordering Information

Non-Linearity	Temperature Range	Order Numbers				
		J Package (J16A)*	N Package (N16A)*	SO Package (M16A)		
$\pm 0.1\%$ FS	$0^{\circ}C \leq T_A \leq +70^{\circ}C$	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP	DAC0802LCM
$\pm 0.19\%$ FS	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	DAC0800LJ	DAC-08Q			
$\pm 0.19\%$ FS	$0^{\circ}C \leq T_A \leq +70^{\circ}C$	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM
$\pm 0.39\%$ FS	$0^{\circ}C \leq T_A \leq +70^{\circ}C$			DAC0801LCN	DAC-08CP	DAC0801LCM

*Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$) $\pm 18V$ or $36V$

Power Dissipation (Note 2) 500 mW

Reference Input Differential Voltage (V_{14} to V_{15}) V^- to V^+

Reference Input Common-Mode Range (V_{14} , V_{15}) V^- to V^+

Reference Input Current 5 mA

Logic Inputs V^- to V^- plus $36V$

Analog Current Outputs ($V_S = -15V$) 4.25 mA

ESD Susceptibility (Note 3) TBD V

Storage Temperature $-65^\circ C$ to $+150^\circ C$

Lead Temp. (Soldering, 10 seconds)

Dual-In-Line Package (plastic) $260^\circ C$

Dual-In-Line Package (ceramic) $300^\circ C$

Surface Mount Package

Vapor Phase (60 seconds) $215^\circ C$

Infrared (15 seconds) $220^\circ C$

Operating Conditions (Note 1)

	Min	Max	Units
Temperature (T_A)			
DAC0800L	-55	+125	$^\circ C$
DAC0800LC	0	+70	$^\circ C$
DAC0801LC	0	+70	$^\circ C$
DAC0802LC	0	+70	$^\circ C$

Electrical Characteristics

The following specifications apply for $V_S = \pm 15V$, $I_{REF} = 2$ mA and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and I_{OUT} .

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution Monotonicity Nonlinearity		8 8	8 8	8 8 ± 0.1	8 8	8 8	8 8 ± 0.19	8 8	8 8	8 8 ± 0.39	Bits Bits %FS
t_s	Settling Time	To $\pm 1/2$ LSB, All Bits Switched "ON" or "OFF", $T_A = 25^\circ C$ DAC0800L DAC0800LC		100	135		100 100	135 150		100	150	ns ns ns
t_{PLH} , t_{PHL}	Propagation Delay Each Bit All Bits Switched	$T_A = 25^\circ C$		35 35	60 60		35 35	60 60		35 35	60 60	ns ns
TCI_{FS}	Full Scale Tempco			± 10	± 50		± 10	± 50		± 10	± 80	ppm/ $^\circ C$
V_{OC}	Output Voltage Compliance	Full Scale Current Change $< 1/2$ LSB, $R_{OUT} > 20$ M Ω Typ	-10		18	-10		18	-10		18	V
I_{FS4}	Full Scale Current	$V_{REF} = 10.000V$, $R_{14} = 5.000$ k Ω $R_{15} = 5.000$ k Ω , $T_A = 25^\circ C$	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		± 0.5	± 4.0		± 1	± 8.0		± 2	± 16	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range	$V^- = -5V$ $V^- = -8V$ to $-18V$	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA mA
V_{IL} V_{IH}	Logic Input Levels Logic "0" Logic "1"	$V_{LC} = 0V$	2.0		0.8	2.0		0.8	2.0		0.8	V V
I_{iL} I_{iH}	Logic Input Current Logic "0" Logic "1"	$V_{LC} = 0V$ $-10V \leq V_{IN} \leq +0.8V$ $2V \leq V_{IN} \leq +18V$		-2.0 0.002	-10 10		-2.0 0.002	-10 10		-2.0 0.002	-10 10	μA μA
V_{IS}	Logic Input Swing	$V^- = -15V$	-10		18	-10		18	-10		18	V
V_{THR}	Logic Threshold Range	$V_S = \pm 15V$	-10		13.5	-10		13.5	-10		13.5	V
I_{15}	Reference Bias Current			-1.0	-3.0		-1.0	-3.0		-1.0	-3.0	μA
di/dt	Reference Input Slew Rate	(Figure 12)	4.0	8.0		4.0	8.0		4.0	8.0		mA/ μs
$PSSI_{FS+}$	Power Supply Sensitivity	$4.5V \leq V^+ \leq 18V$		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$		$-4.5V \leq V^- \leq 18V$ $I_{REF} = 1$ mA		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
I^+ I^-	Power Supply Current	$V_S = \pm 5V$, $I_{REF} = 1$ mA		2.3 -4.3	3.8 -5.8		2.3 -4.3	3.8 -5.8		2.3 -4.3	3.8 -5.8	mA mA
I^+ I^-		$V_S = 5V$, $-15V$, $I_{REF} = 2$ mA		2.4 -6.4	3.8 -7.8		2.4 -6.4	3.8 -7.8		2.4 -6.4	3.8 -7.8	mA mA
I^+ I^-		$V_S = \pm 15V$, $I_{REF} = 2$ mA		2.5 -6.5	3.8 -7.8		2.5 -6.5	3.8 -7.8		2.5 -6.5	3.8 -7.8	mA mA

Electrical Characteristics (Continued)

The following specifications apply for $V_S = \pm 15V$, $I_{REF} = 2\text{ mA}$ and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
P_D	Power Dissipation	$\pm 5V$, $I_{REF} = 1\text{ mA}$		33	48		33	48		33	48	mW
		$5V$, $-15V$, $I_{REF} = 2\text{ mA}$		108	136		108	136		108	136	mW
		$\pm 15V$, $I_{REF} = 2\text{ mA}$		135	174		135	174		135	174	mW

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

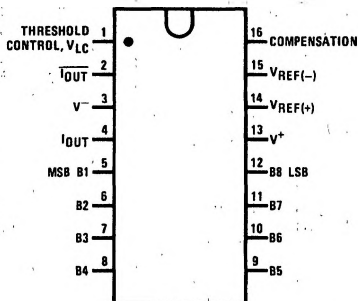
Note 2: The maximum junction temperature of the DAC0800, DAC0801 and DAC0802 is 125°C . For operating at elevated temperatures, devices in the Dual-In-Line J package must be derated based on a thermal resistance of 100°C/W , junction-to-ambient, 175°C/W for the molded Dual-In-Line N package and 100°C/W for the Small Outline M package.

Note 3: Human body model, 100 pF discharged through a $1.5\text{ k}\Omega$ resistor.

Note 4: Pin-out numbers for the DAC080X represent the Dual-In-Line package. The Small Outline package pin-out differs from the Dual-In-Line package.

Connection Diagrams

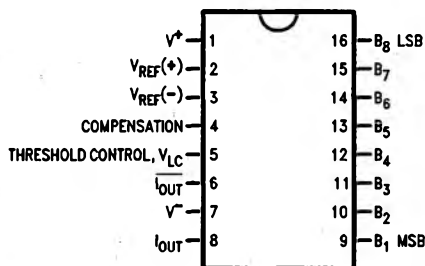
Dual-In-Line Package



Top View

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Small Outline Package

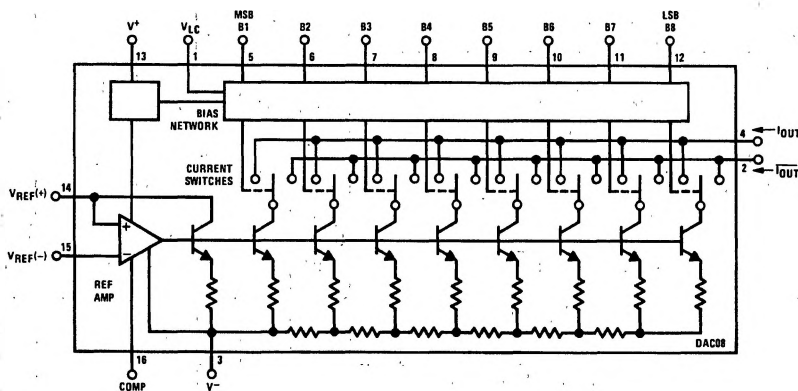


Top View

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See Ordering Information

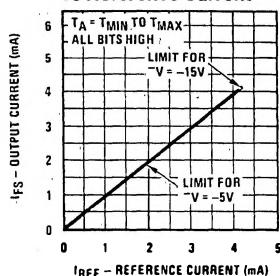
Block Diagram (Note 4)



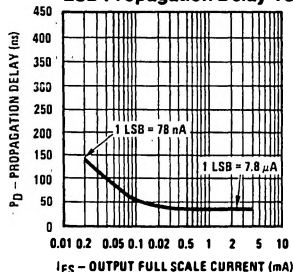
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Typical Performance Characteristics

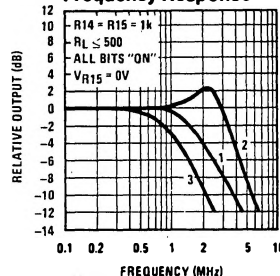
Full Scale Current vs Reference Current



LSB Propagation Delay Vs IFS



Reference Input Frequency Response

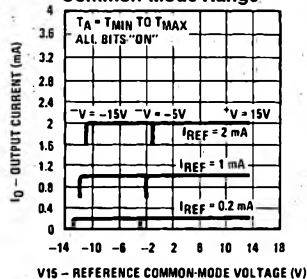


Curve 1: $C_C = 15$ pF, $V_{IN} = 2$ Vp-p centered at 1V.

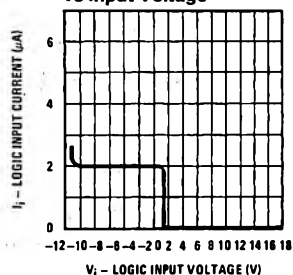
Curve 2: $C_C = 15$ pF, $V_{IN} = 50$ mVp-p centered at 200 mV.

Curve 3: $C_C = 0$ pF, $V_{IN} = 100$ mVp-p at 0V and applied through 50Ω connected to pin 14.2V applied to R14.

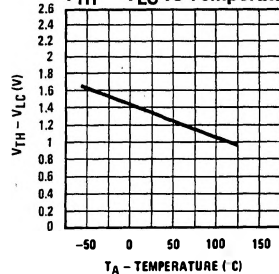
Reference Amp Common-Mode Range



Logic Input Current vs Input Voltage

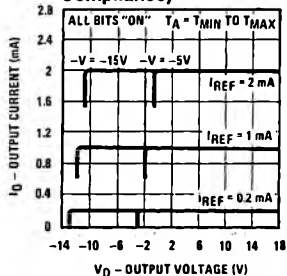


VTH - VLC vs Temperature

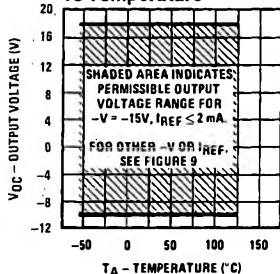


Note. Positive common-mode range is always $(V+) - 1.5V$.

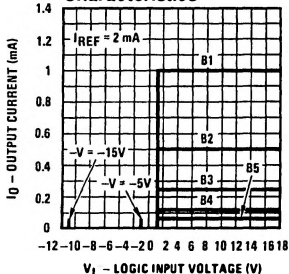
Output Current vs Output Voltage (Output Voltage Compliance)



Output Voltage Compliance vs Temperature



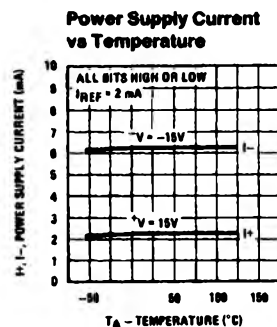
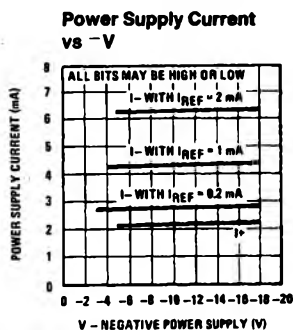
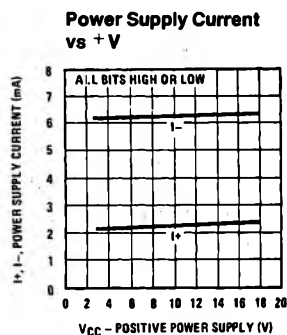
Bit Transfer Characteristics



TL/H/5686-3

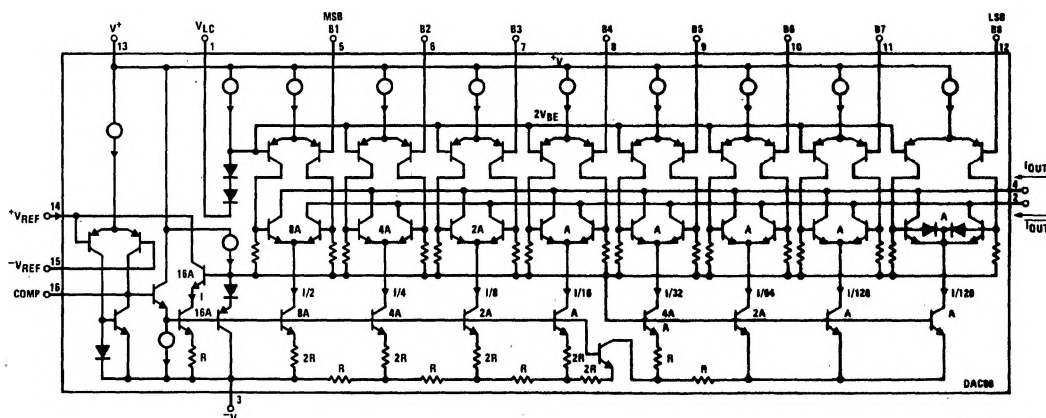
Note. B1-B8 have identical transfer characteristics. Bits are fully switched with less than $1/4$ LSB error, at less than ± 100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range ($V_{LC} = 0V$).

Typical Performance Characteristics (Continued)



TL/H/5686-4

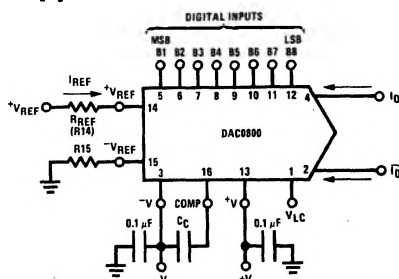
Equivalent Circuit



TL/H/5686-15

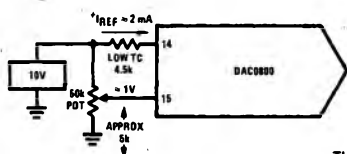
FIGURE 2

Typical Applications (Continued)



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FIGURE 3. Basic Positive Reference Operation (Note 4)



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FIGURE 4. Recommended Full Scale Adjustment Circuit (Note 4)

$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$$I_O + I_{O-} = I_{FS} \text{ for all logic states}$$

For fixed reference, TTL operation,

typical values are:

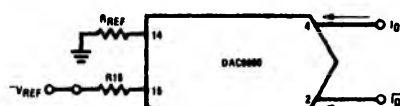
$$V_{REF} = 10.000V$$

$$R_{REF} = 5.000k$$

$$R15 \approx R_{REF}$$

$$C_C = 0.01 \mu F$$

$$V_{LC} = 0V \text{ (Ground)}$$



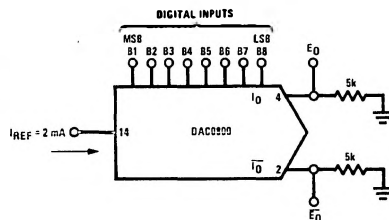
TL/H/5686-16

$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note. R_{REF} sets I_{FS} ; $R15$ is for bias current cancellation

FIGURE 5. Basic Negative Reference Operation (Note 4)

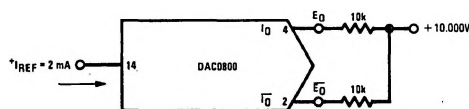
Typical Applications (Continued)



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	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\bar{I}_O$ mA	E_O	$\bar{E}_O$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	0.000
Full Scale - LSB	1	1	1	1	1	1	1	0	1.984	0.008	-9.920	-0.040
Half Scale + LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half Scale - LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

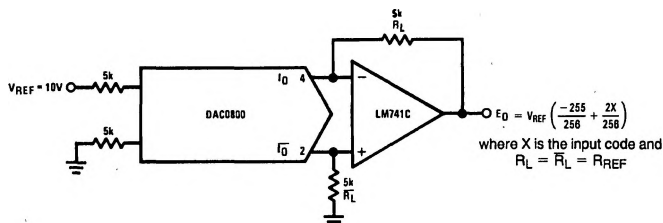
FIGURE 6. Basic Unipolar Negative Operation (Note 4)



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	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\bar{E}_O$
Pos. Full Scale	1	1	1	1	1	1	1	1	-9.920	+10.000
Pos. Full Scale - LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale - LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	-9.920

FIGURE 7. Basic Bipolar Output Operation (Note 4)



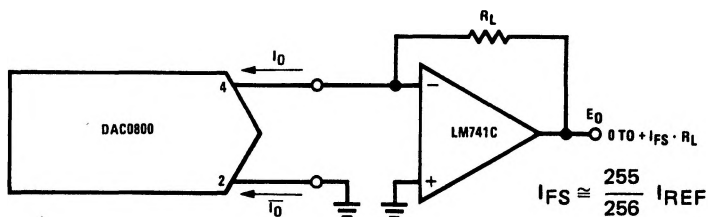
TL/H/5686-18

If $R_L = \bar{R}_L$ within $\pm 0.05\%$, output is symmetrical about ground

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.960
Pos. Full Scale - LSB	1	1	1	1	1	1	1	0	+9.880
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(-)Zero Scale	0	1	1	1	1	1	1	1	-0.040
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	-9.880
Neg. Full Scale	0	0	0	0	0	0	0	0	-9.960

FIGURE 8. Symmetrical Offset Binary Operation (Note 4)

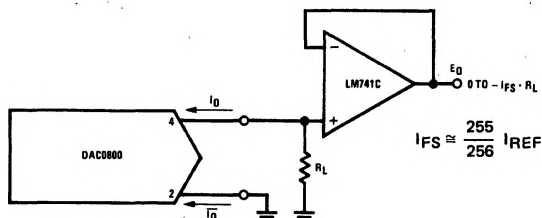
Typical Applications (Continued)



TL/H/5686-19

For complementary output (operation as negative logic DAC), connect inverting input of op amp to I_O (pin 2), connect I_O (pin 4) to ground.

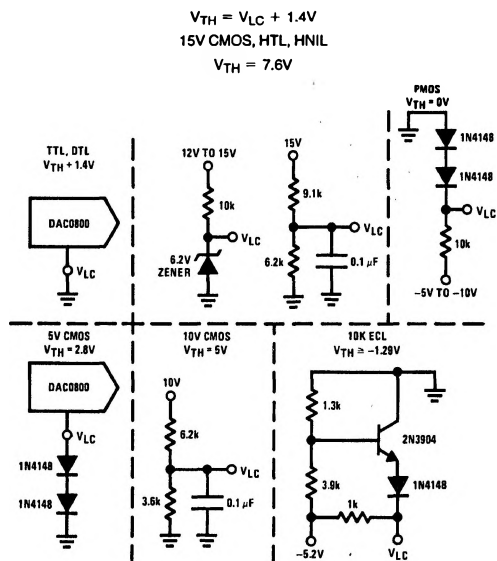
FIGURE 9. Positive Low Impedance Output Operation (Note 4)



TL/H/5686-20

For complementary output (operation as a negative logic DAC) connect non-inverting input of op amp to I_O (pin 2); connect I_O (pin 4) to ground.

FIGURE 10. Negative Low Impedance Output Operation (Note 4)



Note. Do not exceed negative logic input range of DAC.

FIGURE 11. Interfacing with Various Logic Families

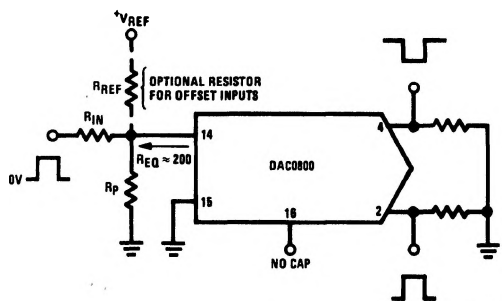
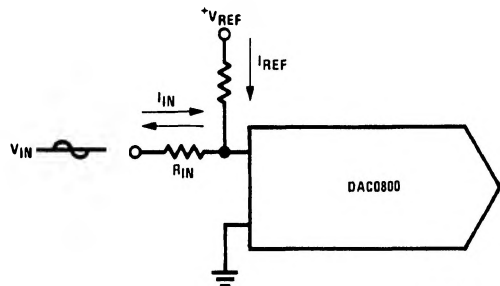


FIGURE 12. Pulsed Reference Operation (Note 4)

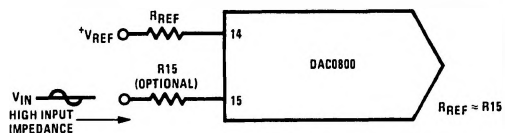
Typical Applications (Continued)

(a) $I_{REF} \geq \text{peak negative swing of } I_{IN}$



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(b) $+V_{REF}$ must be above peak positive swing of V_{IN}



TL/H/5686-12

FIGURE 13. Accommodating Bipolar References (Note 4)

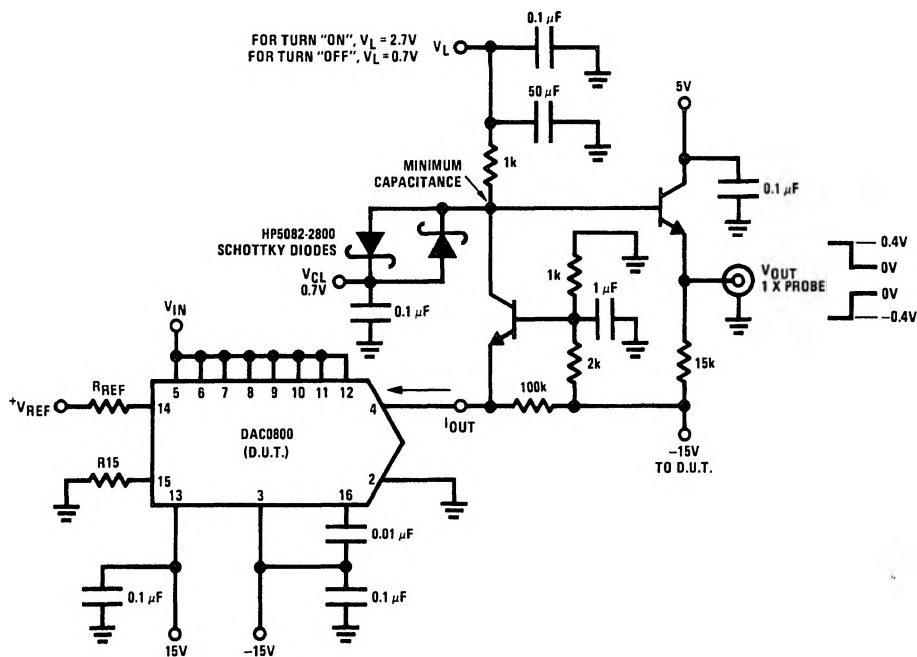


FIGURE 14. Settling Time Measurement (Note 4)

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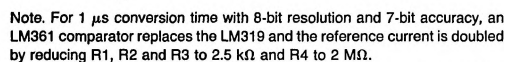


FIGURE 15. A Complete 2 μ s Conversion Time, 8-Bit A/D Converter (Note 4)

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