BURR-BROWN®

DAC1204/1214

**PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE**

QUAD Monolithic 12-Bit DIGITAL-TO-ANALOG CONVERTER (Serial Interface)

FEATURES

- **QUAD MONOLITHIC 12-BIT DAC**
  - **Current Output: 1mA Span**
  - **Minimal External Components Required; One Op Amp Only**
  - **Internal Feedback Resistor (R_{FB}) for External I/V Amp Trimmed at Wafer Level;**
    - **DAC1204: V_{OUT} = ±10V**
    - **DAC1214: V_{OUT} = ±5V, 0 to 10V**
  - **Internal High Stability Voltage Reference**
- **HIGH SPEED SERIAL INTERFACE: 10MHz Clock**
- **FOUR DACs SIMULTANEOUS UPDATE FUNCTION: Available Individual Updating**
- **PROGRAMMABLE FUNCTION FOR BIPOLAR/UNIPOLAR OUTPUT SELECT**
- **CLEAR FUNCTION FOR RESET TO OUTPUT ZERO**
- **SINGLE +5V SUPPLY**
- **28-PIN SOIC**

APPLICATIONS

- **MOTOR CONTROL**
- **ATE PIN-ELECTRONICS LEVEL SETTING**
- **PROCESS CONTROL**
- **AUTO CALIBRATION CIRCUIT**
- **DSP PROCESSOR BOARD**
- **UPGRADE REPLACEMENT FOR MULTIPLYING DAC**

DESCRIPTION

The DAC1204 and DAC1214 are serial interface, quad 12-bit current output digital-to-analog converters. These DACs consist of four separate DACs with high stability feedback resistors, a high-stability bandgap reference and a 16-bit serial-to-parallel register which is followed by four separate double-buffered registers on a single monolithic chip. The optimum performance is achieved from a combination of state-of-the art Bi CMOS process and advanced laser trimming technology.

The current output stage of the DAC1204 and DAC1214 has a pair of feedback resistors which are trimmed at wafer level. The feedback resistors of the DAC1204 are specified for ±10V output range, while the later is specified for ±5V (or 0 to 10V) output range. Thus the external I/V converter is possible with only one op amp for both bipolar and unipolar output range.

The DAC1204 and DAC1214 have a high speed serial interface capable of clocking in data at a rate of 10MHz. The serial data is a 16-bit word including channel address bits, output mode select (bipolar or unipolar mode) bits and actual DAC data. Serial data is clocked into the 16-bit shift register (MSB first) then latched into the DAC's first register. All DAC analog outputs can be simultaneously updated using asynchronous load (LOAD) signal. Also, DAC registers can be updated independently. These DACs have an asynchronous clear (CLR) control for reset to bipolar zero or unipolar zero depending on the output mode selected. This feature is useful for power-on-reset or system calibration.

All digital pins are CMOS/TTL compatible. Power supply voltage is +5VDC. The DAC1204 and DAC1214 are available in 28 pin plastic SOIC package.

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SPECIFICATIONS

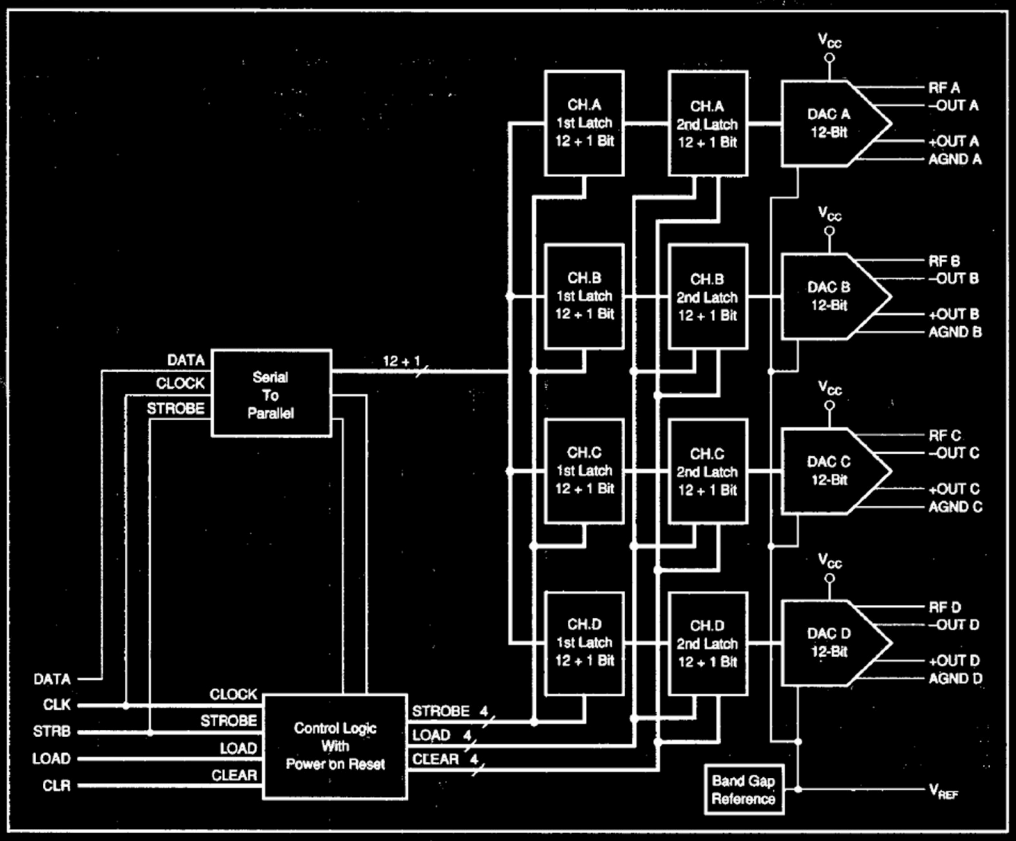
ELECTRICAL

T_A = 25°C, V_{CC} = V_{DD} = 5.0V, V_{REF} = internal or external 2.500V, with external I/V amp using internal feedback resistor and suitable op-amp unless otherwise noted.

	DAC1204U, DAC1214U			DAC1204UB, DAC1214UB			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DIGITAL INPUT							
Resolution		12			*		Bits
Digital Input Voltage							
V_{IH}	2.0		5.0	*		*	V
V_{IL}	0		0.8	*		*	V
Digital Input Current							
I_{IH} at V_{IH} = 5V			10			*	µA
I_{IL} at V_{IL} = 0V			100			*	µA
Maximum Input Clock Frequency	10			*			MHz
Input Pulse Width							
T_{WH}(1)	40			*			ns
T_{WL}(1)	40			*			ns
Input Set-up Time(1)			20			*	ns
Input Hold Time(1)			20			*	ns
TRANSFER CHARACTERISTICS							
DC ACCURACY							
Integral Linearity Error	–1.0		+1.0	–0.5		+0.5	LSB
Differential Linearity Error	–1.0		+1.0	–0.5		+0.5	LSB
Gain Error(2)	–8.0		+8.0	–4.0		+4.0	LSB
Bipolar Zero Error(2)	–4.0		+4.0	–2.0		+2.0	LSB
Unipolar Zero Error(2) (DAC1214 Only)	–2.0		+2.0	–1.0		+1.0	LSB
Monotonicity (0 to 70°C)		Guaranteed			Guaranteed		
MISMATCH AMONG CHANNELS							
Integral Linearity Error		1.0	TBD		0.5	TBD	LSB
Differential Linearity Error		1.0	TBD		0.5	TBD	LSB
Gain Error(2)		8.0	TBD		4.0	TBD	LSB
Bipolar Zero Error(2)		4.0	TBD		2.0	TBD	LSB
Unipolar Zero Error(2) (DAC1214 Only)		2.0	TBD		1.0	TBD	LSB
DRIFT (0 to 70°C)							
Gain Drift(2) with External V_{REF}		±10	TBD		*	TBD	ppm/°C
Gain Drift(2) with Internal V_{REF}		±25	TBD		*	TBD	ppm/°C
Bipolar Zero Drift(2) with External/Internal V_{REF}		±5	TBD		*	TBD	ppm FSR/°C
Unipolar Zero Drift(2) with External/Internal V_{REF} (DAC1214 Only)		±5	TBD		*	TBD	ppm FSR/°C
AC PERFORMANCE							
Settling Time; (to 0.012% of FSR, Load to I_{OUT})		500			*		ns
Glitch Energy(3)		20			*		nV-s
Crosstalk:(3)							
Digital-to-Analog		20			*		nV-s
Channel-to-Channel		–78			*		dB
REFERENCE							
External Reference Voltage Range	2.45	2.50	2.55	*	*	*	V
External Reference Current Drain at V_{REF} = 2.500V		±10	±50		*	*	µA
ANALOG OUTPUT							
Voltage Output Configuration							
Bipolar Range							
DAC1204		±10			*		V
DAC1214		±5			*		V
Unipolar Range							
DAC1214		0 to +10			*		V
Output Impedance at Output to Ground		1.0			*		kΩ
Short Circuit Duration		Indefinite to Ground			*		
POWER SUPPLY REQUIREMENTS							
Supply Voltage							
V_{CC}, V_{DD}	4.75	5.00	5.25	*	*	*	V
Supply Current (No Load)							
I_{CC} + I_{DD} (V_{CC} = V_{DD} = 5.0V)		20	TBD		*	*	mA
Power Dissipation		100	TBD		*	*	mW
Power Supply Rejection Ratio(2)		±0.001			*		% of FSR/% V_{CC}
TEMPERATURE RANGE							
Specification	0		70	*		*	°C
Operating	–40		+85	*		*	°C
Storage	–55		+125	*		*	°C

NOTES: (1) See serial interface timing for details. (2) Offset, linearity and CMRR of external Op-Amp influence each performance. (3) Specified condition (Clock/Signal frequency, Op-Amp, Band-Width, etc.) should be determined.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND	0 to +6V
V_{CC} to AGND	0 to +6V
AGND to DGND	±0.3V
Digital Input to DGND	–0.3V to +V_{DD} +0.3V
External Voltage applied to:	
Internal Feed-back Resistor	±25V
$V_{REF\ IN}$	–0.3V to V_{CC} +0.3V
–Out/+Out	–0.3V to V_{CC} +0.3V
Lead Temperature; (soldering, 5s)	+260°C
(reflow, 10s)	+235°C
Max Junction Temperature	+125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	OUTPUT RANGE	LINEARITY ERR	PACKAGE
DAC1204U	±10V	±1LSB	28-Pin SOIC
DAC1204UB	±10V	±0.5LSB	28-Pin SOIC
DAC1214U	±5V, 0 to 10V	±1LSB	28-Pin SOIC
DAC1214UB	±5V, 0 to 10V	±0.5LSB	28-Pin SOIC

PACKAGE INFORMATION[1]

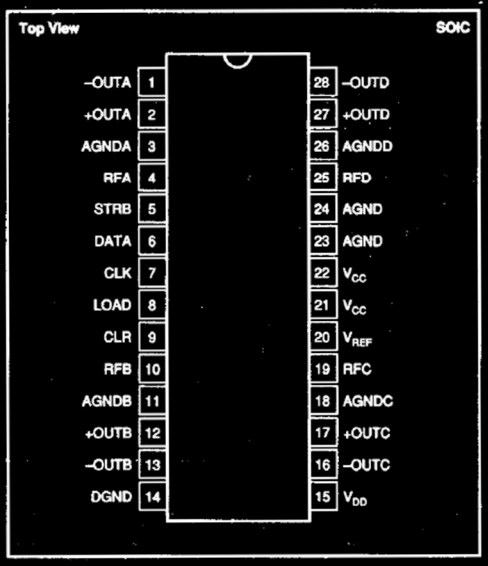
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DAC1204U, UB	28-Pin SOIC	809
DAC1204UB	28-Pin SOIC	809
DAC1214U	28-Pin SOIC	809
DAC1214UB	28-Pin SOIC	809

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	–OUTA	DAC A Current Output.
2	+OUTA	DAC A Common Current Output.
3	AGNDA	DAC A Analog Ground.
4	RFA	DAC A Feed-back Resistor.
5	STRB	1st Latch Register Update. Data is latched in on negative edge.
6	DATA	Serial Data Input. Data is clocked in on positive edge of the CLK.
7	CLK	Serial Clock Input.
8	LOAD	Load DAC Input (active low) - 2nd Latch Register Update.
9	CLR	Reset to DAC Output zero (active low).
10	RFB	DAC B Feed-back Resistor.
11	AGNDB	DAC B Analog Ground.
12	+OUTB	DAC B Common Current Output.
13	–OUTB	DAC B Current Output.
14	DGND	Digital Ground.
15	V_{DD}	Digital Power Supply, +5V typ.
16	–OUTC	DAC C Current Output.
17	+OUTC	DAC C Common Current Output.
18	AGNDC	DAC C Analog Ground.
19	RFC	DAC C Feed-back Resistor.
20	V_{REF}	Reference Voltage Input.
21	V_{CC}	Analog Power Supply, +5V typ.
22	V_{CC}	Analog Power Supply, +5V typ.
23	AGND	Analog Power Ground.
24	AGND	Analog Power Ground.
25	RFD	DAC D Feed-back Resistor.
26	AGNDD	DAC D Analog Ground.
27	+OUTD	DAC D Common Current Output.
28	–OUTD	DAC D Current Output.

PIN CONNECTIONS



DIGITAL INPUTS DESCRIPTION

INPUT CODES

All digital inputs are TTL and CMOS compatible. For bipolar output range, input codes for the DAC1204 and DAC1214 are Binary Two's Compliment (BTC) code. For unipolar output range, input codes are Unipolar Straight Binary (USB) code. The input/output relationship is shown in Table Ia and Ib.

DIGITAL INPUT CODE (BTC)	ANALOG OUTPUT (BIPOLAR)
$7FF_{HEX}$	+FS
000_{HEX}	BPZ
FFF_{HEX}	BPZ –1LSB
800_{HEX}	–FS

TABLE Ia. Digital Input/Bipolar Output Relationships.

DIGITAL INPUT CODE (USB)	ANALOG OUTPUT (UNIPOLAR)
FFF_{HEX}	FS
800_{HEX}	FS/2
$7FF_{HEX}$	FS/2 –1LSB
000_{HEX}	ZERO

TABLE Ib.Digital Input/Unipolar Output Relationships.

SERIAL INPUT DATA FORMAT

Serial data is a 16-bit word per channel and is clocked in on the raising edge of clock (CLK) into the internal 16-bit shift register with MSB first format. Figure 1 shows the serial data input format. The 16-bit serial input format comprises two DAC address bits (A1, A0), two output mode select bits (M1, M0) and twelve bits of DAC data (D11...D00). A1 and A0 shown in Table IIa set the DAC address, and M1 and M0 shown in Table IIb select the output range of bipolar or unipolar.

A1	A0	SELECTED DAC
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

TABLE IIa. DAC Address.

M1	M0	DAC OUTPUT MODE
0	0	Bipolar Output
0	1	Unipolar Output
1	X	Reserved
NOTES: 0 = logical "Low", 1 = logical "High", X = Don't Care.		

TABLE IIb. DAC Output Mode Select.

DIGITAL INTERFACE TIMING

Interface logic signals of the DAC1204 and DAC1214 consist of the serial data clock (CLK), serial data (DATA), strobe (STRB), load (LOAD) and clear (CLR) controls. Figure 2 shows a typical interface timing diagram. The serial data is clocked in on positive edge of CLK into the shift register until all 16 bits of data are entered and then is transferred into the addressed DAC first latch register from the shift register on negative edge of STRB. The DAC data is allowed to stay in each first register until each first latch register is updated by next STRB signal. Also the STRB signal and DAC address bits (A0, A1) on serial data frame with LOAD signal allow DAC update; independently or simultaneously. The STRB signal must be "High" for at least one clock cycle before going "Low" and must be held "Low" for at least one cycle after the signal is changed from "High" to "Low" as shown in Figure 2.

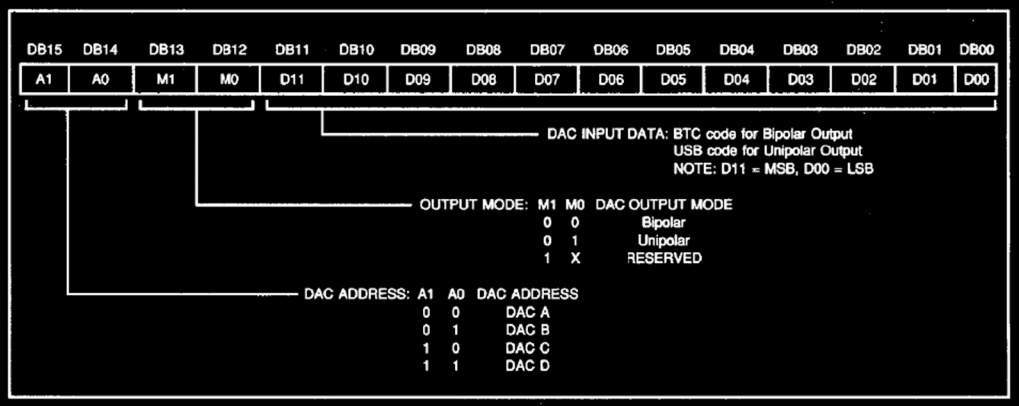


FIGURE 1. Serial Input Data Format.

LOAD signal is asynchronous with respect to DATA, CLK and STRB signals and can simultaneously update all four DAC second latch registers. When LOAD signal is changed "High" to "Low", the data on all first latch registers are loaded into corresponding second latch registers and DAC's outputs are updated simultaneously. This mode is a Latch Mode. In this case, if the LOAD signal become "Low" within two clocks from the negative edge of STRB signal, the previous data of first latch register is loaded into the second latch register. If LOAD signal is fixed "Low", the data on the first latch register addressed by A1, A0 is loaded into corresponding second latch register on second negative edge of CLK after STRB goes "Low", and in this case, DAC's output can be updated independently. This is a Transparent Mode.

CLR signal, also, is asynchronous with respect to DATA, CLK, STRB signals and can simultaneously reset to bipolar zero or unipolar zero depending on the output mode selected (M_0, M_1) when the CLR is "Low".

CIRCUIT CONNECTION

Figure 3 shows a typical connection diagram for the DAC1204 and DAC1214. The output stage of the DAC1204 and DAC1214 is current output mode.

For optimum performance and noise rejection, the DACs and I/V op amp should be located close to each other and power supply decoupling capacitors should be located close to the DACs.

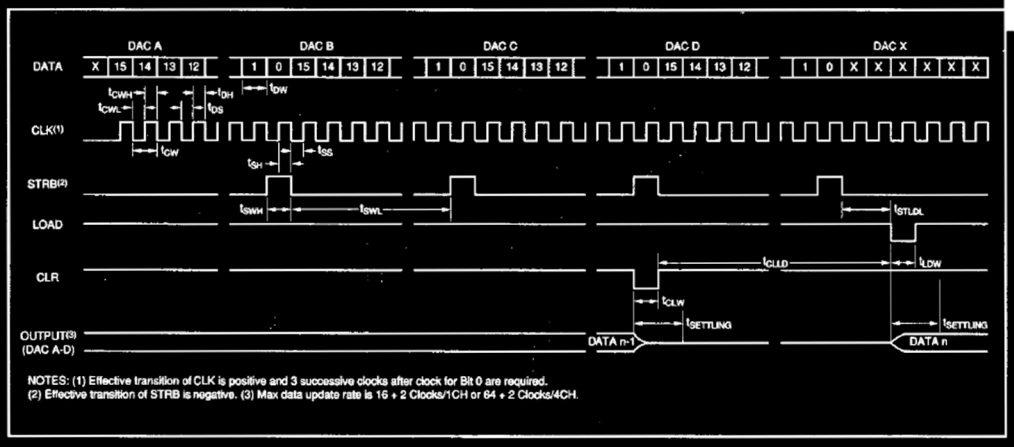


FIGURE 2a. Serial Interface Timing Diagram (Latch Mode).

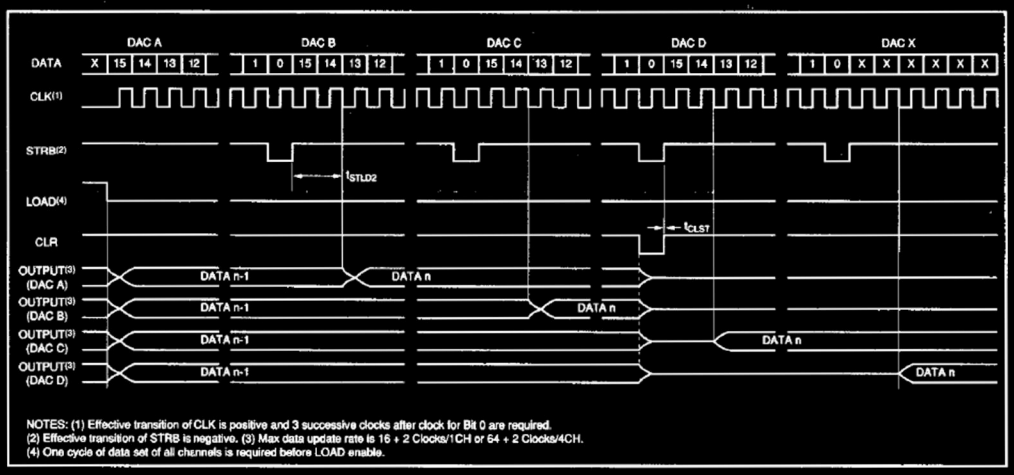


FIGURE 2b. Serial Interface Timing Diagram (Transparent Mode).

TIMING SPECIFICATION

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CW}	CLOCK (CLK) width	100			ns
t_{CWL}	CLOCK (CLK) low width	40			ns
t_{CWH}	CLOCK (CLK) high width	40			ns
t_{SWL}	STROBE (STRB) low width	1			CLOCK
t_{SWH}	STROBE (STRB) high width	1			CLOCK
t_{DW}	DATA (DATA) width	100			ns
t_{LDW}	LOAD (LOAD) low width	40			ns
t_{CLW}	CLEAR (CLR) low width	40			ns
t_{DS}	DATA (DATA) to CLOCK (CLK) set-up time	20			ns
t_{DH}	DATA (DATA) to CLOCK (CLK) hold time	20			ns
t_{SS}	STROBE (STRB) to CLOCK (CLK) set-up time	20			ns
t_{SH}	STROBE (STRB) to CLOCK (CLK) hold time	20			ns
t_{STLD1}	STROBE (STRB) to LOAD (LOAD) delay time for latch mode	2.5			CLOCK
t_{STLD2}	STROBE (STRB) to LOAD (LOAD) delay time for transparent mode			2.5	CLOCK
t_{CLLD}	CLEAR (CLR) to LOAD (LOAD) delay time	100			ns
t_{CLST}	CLEAR (CLR) to STROBE (STRB) delay time	0			ns

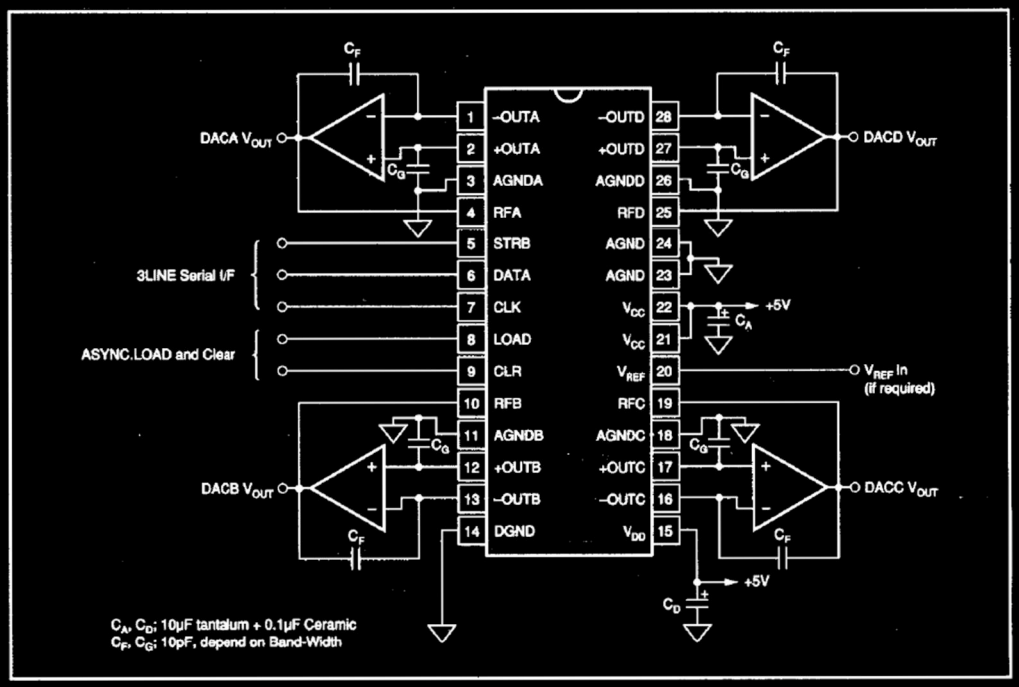


FIGURE 3. Typical I/V Amp Connection.