National Semiconductor

MICRO-DAC™ DAC1208/DAC1209/DAC1210/DAC1230/ DAC1231/DAC1232 12-Bit, μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1208 and the DAC1230 series are 12-bit multiplying D to A converters designed to interface directly with a wide variety of microprocessors (8080, 8048, 8085, Z-80, etc.). Double buffering input registers and associated control lines allow these DACs to appear as a two-byte "stack" in the system's memory or I/O space with no additional interfacing logic required.

The DAC1208 series provides all 12 input lines to allow single buffering for maximum throughput when used with 16-bit processors. These input lines can also be externally configured to permit an 8-bit data interface. The DAC1230 series can be used with an 8-bit data bus directly as it internally formulates the 12-bit DAC data from its 8 input lines. All of these DACs accept left-justified data from the processor.

The analog section is a precision silicon-chromium (Si-Cr) R-2R ladder network and twelve CMOS current switches. An inverted R-2R ladder structure is used with the binary weighted currents switched between the I_{OUT1} and I_{OUT2} maintaining a constant current in each ladder leg independent of the switch state. Special circuitry provides TTL logic input voltage level compatibility.

The DAC1208 series and DAC1230 series are the 12-bit members of a family of microprocessor compatible DACs (MICRO-DACs™). For applications requiring other resolutions, the DAC1000 series for 10-bit and DAC0830 series for 8-bit are available alternatives.

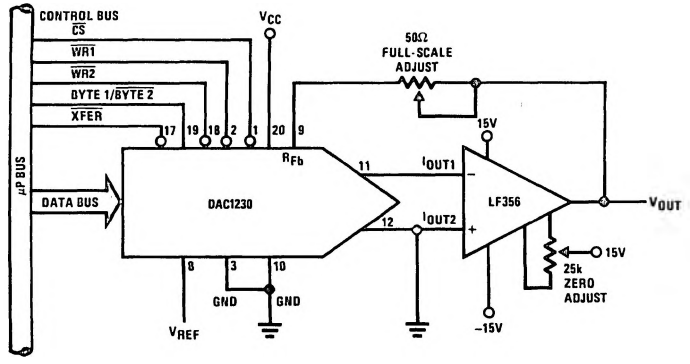
Features

- Linearity specified with zero and full-scale adjust only
- Direct interface to all popular microprocessors
- Double-buffered, single-buffered or flow through digital data inputs
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- Operates stand-alone (without μP) if desired
- All parts guaranteed 12-bit monotonic
- DAC1230 series is pin compatible with the DAC0830 series 8-bit MICRO-DACs

Key Specifications

Current Settling Time	1 μs
Resolution	12 Bits
Linearity (Guaranteed over temperature)	10, 11, or 12 Bits of FS
Gain Tempco	1.3 ppm/°C
Low Power Dissipation	20 mW
Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
ESD Susceptability	800V

Operating Conditions

Lead Temperature (Soldering, 10 sec.)	300°C
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC1208LCJ, DAC1209LCJ, DAC1210LCJ, DAC1230LCJ, DAC1231LCJ, DAC1232LCJ, DAC1231LIN, DAC1232LIN	−40°C ≤ T_A ≤ +85°C
DAC1208LCJ-1, DAC1210LCJ-1, DAC1230LCJ-1, DAC1231LCJ-1, DAC1232LCJ-1, DAC1231LCN, DAC1232LCN, DAC1231LCWM, DAC1232LCWM	0°C ≤ T_A ≤ +70°C
Range of V_{CC}	4.75 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted. **Boldface limits apply from T_{MIN} to T_{MAX} (see Note 13);** all other limits $T_A = T_J$ = 25°C.

Parameter	Conditions	Notes	Typ (Note 10)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
Resolution			12	**12**	**12**	Bits
Linearity Error (End Point Linearity)	Zero and Full-Scale Adjusted	4, 7, 13				
	DAC1208, DAC1230			**±0.018**	**±0.018**	% of FSR
	DAC1209, DAC1231			**±0.024**	**±0.024**	% of FSR
	DAC1210, DAC1232			**±0.050**	**±0.05**	% of FSR
Differential Non-Linearity	Zero and Full-Scale Adjusted	4, 7, 13				
	DAC1208, DAC1230			**±0.018**	**±0.018**	% of FSR
	DAC1209, DAC1231			**±0.024**	**±0.024**	% of FSR
	DAC1210, DAC1232			**±0.050**	**±0.05**	% of FSR
Monotonicity		4	12	**12**	**12**	Bits
Gain Error (Min)	Using Internal R_{Fb} V_{ref} = ±10V, ±1V	7	−0.1	0.0		% of FSR
Gain Error (Max)		7	−0.1	−0.2		% of FSR
Gain Error Tempco		7	±1.3		**±6.0**	ppm of FS/°C
Power Supply Rejection	All Digital Inputs Latched High	7	±3.0	±30		ppm of FSR/V
Reference Input Resistance (Min) Reference Input Resistance (Max)		13	15 15	**10** **20**	**10** **20**	kΩ
Output Feedthrough Error	V_{REF} = 20 Vp-p, f = 100 kHz All Data Inputs Latched Low	9	3.0			mVp-p
Output Capacitance	All Data Inputs Latched High I_{OUT1}				200	pF
	All Data Inputs Latched High I_{OUT2}				70	pF
	All Data Inputs Latched Low I_{OUT1}				70	pF
	All Data Inputs Latched Low I_{OUT2}				200	pF
Supply Current Drain		13		2.0	**2.5**	mA
Output Leakage Current I_{OUT1}	All Data Inputs Latched Low	11, 13	0.1	**15**	**15**	nA
I_{OUT2}	All Data Inputs Latched High	11, 13	0.1	**15**	**15**	nA
Digital Input Threshold	Low Threshold	13		**0.8**	**0.8**	V_{DC}
	High Threshold	13		**2.2**	**2.2**	V_{DC}
Digital Input Currents	Digital Inputs <0.8V	13		**−200**	**−200**	μA_{DC}
	Digital Inputs >2.2V	13		**10**	**10**	μA_{DC}

Electrical Characteristics (Continued)

V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted. **Boldface limits apply from T_{MIN} to T_{MAX} (see Note 13);** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	See Note	Typ (Note 10)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
AC CHARACTERISTICS							
t_s	Current Setting Time	V_{IL} = 0V, V_{IH} = 5V		1.0			µs
t_W	Write and XFER Pulse Width Min.	V_{IL} = 0V, V_{IH} = 5V	8	50		320 **320**	ns
t_{DS}	Data Setup Time Min.	V_{IL} = 0V, V_{IH} = 5V		70		320 **320**	
t_{DH}	Data Hold Time Min.	V_{IL} = 0V, V_{IH} = 5V		30		90 **90**	
t_{CS}	Control Setup Time Min.	V_{IL} = 0V, V_{IH} = 5V		60		320 **320**	
t_{CH}	Control Hold Time Min.	V_{IL} = 0V, V_{IH} = 5V		0		10	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if V_{REF} = 10V then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels. Guaranteed for V_{CC} = 11.4V to 15.75V and V_{REF} = −10V to +10V.

Note 7: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1208 is 0.012% of FSR(max). This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% × V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR(parts per million of full-scale range) and ppm of FS(parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. In this instance, 1 ppm of FSR = $V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ±6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from −40°C to +85°C of ±(6)($V_{REF}/10^6$)(125°C) or ±0.75 (10^{-3}) V_{REF} which is ±0.075% of V_{REF}.

Note 8: This spec implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH} and t_S to apply.

Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 10: Typicals are at 25°C and represent the most likely parametric norm.

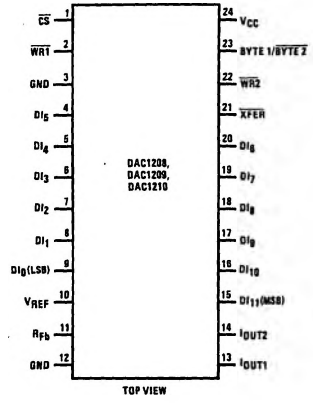
Note 11: A 10 nA leakage current with R_{Fb} = 20k and V_{REF} = 10V corresponds to a zero error of $(10 \times 10^{-9} \times 20 \times 10^3) \times 100\%$ 10V or 0.002% of FS.

Note 12: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

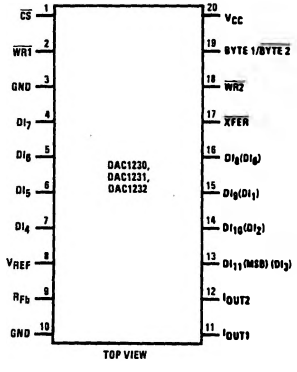
Note 13: Tested limit for −1 suffix parts applies only at 25°C.

Connection Diagrams

Dual-In-Line Package



Dual-In-Line Package



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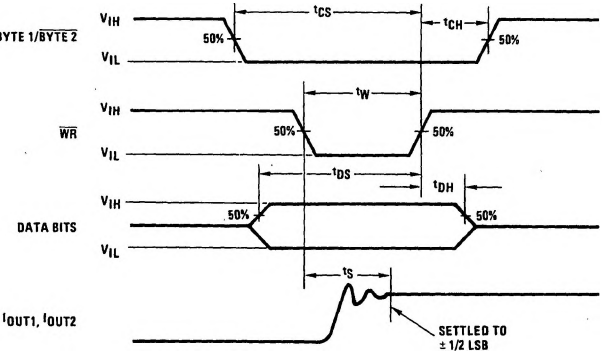
See Ordering Information

Switching Waveforms



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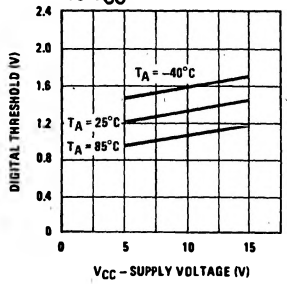
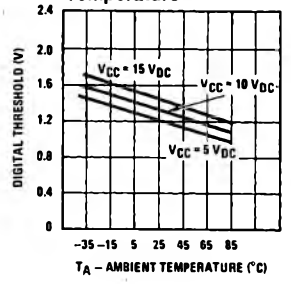
Typical Performance Characteristics

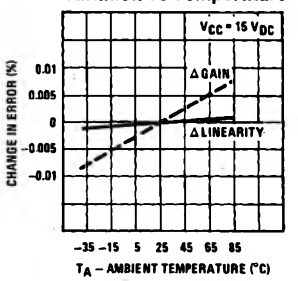
Digital Input Threshold vs V_{CC}



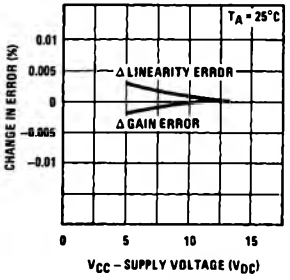
Digital Input Threshold vs Temperature



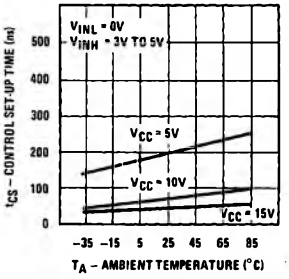
Gain and Linearity Error Variation vs Temperature



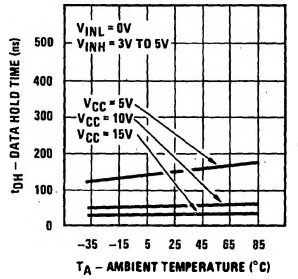
Gain and Linearity Error Variation vs Supply Voltage



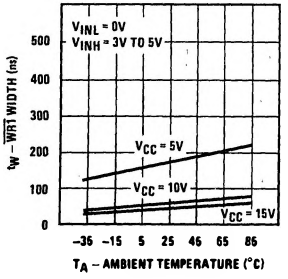
Control Set-Up Time, t_{CS}



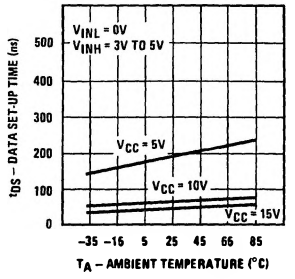
Data Hold Time, t_{DH}



Write Pulse Width, t_W



Data Set-Up Time, t_{DS}



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Definition of Package Pinouts

CONTROL SIGNALS (all control signals are level actuated)

$\overline{CS}$: Chip Select (active low). The $\overline{CS}$ will enable $\overline{WR1}$.

$\overline{WR1}$: Write 1. The active low $\overline{WR1}$ is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR1}$ is high. The 12-bit input latch is split into two latches. One holds the first 8 bits, while the other holds 4 bits. The Byte 1/$\overline{Byte\ 2}$ control pin is used to select both latches when Byte 1/$\overline{Byte\ 2}$ is high or to overwrite the 4-bit input latch when in the low state.

Byte 1/$\overline{Byte\ 2}$: Byte Sequence Control. When this control is high, all 12 locations of the input latch are enabled. When low, only the four least significant locations of the input latch are enabled.

$\overline{WR2}$: Write 2 (active low). The $\overline{WR2}$ will enable $\overline{XFER}$.

$\overline{XFER}$: Transfer Control Signal (active low). This signal, in combination with $\overline{WR2}$, causes the 12-bit data which is available in the input latches to transfer to the DAC register.

DI_0 to DI_{11}: Digital Inputs. DI_0 is the least significant digital input (LSB) and DI_{11} is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital code of all 1s in the DAC register, and is zero for all 0s in the DAC register.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} = \text{constant}$ (for a fixed reference voltage). This constant current is

$$V_{REF} \times \left(1 - \frac{1}{4096}\right)$$

divided by the reference input resistance.

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

GND: Pins 3 and 12 of the DAC1208, DAC1209, and DAC1210 must be connected to ground. Pins 3 and 10 of the DAC1230, DAC1231, and DAC1232 must be connected to ground. It is important that I_{OUT_1} and I_{OUT_2} are at ground potential for current switching applications. Any difference of potential (V_{OS} on these pins) will result in a linearity change of

$$\frac{V_{OS}}{3\,V_{REF}}$$

For example, if V_{REF} = 10V and these ground pins are 9 mV offset from I_{OUT_1} and I_{OUT_2}, the linearity change will be 0.03%.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1208 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

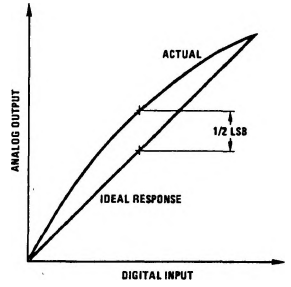
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ± ½ LSB of the final output value.

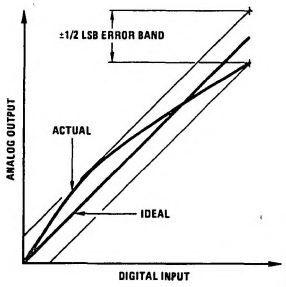
Full-Scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1208 or DAC1230 series, full-scale is $V_{REF} - 1$ LSB. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 2.44\ mV = 9.9976V$. Full-scale error is adjustable to zero.

Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.



a) End Point Test After Zero and FS Adjust



b) Shifting FS Adjust to Pass Best Straight Line Test

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Application Hints

1.0 DIGITAL INTERFACE

These DACs are designed to provide all of the necessary digital input circuitry to permit a direct interface to a wide variety of microprocessor systems. The timing and logic level convention of the input control signals allow the DACs to be treated as a typical memory device or I/O peripheral with no external logic required in most systems. Essentially these DACs can be mapped as a two-byte stack in memory (or I/O space) to receive their 12 bits of input data in two successive 8-bit data writing sequences. The DAC1230 series is intended for use in systems with an 8-bit data bus. The DAC1208 series provides all 12 digital input lines which can be externally configured to be controlled from an 8-bit bus or can be driven directly from a 16-bit data bus.

All of the digital inputs to these DACs contain a unique threshold regulator circuit to maintain TTL voltage level compatibility independent of the applied V_{CC} to the DAC. Any input can also be driven from higher voltage CMOS logic levels in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. As a troubleshooting aid, if any digital input is inadvertently left floating, the DAC will interpret the pin as a logic "1".

Double buffered digital inputs allow the DAC to internally format the 12-bit word used to set the current switching R-2R ladder network (see section 2.0) from two 8-bit data write cycles. *Figures 1* and *2* show the internal data registers and their controlling logic circuitry. The timing diagrams for updating the DAC output are shown in sections 1.1, 1.2 and 1.3 for three possible control modes. The method used depends strictly upon the particular application.

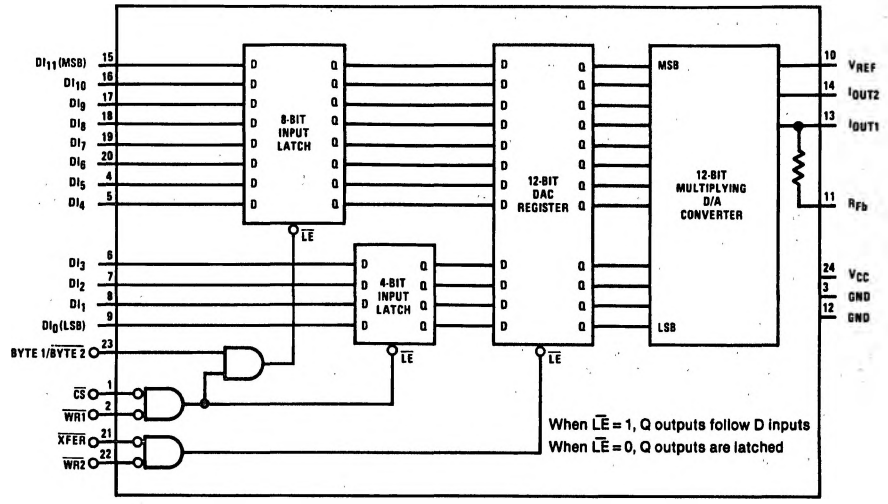

FIGURE 1. DAC1208, DAC1209, DAC1210 Functional Diagram

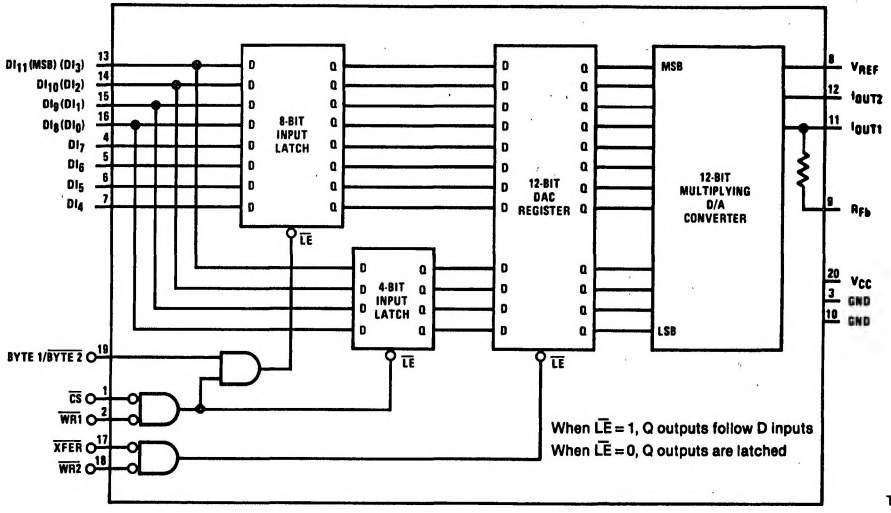

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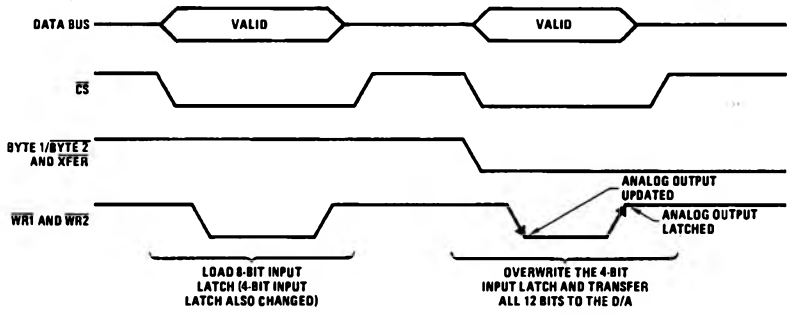
FIGURE 2. DAC1230, DAC1231, DAC1232 Functional Diagram

Application Hints (Continued)

1.1 Automatic Transfer

The 12-bit DAC word is automatically transferred to the DAC register and the R-2R ladder when the second write (the 4 LSBs of the data) occurs.



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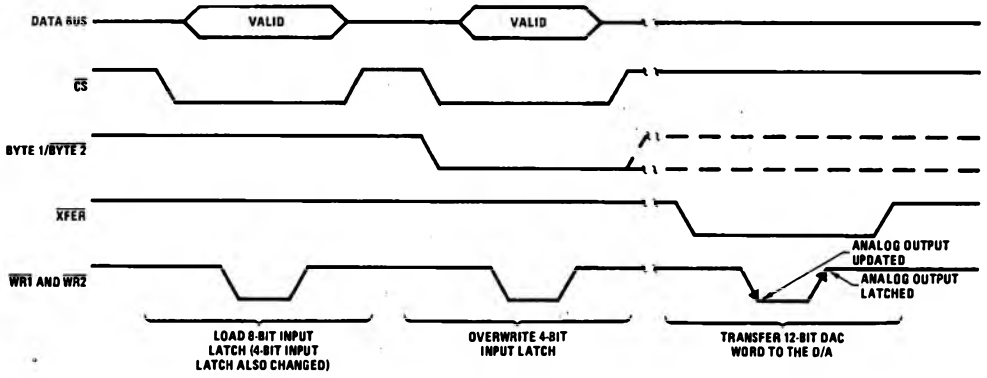
1.2 Independent Processor Transfer Control

In this case a separate address is decoded to provide the $\overline{XFER}$ signal. This allows the processor to load the next required DAC word but not change the analog output until some time later, most useful for the simultaneous updating of several DACs in a system where their $\overline{XFER}$ lines would be tied together.



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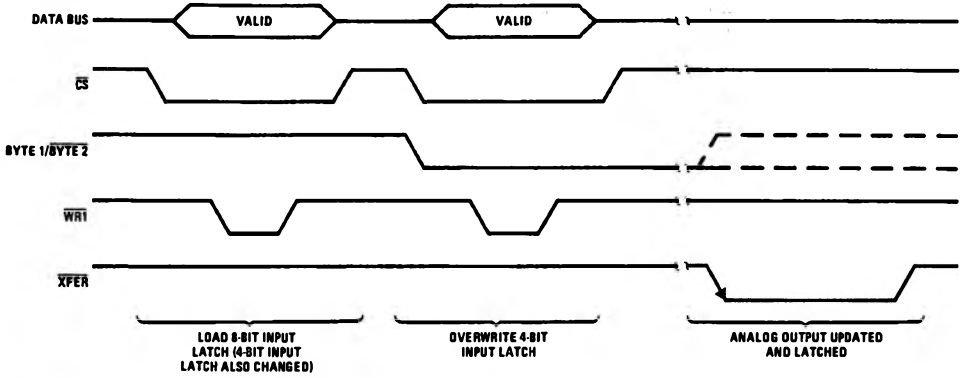
1.3 Transfer via an External Strobe

This method is basically the same as the previous operation except the $\overline{XFER}$ signal is provided by a device other than the processor. This allows the DAC to hold the code for a conditional analog output signal which will be required on demand from an external monitoring device (an analog voltage comparator for instance).



$\overline{WR2}$ tied to a logic low (0V)

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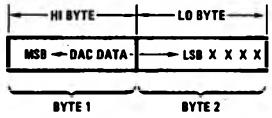
Application Hints (Continued)

1.4 Left-Justified Data Format

It is important to realize that the input registers of these DACs are arranged to accept a left-justified data word from the microprocessor with the most significant 8 bits coming first (Byte 1) and the lower 4 bits second. Left justification simply means that the binary point is assumed to be located to the left of the most significant bit. *Figure 3* shows how the 12 bits of DAC data should be arranged in 2 8-bit registers of an 8-bit processor before being written to the DAC.



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X = don't care

FIGURE 3. Left-Justified Data Format

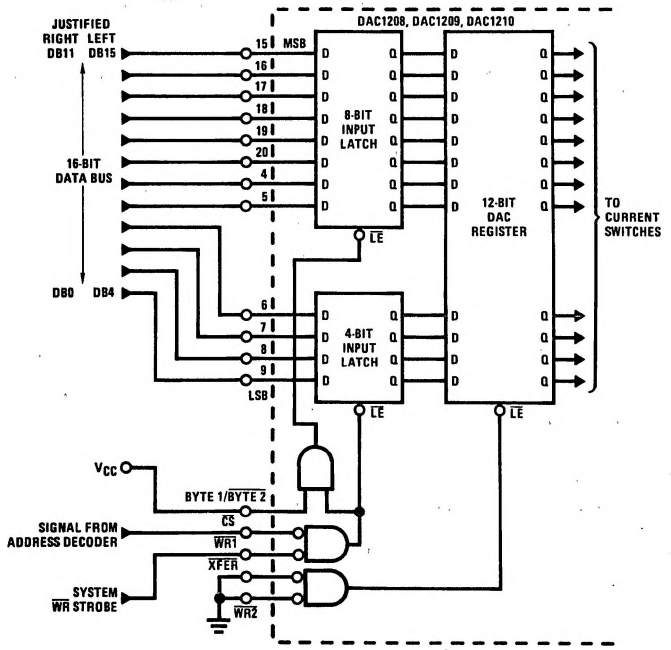
1.5 16-Bit Data Bus Interface

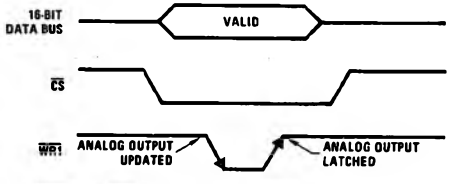
The DAC1208 series provides all 12 digital input lines to permit a direct parallel interface to a 16-bit data bus. In this instance, double buffering is not always necessary (unless a simultaneous updating of several DACs or a data transfer via an external strobe is desired) so the 12-bit DAC register can be wired to flow-through whereby its Q outputs always reflect the state of its D inputs. The external connections required and the timing diagram for this single buffered application are shown in *Figure 4*. Note that either left or right-justified data from the processor can be accommodated with a 16-bit data bus.

1.6 Flow-Through Operation

Through primarily designed to provide microprocessor interface compatibility, the MICRO-DACs can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in appli-

Interface Timing





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XFER and WR2 grounded; Byte 1/Byte 2 tied to V_{CC}.

FIGURE 4. 16-Bit Data Bus Interface for the DAC1208 Series

Application Hints (Continued)

cations where the DAC is used in a continuous feedback control loop and is driven by a binary up/down counter, or in function generation circuits where a ROM is continuously providing DAC data.

Only the DAC1208, DAC1209, DAC1210 devices can have all 12 inputs flow-through. Simply grounding $\overline{CS}$, $\overline{WR1}$, $\overline{WR2}$ and $\overline{XFER}$ and tying Byte 1/$\overline{Byte\ 2}$ high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.7 Address Decoding Tips

It is possible to map the MICRO-DACs into system ROM space to allow more efficient use of existing address decoding hardware. The DAC in effect can share the same addresses of any number of ROM locations. The ROM outputs will only be enabled by a READ of its address (gated by the system READ strobe) and the DAC will only accept data that is written to the same address (gated by the system WRITE strobe).

The Byte 1/$\overline{Byte\ 2}$ control function can easily be generated by the processor's least significant address bit (A0) by placing the DAC at two consecutive address locations and utilizing double-byte WRITE instructions which automatically increment or decrement the address. The $\overline{CS}$ and $\overline{XFER}$ signals can then be decoded from the remaining address bits. Care must be taken in selecting the actual address used for Byte 1 of the DAC to prevent a carry (as a result of incrementing the address for Byte 2) from propagating through the address word and changing any of the bits decoded for $\overline{CS}$ or $\overline{XFER}$. *Figure 5* shows how to prevent this effect.

The same problem can occur from a borrow when an auto-decremented address is used; but only if the processor's address outputs are inverted before being decoded.

1.8 Control Signal Timing

When interfacing these MICRO-DACs to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{WR}$ strobe pulse width which is specified as 320 ns for $V_{CC} = 11.4V$ to 15.75V and operation over temperature, but typically a pulse width of only 250 ns is adequate. A second consideration is that the guaranteed minimum data hold time of 90 ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{CS}$) $\overline{WR}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{WR}$ pulse

Write Cycle	Address Bits			
	15 ... 2		1*	0**
First (Byte 1)	Decoded to Address DAC		0	1
Second (Byte 2)			1	0

*Starting with a 0 prevents a carry on address incrementing.

**Used as Byte 1/$\overline{Byte2}$ Control.

FIGURE 5

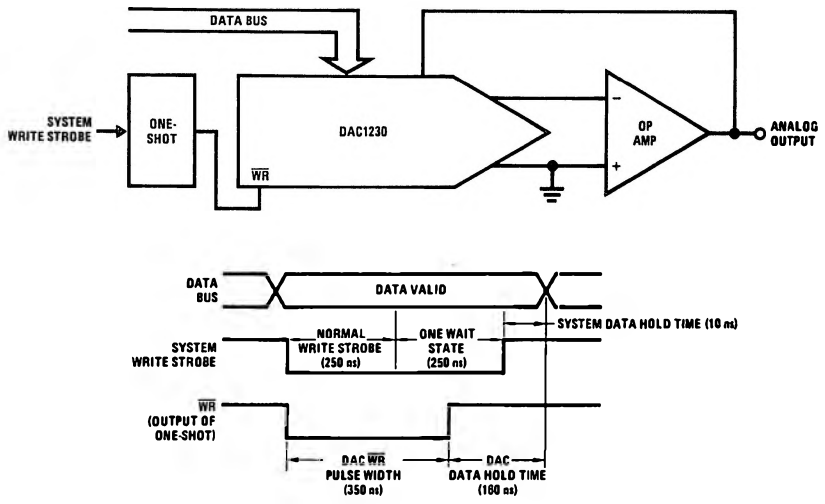

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FIGURE 6. Accommodating a High Speed System

Application Hints (Continued)

width. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{WR}$ pin of the DAC. This is illustrated in *Figure 6* for an exemplary system which provides a 250 ns $\overline{WR}$ strobe time with a data hold time of only 10 ns.

The proper data set-up time prior to the latching edge (low to high transition) of the $\overline{WR}$ strobe, is insured if the $\overline{WR}$ pulse width is within spec and the data is valid on the bus for the duration of the DAC $\overline{WR}$ strobe.

1.9 Digital Signal Feedthrough

A typical microprocessor is a tremendous potential source of high frequency noise which can be coupled to sensitive analog circuitry. The fast edges of the data and address bus signals generate frequency components of 10's of megahertz and may cause fast transients to appear at the DAC output, even when data is latched internally.

In low frequency or DC applications, low pass filtering can reduce the magnitude of any fast transients. This is most easily accomplished by over-compensating the DAC output amplifier by increasing the value of its feedback capacitor.

In applications requiring a fast output response from the DAC and op amp, filtering may not be feasible. In this event, digital signals can be completely isolated from the DAC circuitry, by the use of a DM74LS374 latch, until a valid $\overline{CS}$ signal is applied to update the DAC. This is shown in *Figure 7*.

A single TRI-STATE® data buffer such as the DM81LS95 can be used to isolate any number of DACs in a system. *Figure 8* shows this isolating circuitry and decoding hardware for a multiple DAC analog output card. Pull-up resistors are used on the buffer outputs to limit the impedance at the DAC digital inputs when the card is not selected. A unique feature of this card is that the DAC $\overline{XFER}$ strobes are controlled by the data bus. This allows a very flexible update of any combination of analog outputs via a transfer word which would contain a zero in the bit position assigned to any of the DACs required to change to a new output value.

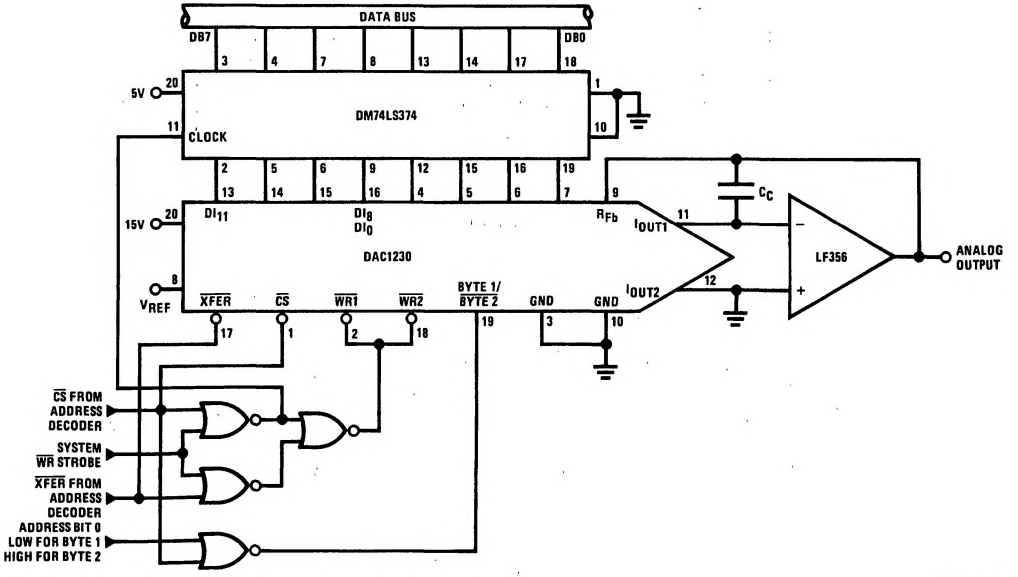

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FIGURE 7. Isolating Data Bus from DAC Circuitry to Eliminate Digital Noise Coupling

Application Hints (Continued)

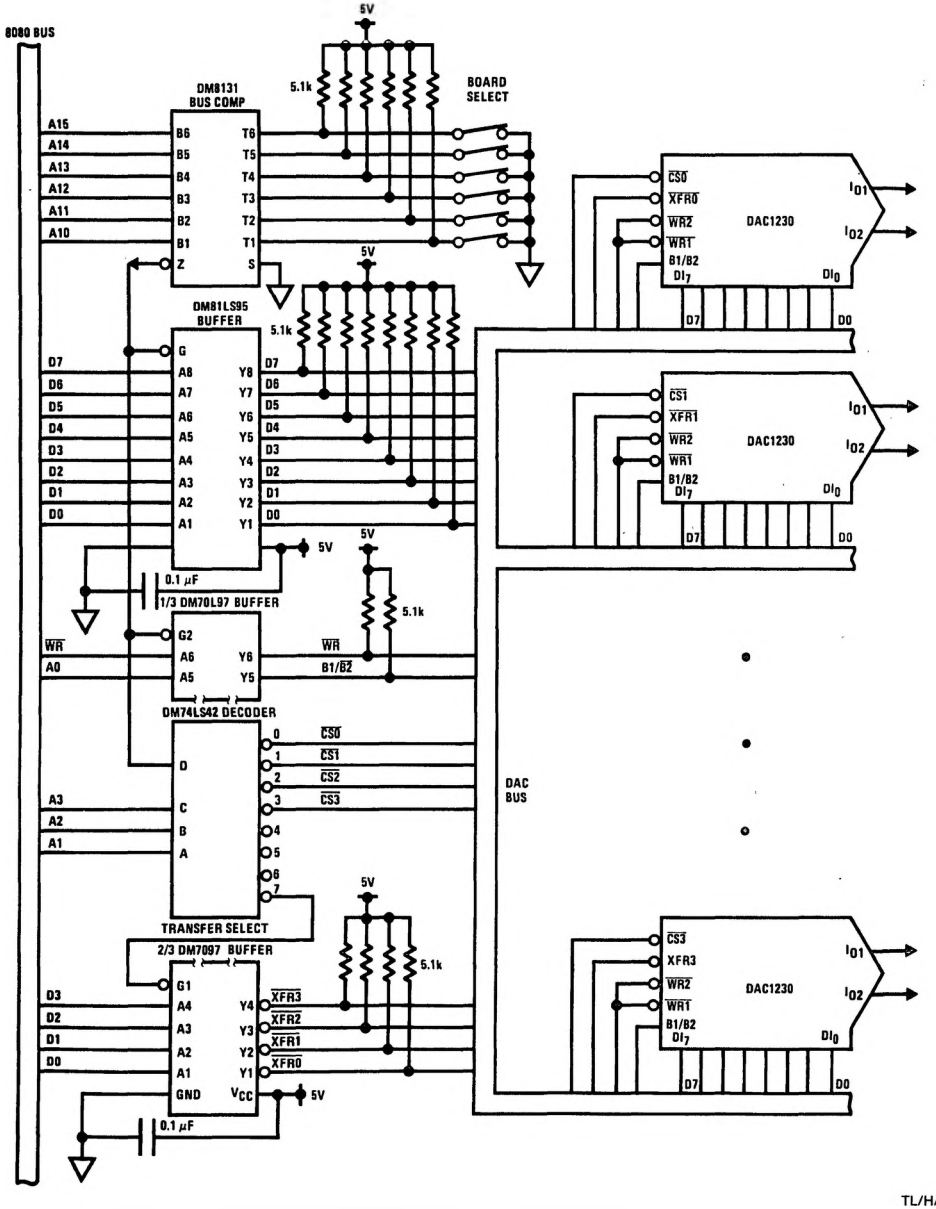

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FIGURE 8. TRI-STATE® Buffers Isolate the Data and Control Lines from the DACs. A Transfer Word Provides a Flexible Update.

Application Hints (Continued)

2.0 ANALOG APPLICATIONS

The analog output signal for these DACs is derived from a conventional R-2R current switching ladder network. A detailed description of this network can be found on the DAC1000 series data sheet. Basically, output I_{OUT1} provides a current directly proportional to the product of the applied reference voltage and the digital input word. A second output, I_{OUT2} will be a current proportional to the complement of the digital input. Specifically:

$$I_{OUT1} = \frac{V_{REF}}{R} \times \frac{D}{4096}$$

$$I_{OUT2} = \frac{V_{REF}}{R} \times \frac{4095 - D}{4096}$$

where D is the decimal equivalent of the applied 12-bit binary word (ranging from 0 to 4095), V_{REF} is the voltage applied to the V_{REF} terminal and R is the internal resistance of the R-2R ladder. R is nominally 15 kΩ.

2.1 Obtaining a Unipolar Output Voltage

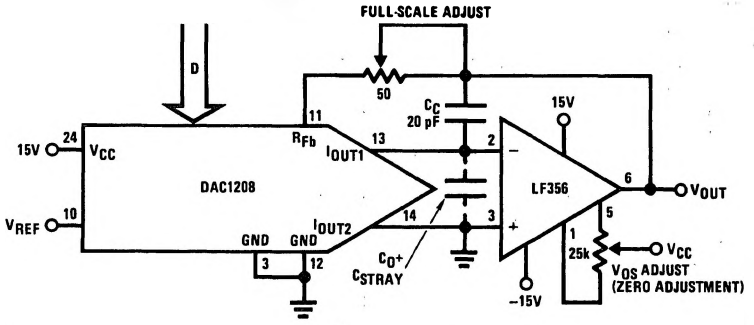
To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential (0 V_{DC}) as possible. With $V_{REF} = +10V$ every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in *Figure 9*.

The inverting input of the op amp is a virtual ground created by the feedback from its output through the internal 15 kΩ resistor, R_{Fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{Fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{Fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage source or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15 kΩ to ground to external circuitry.

Always use the internal R_{Fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET™ op amps are highly recommended for use with these DACs because of their very low input current.



$$V_{OUT} = -(I_{OUT1} \times R_{Fb})$$

$$= \frac{-V_{REF}(D)}{4096}$$

for $0 \leq D \leq 4095$

FIGURE 9. Unipolar Output Configuration

Application Hints (Continued)

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{Fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in *Figure 9*, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

2.1.1 Zero and Full-Scale Adjustments

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

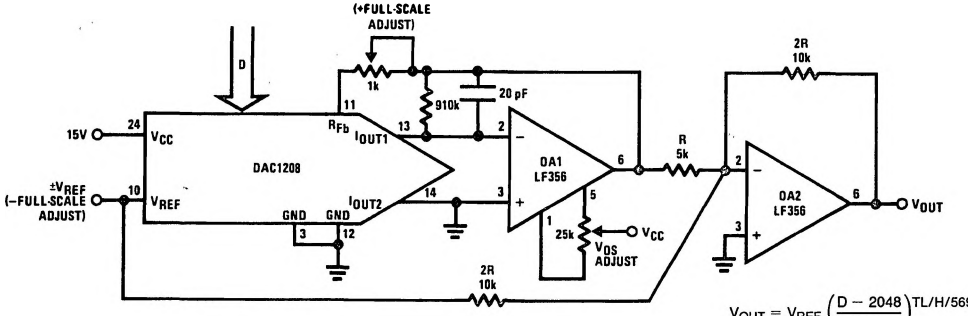
The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near 0 V_{DC} as possible. This is accomplished by shorting out R_{Fb}, the amplifier feedback resistor, and adjusting the v_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all ones for I_{OUT2}). The short around R_{Fb} is then removed and the converter is zero adjusted.

A unique feature of this series of DACs is that the full-scale or gain error is guaranteed to be negative. The gain error specification is a measure of how close the value of the internal feedback resistor, R_{Fb}, matches the R-2R ladder resistors. A negative gain error indicates that R_{Fb} is a smaller resistance value than it should be. To adjust this gain error, some resistance must always be added in series with R_{Fb}. The 50Ω potentiometer shown is sufficient to adjust the worst-case gain error for these devices.

2.2 Bipolar Output Voltage from a Fixed Reference

The addition of a second op amp to the unipolar circuit can generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word to allow two quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication. This circuit is shown in *Figure 10*.

This configuration features several improvements over existing circuits for a bipolar output shown with other multiplying DACs. Only the offset voltage of amplifier 1 affects the linearity of the DAC. The offset voltage error of the second op amp (although a constant output error) has no effect on linearity. In addition, this configuration offers a non-interactive positive and negative full-scale calibration procedure.



$$V_{OUT} = V_{REF}\left(\frac{D - 2048}{2048}\right)$$ TL/H/5690-16

for $0 \le D \le 4095$

$$1\ LSB = \frac{|V_{REF}|}{2048}$$

Input Code MSB.....LSB	Ideal V_{OUT}	
	$+V_{REF}$	$-V_{REF}$
1 1 1 1 1 1 1 1 1 1 1 1	$V_{REF} - 1$ LSB	$-\|V_{REF}\| + 1$ LSB
1 1 0 0 0 0 0 0 0 0 0 0	$V_{REF}/2$	$-\|V_{REF}\|/2$
1 0 0 0 0 0 0 0 0 0 0 0	0	0
0 1 1 1 1 1 1 1 1 1 1 1	−1 LSB	+1 LSB
0 0 1 1 1 1 1 1 1 1 1 1	$-\frac{V_{REF}}{2} - 1$ LSB	$\frac{\|V_{REF}\|}{2} + 1$ LSB
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}$	$+\|V_{REF}\|$

FIGURE 10. Bipolar Output Voltage Configuration

Application Hints (Continued)

2.2.1 Zero and Full-Scale Adjustments

To calibrate the bipolar output circuit, three adjustments are required. The first step is to set all of the digital inputs LOW (to force I_{OUT1} to 0) then null the V_{OS} of amplifier 1 by setting the voltage at its inverting input (pin 2) to zero volts. Next, with a code of all zeros still applied, adjust "−full-scale adjust", the reference voltage, for $V_{OUT} = \pm|V_{REF}$ ideal|. The polarity of the output voltage at this time will be opposite that of the applied reference. Finally, set all of the digital inputs HIGH and adjust "+full-scale adjust" for

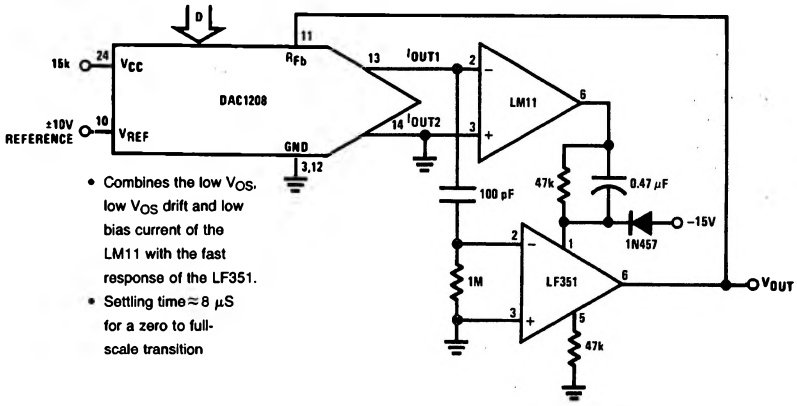
$$V_{OUT} = V_{REF}\frac{2047}{2048}.$$

The polarity of the output will be the same as that of the reference voltage.

3.0 APPLICATION IDEAS

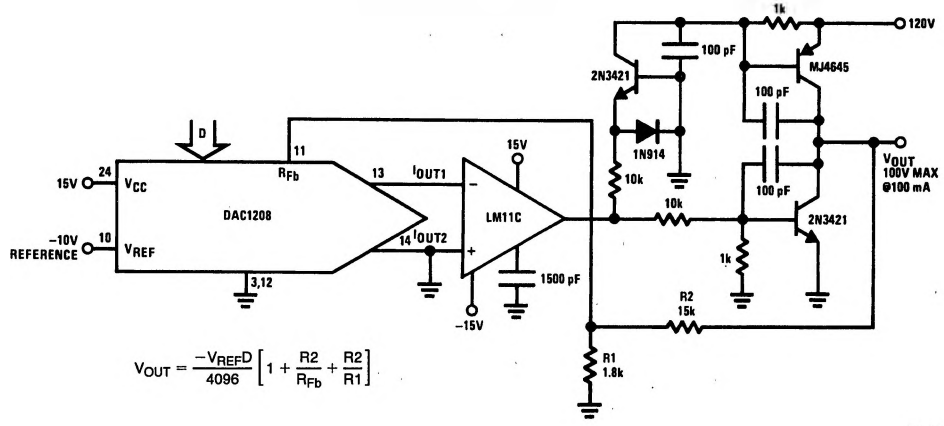
In this section the digital input word is represented by the letter D and is equal to the decimal equivalent of the 12-bit binary input. Hence D can be any integer value between 0 and 4095.

Composite Amplifier for Good DC Characteristics and Fast Output Response



- Combines the low V_{OS}, low V_{OS} drift and low bias current of the LM11 with the fast response of the LF351.
- Settling time ≈ 8 μS for a zero to full-scale transition

High Voltage, Power DAC



$$V_{OUT} = \frac{-V_{REF}D}{4096}\left[1 + \frac{R2}{R_{Fb}} + \frac{R2}{R1}\right]$$

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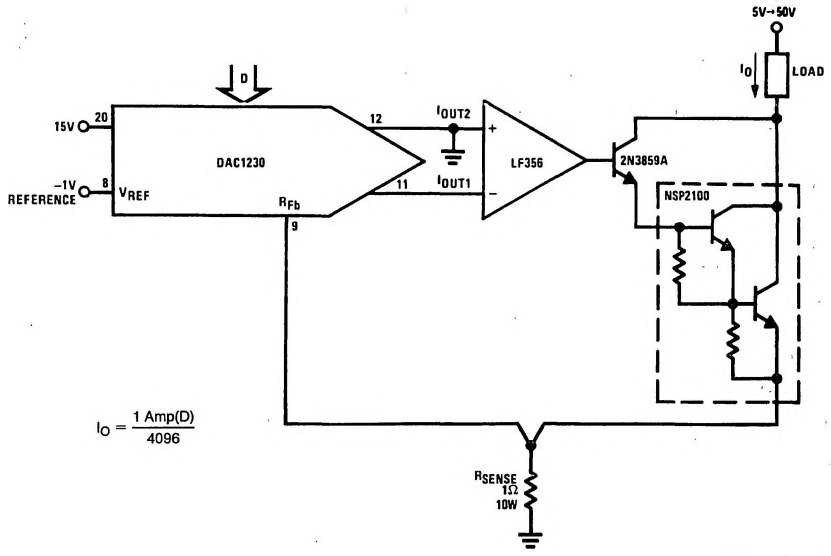
Application Hints (Continued)

High Current Controller



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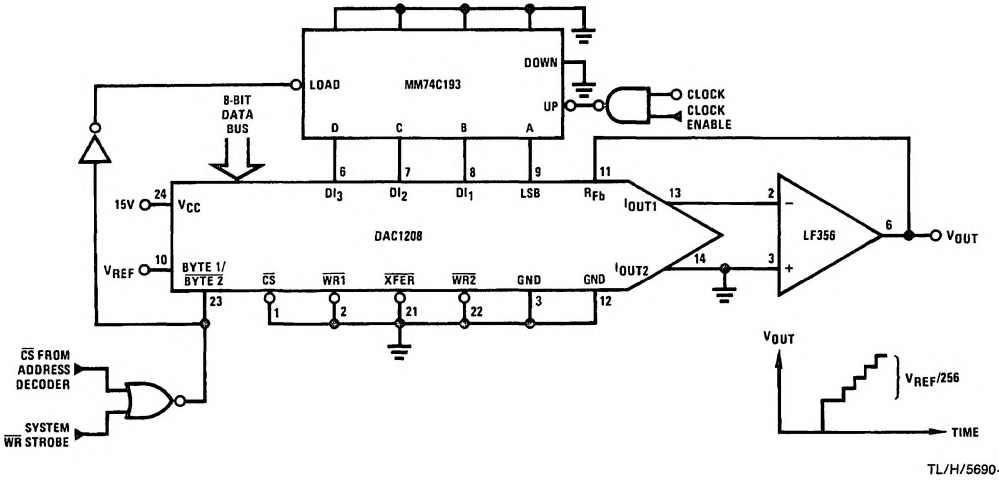
8-Bit Course, 4-Bit Vernier DAC



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Ordering Information

Part Number	Non-Linearity	Package	Temperature Range
DAC1208LCJ	0.018%	J24A Cerdip	−40°C to +85°C
DAC1208LCJ-1	0.018%	J24A Cerdip	0°C to +70°C
DAC1209LCJ	0.024%	J24A Cerdip	−40°C to +85°C
DAC1210LCJ	0.050%	J24A Cerdip	−40°C to +85°C
DAC1210LCJ-1	0.050%	J24A Cerdip	0°C to +70°C
DAC1230LCJ	0.018%	J20A Cerdip	−40°C to +85°C
DAC1230LCJ-1	0.018%	J20A Cerdip	0°C to +70°C
DAC1231LCJ	0.024%	J20A Cerdip	−40°C to +85°C
DAC1231LCJ-1	0.024%	J20A Cerdip	0°C to +70°C
DAC1231LCN	0.024%	N20A Plastic	0°C to +70°C
DAC1231LCWM	0.024%	M20B SO	0°C to +70°C
DAC1231LIN	0.024%	N20A Plastic	−40°C to +85°C
DAC1232LCJ	0.050%	J20A Cerdip	−40°C to +85°C
DAC1232LCJ-1	0.050%	J20A Cerdip	0°C to +70°C
DAC1232LCN	0.050%	N20A Plastic	0°C to +70°C
DAC1232LCWM	0.050%	M20B SO	0°C to +70°C
DAC1232LIN	0.050%	N20A Plastic	−40°C to +85°C