ADVANCE INFORMATION

# DAC 3560C
# Audio-Subsystem for Portable Applications

Edition Feb. 5, 2003
6251-588-1AI

MICRONAS

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**Audio-Subsystem for Portable Applications**

## 1. Introduction

The DAC 3560C is a single-chip, high-precision, dual digital-to-analog converter designed for audio applications. The employed conversion technique is based on oversampling with noise-shaping.

With Micronas' unique multibit sigma-delta technique, less sensitivity to clock jitter, high linearity, and a superior S/N ratio have been achieved. The DAC 3560C is controlled via SPI or $I^2C$ bus.

Digital audio input data is received via a versatile $I^2S$ interface. The DAC 3560C provides three integrated power audio drivers: a stereo headphone, a mono earpiece and a mono loudspeaker driver. Moreover, mixing additional analog sources to the D/A-converted signal is supported.

For applications with a noise-critical power supply environment, the DAC 3560C is equipped with an integrated Low Drop-Out Voltage Regulator (LDO). The LDO provides a stable 2.85 V output voltage and is intended for supplying the headphone and earpiece drivers. With the LDO, the Power Supply Rejection Ratio (PSRR) of the audio outputs is improved to more than 100 dB.

The DAC 3560C is designed for all kinds of applications in the audio and multimedia field, such as: mobile phones, PDAs, and digital audio players.

### 1.1. Features

- Three Integrated Short-Circuit-Protected Power Audio Drivers:
  - Stereo headphone output (25 mW at $V_{SUP}$=2.85 V, or 80 mW at $V_{SUP}$=5 V respectively)
  - Mono earpiece output (100 mW at $V_{SUP}$=2.85 V, or 300 mW at $V_{SUP}$=5 V, respectively)
  - Mono loudspeaker output (400 mW at $V_{SUP}$=3 V, or 1.1 W at $V_{SUP}$=5 V, respectively)
- Integrated LDO (Low Drop-Out Regulator)
- 100 dB PSRR
- 98 dB (A) Dynamic Range Multi-Bit Sigma Delta DAC
- Continuous Sample Rates from 8 kHz to 192 kHz
- Capacitor-free Headset Connection
- Analog Stereo and Mono Line Inputs with Programmable Gain
- $I^2C$/SPI Compatible Serial Control Ports
- $I^2S$ Digital Audio Interface
- Programmable Power Management
- –30 dB to 6 dB Analog Volume, Mute
- 2.2 V to 5.5 V Supply Voltage
- 1.8 V to 5.5 V Digital I/O Voltage
- Standby Mode
- Zero-Power Mode (< 10 µA)
- PQFN40 Package

### 1.2. Target Systems

- PDAs
- Hand-held Terminals
- Mobile and Cordless Phones
- Portable MP3 and CD Players

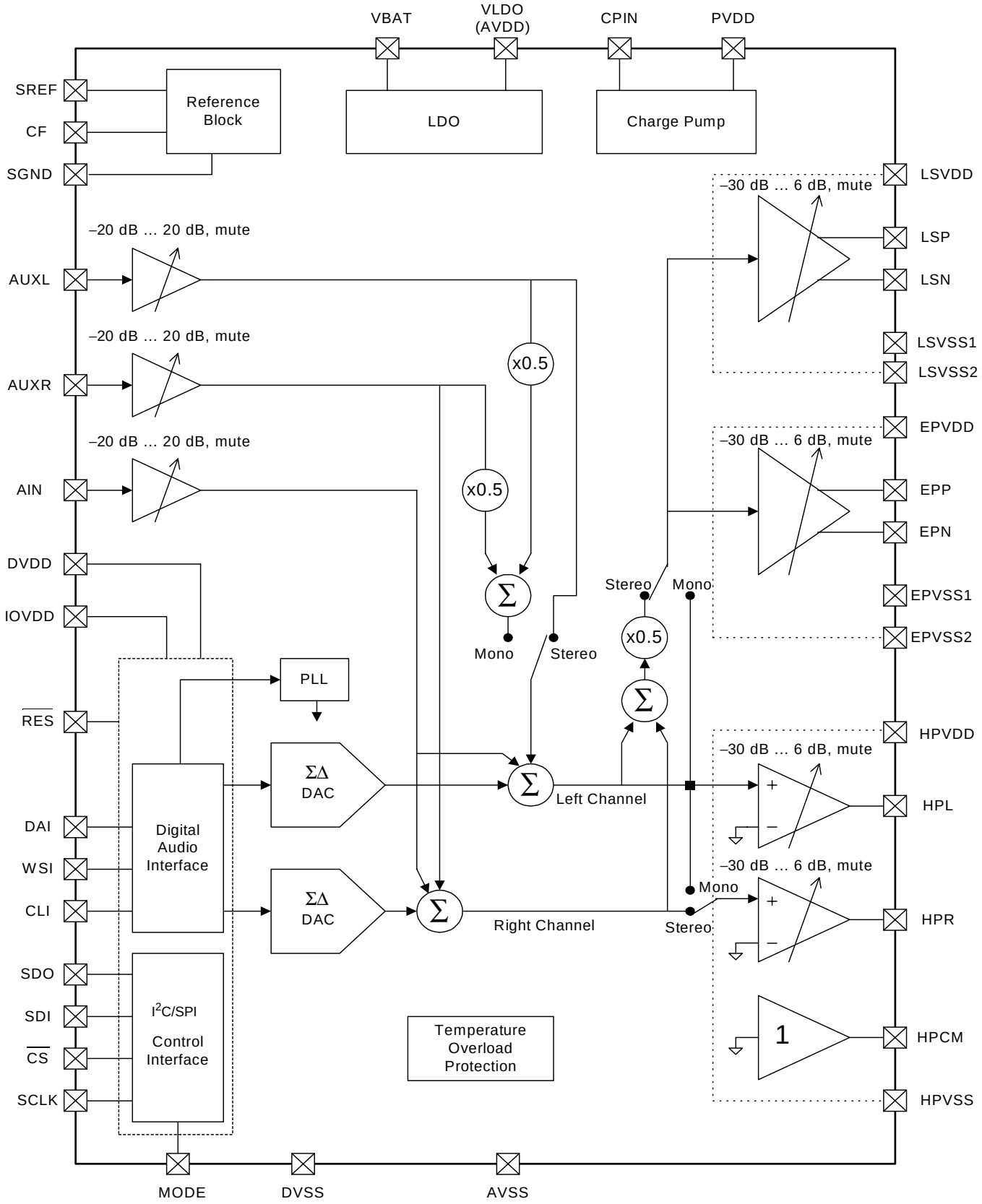



**Fig. 1–1:** Block Diagram

## 2. Functional Description

The main blocks are described in the following chapters. All functions are controlled via I²C/SPI protocol.

### 2.1. Digital Audio Interface (I²S)

The I²S interface is the digital audio interface between the DAC 3560C and external digital audio sources. It covers most of the I²S-compatible formats. All modes have two common features:

1. The MSB is left-justified to an I²S frame identification (WSI) transition.
2. Data is valid on the rising edge of the bit clock CLI.

**16-bit mode:**
In this case, the bit clock is 32 x $fs_{audio}$. Maximum word length is 16 bit.

**32-bit mode:**
In this case, the bit clock is 64 x $fs_{audio}$. Maximum word length is 32 bit.

**Automatic Detection:**
No I²C/SPI control is required to switch between 16-bit and 32-bit mode. It is recommended to switch the DAC 3560C into mute position while alternating between the two modes. For high-quality audio, it is recommended to use the 32-bit mode of the I²S interface to make use of the full dynamic range (if more than 16 bits are available).

**Left-Right Selection:**
Standard I²S format defines an audio frame always starting with the left channel and low-state of WSI. However, the DAC 3560C permits to change the polarity of WSI.

**Delay Bit:**
The standard I²S format requires a delay of one clock cycle between transitions of WSI and data MSB. In order to fit other formats, however, this characteristic can be switched on or off.

**Note:** Volume mute should be applied before changing I²S mode in order to avoid audible clicks

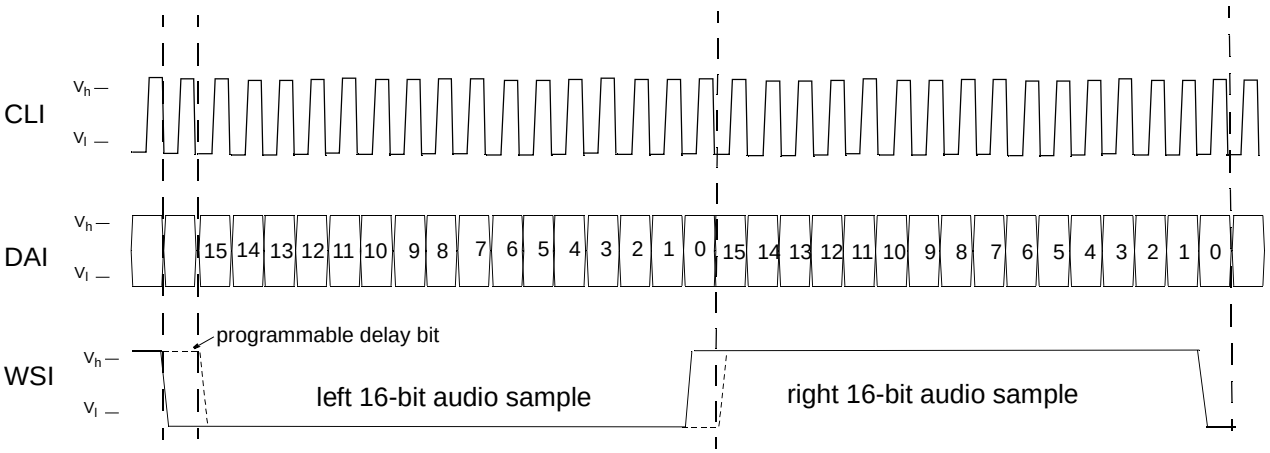



**Fig. 2–1:** I²S 16-bit mode

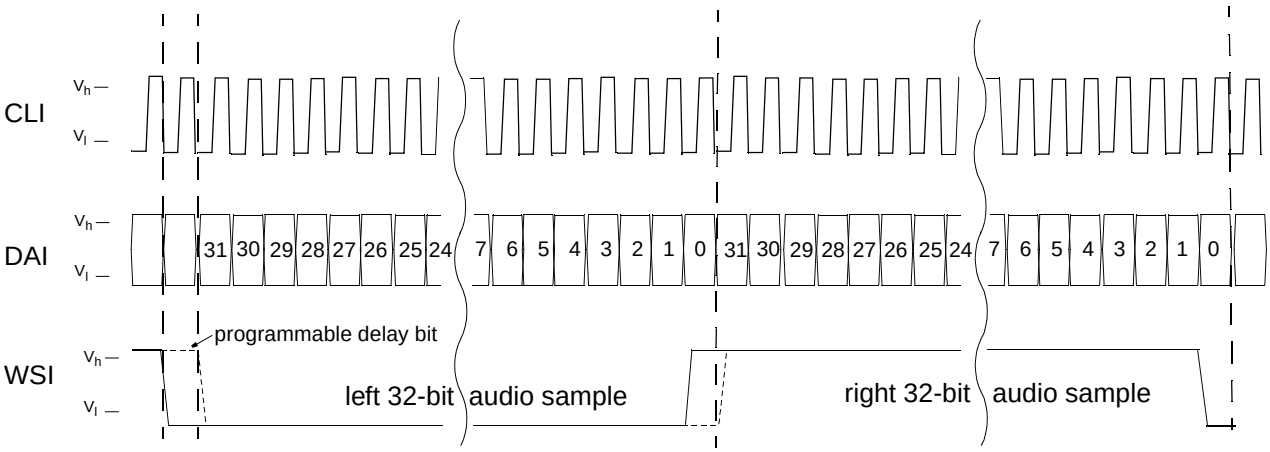



**Fig. 2–2:** I²S 32-bit mode

### 2.2. Clock System

Most DACs need 256 x $fs_{audio}$, 384 x $fs_{audio}$, or at least an asynchronous clock. The DAC 3560C does not need an external Master clock. No crystal is required.

All internal clocks are generated by an internal PLL circuit, which locks to the $I^2S$ bit clock (CLI). If no $I^2S$ clock is present, the IC can still be controlled and the analog signal path is still available as no $I^2S$ clock is needed for this.

The PLL also generates the clock for the DAC and the noise shaping system. Audible oversampling artifacts even at low audio sampling frequencies are eliminated.

### 2.3. Control Interface

The DAC 3560C has many register-programmable features. The control interface is used to program the registers of the device. It uses four pins:

SCLK - Serial Data Clock

SDI - Serial Data Input (Input/Output for $I^2C$)

SDO - Serial Data Output (SPI)

$\overline{CS}$ - Chip Select (SPI)

**Table 2–1:** Standard Protocols

| MODE Pin | Control Protocol |
|---|---|
| 1 | $I^2C$ |
| 0 | SPI |

The control interface supports two standard protocols, the $I^2C$ protocol (two-wire operation) and the SPI protocol (three or four-wire operation). The state of the MODE pin selects the control interface type.

### 2.4. Registers

All registers of the DAC 3560C are 8 bits wide and offer read/write access.

In Section 3. “Control Registers”, a definition of the DAC 3560C control registers is shown. A hardware reset initializes all control registers to 0, which is the default value for all registers. The registers are addressed by the sub-address byte, which follows the device address in $I^2C$ mode and is the first byte to be sent in SPI mode. The structure of the sub-address is identical in both modes (R/W is ignored in $I^2C$ mode).

**Table 2–2:** Sub-Address Byte

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Function | 0 | 0 | R/W | A4 | A3 | A2 | A1 | A0 |

**Table 2–3:** Structure of the Sub-Address Byte

| R | Reserved | Set to 0 | |
|---|---|---|---|
| R/W[1)] | Read/Write Access | 1=Read | 0=Write |
| A [4:0] | Control Interface Sub-Address | | |
| [1)] R/W must be set to 0 in $I^2C$ mode | | | |

**Note:** Pin $\overline{CS}$ must be set to IOVDD when using $I^2C$ mode.

### 2.5. I²C Bus Interface

The DAC 3560C is equipped with an I²C bus slave interface. The I²C bus interface uses one level of sub-addressing: the I²C device address is used to address the IC. The registers are read/write. The register address is incremented automatically at each data byte unless a stop condition occurs. The I²C device address is given below. .

**Table 2–4:** I²C device address byte

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | W/R |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0/1 |

Fig. 2–3 shows I²C bus protocols for write and read operations of the interface; the read operations require an extra start condition and repetition of the chip address with the device read command (DR). Fields with signals/data originating from the DAC 3560C are marked with a gray background.

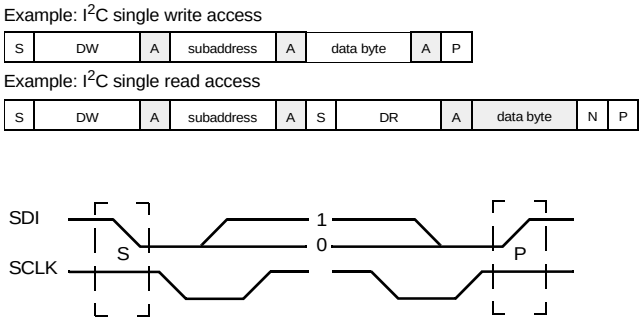



**Fig. 2–3:** Example of an I²C protocol for the DAC 3560C (MSB first; data must be stable while clock is high)

**Abbreviations:**

A = Acknowledge
N = Not Acknowledge (NAK)
S = Start
P = Stop
DW = I²C Device Write Address ($9A_{hex}$)
DR = I²C Device Read Address ($9B_{hex}$)

### 2.6. SPI Bus Interface

The SPI bus is a 4-wire serial communications interface. Unlike the I²C bus, the SPI uses two separate pins for input and output and $\overline{CS}$ signal instead of individual device addresses.

Read and write starts with a low signal at $\overline{CS}$. The first byte is always interpreted as sub-address byte, which contains the Register address. The following byte or bytes are then read/write register data.

If more than one data byte appears without changing $\overline{CS}$, the register address will be incremented automatically at each data byte.

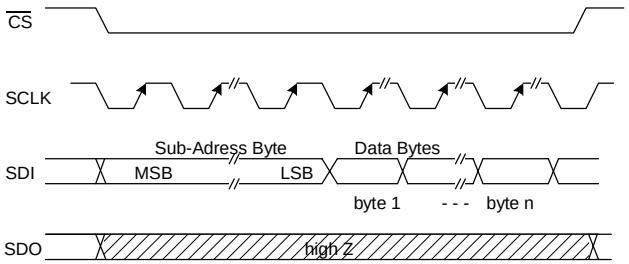



**Fig. 2–4:** SPI Control Port - Write Access

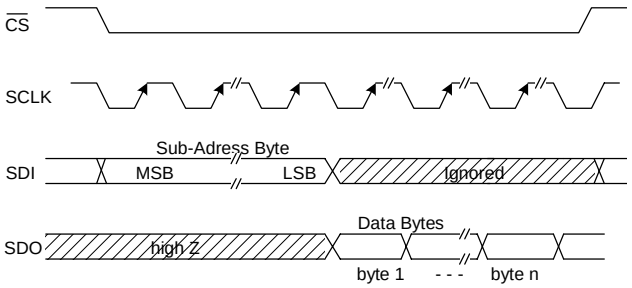



**Fig. 2–5:** SPI Control Port - Read Access

### 2.7. Noise Shaper and Multibit DAC

The input signal is interpolated to a higher sampling rate. A successive noise shaper converts the oversampled audio signal into a multibit noise-shaped signal. This technique results in extremely low quantization noise in the audio band.

### 2.8. Analog Low-Pass

The analog low-pass follows the multibit DAC and is a third order low pass filter with approximately 70 kHz cut-off frequency. It removes the out-of-band components of the oversampled audio signal.

### 2.9. Analog Input

In addition to the digital audio input, the DAC 3560C provides three analog inputs, (AUXL, AUXR, AIN) for stereo and mono signals. The analog audio signals can be mixed to the digital audio signal as well as being used without digital audio. All three analog inputs are equipped with 20 dB to –20 dB gain controls for individual input level adjustments in steps of 2 dB.

### 2.10. Analog Audio Driver Output

The device provides three integrated audio drivers.

**Table 2–5:** Analog Audio Driver Output

| **Integrated Audio Drivers** | |
|---|---|
| Stereo headphone driver | 25 mW at 2.85 V supply<br>80 mW at 5 V supply |
| Mono earpiece driver | 100 mW at 2.85 V supply<br>300 mW at 5 V supply |
| Mono loudspeaker driver | 400 mW at 3 V supply<br>1.1 W at 5 V supply |

All drivers are equipped with analog volume controls, which are individually adjustable from 6 dB to –30 dB in 1.5 dB steps. The earpiece driver and the loudspeaker driver have differential outputs, while the headphone drivers are single-ended. Single-ended drivers usually require a large coupling capacitor to block the DC bias from the headphone. The DAC 3560C provides a headphone common output (HPCM), which eliminates the need for such bulky DC-blocking capacitors. All driver outputs are short-circuit-protected.

### 2.11. LDO

For applications with a noise-critical power supply environment, the DAC 3560C is equipped with an integrated Low-Dropout Voltage Regulator (LDO). The LDO provides a stable 2.85 V output voltage and is intended to supply the headphone and earpiece drivers. With the LDO, the Power Supply Rejection Ratio (PSRR) of the audio outputs is improved to more than 100 dB.

For applications where the LDO cannot be used, e.g., for supply voltages below 2.85 V, it can be disabled via the Mode-Control-Register, (see Section 5.) for details on using the DAC 3560C with or without the internal LDO. The LDO is short-circuit-protected.

### 2.12. Charge Pump

The DAC 3560C offers an internal charge pump circuit that allows to operate the IC with a supply voltage as low as 2.2 V. An additional capacitor must be connected between pin PVDD and pin VLDO for the charge pump to work properly. The switching frequency is far above the audio range and therefore does not interfere with the audio signals. The charge pump must be turned on if the supply voltage of the IC drops below 2.7 V. (see Section 5.) for details on using the DAC 3560C with a lowered supply voltage of 2.2 V.

### 2.13. Reference Block

This block provides the reference level for the analog audio signals. Two modes are possible:

**LDO-Mode:** The audio reference level is fixed to 1.425 V (Pin SREF), which is one half of the LDO output voltage.

**Non-LDO-Mode:** The audio reference level at Pin SREF is derived from an internal voltage divider to VBAT/2.

A capacitor connected between SREF and SGND reduces the noise coming from SREF. In addition, a second capacitor can be connected to pin CF to form a second order noise filter. (See Section 5. for details).

### 2.14. Temperature Overload Protection

The DAC 3560C has an internal temperature overload protection, which disables all audio drivers and the LDO, if the junction temperature exceeds 140 °C. Once the chip has cooled down to 120 °C, the LDO and the audio drivers are enabled again.

### 2.15. Power Management

As the device has more than one signal path, the DAC 3560C offers a Block-Control-Register, which permits individual control over the power state of the signal chain for optimized power consumption. A zero power and a stand-by mode are also provided.

### 2.16. Click and Pop Suppression

The DAC 3560C has on-chip facilities allowing to turn the audio output drivers on or off without audible click and pop transients.

## 3. Control Registers

The DAC 3560C contains 11 registers (all 8 bits). All registers, with the exception of the Reset Register, (write only), allow read and write access.

**Note:** The default value for all registers after software or hardware reset is 0.

### 3.1. Register Map

**Table 3–1:** Register Map Table

| Sub-Address | Register |
|---|---|
| 00h | Reset Register |
| 01h | Block Control Register |
| 02h | Mode Control Register |
| 03h | $I^2S$-Interface Control Register |
| 04h | Left Headphone Volume Control |
| 05h | Right Headphone Volume Control |
| 06h | Earpiece Volume Control |
| 07h | Loudspeaker Volume Control |
| 08h | Left Input Aux Gain Control |
| 09h | Right Input Aux Gain Control |
| 0Ah | Ain Input Gain Control |
| 0Bh...FFh | Reserved |

**Table 3–2:** Register Description

| Name | Sub-Address | Dir | Default after Reset | Function |
|---|---|---|---|---|
| **DACC-Register** | | | | |
| **Reset Register** | **h00** | **W** | **h00** | |
| Reset | h0X | W | 0 | Writing to this Register clears all internal registers to their default reset value |
| **Block Control Register** | **h01** | **RW** | **h00** | **Ignored, if in Standby or Zero Power Mode** |
| PDAC | h01[7] | RW | 0 | 1 = On, 0 = Off (Power DAC) |
| PAIN | h01[6] | RW | 0 | 1 = On, 0 = Off (Power Ain) Gain |
| PAUX | h01[5] | RW | 0 | 1 = On, 0 = Off (Power Aux) Gain |
| PL | h01[4] | RW | 0 | 1 = On, 0 = Off (Power Loudspeaker) Driver |
| PE | h01[3] | RW | 0 | 1 = On, 0 = Off (Power Earpiece) Driver |
| PRH | h01[2] | RW | 0 | 1 = On, 0 = Off (Power Right Headphone) Driver |
| PLH | h01[1] | RW | 0 | 1 = On, 0 = Off (Power Left Headphone) Driver |
| ENHPC | h01[0] | RW | 0 | 1 = On, 0 = Off (Enable Headphone Common Output) Driver |
| **Mode Control Register** | **h02** | **RW** | **h00** | **For details, please refer to Section 5.** |
| – | h02[7] | RW | 0 | Reserved |
| RDWN | h02[6] | RW | 0 | 1 = On, 0 = Off (Ramp down SREF during Standby Mode) |
| CPON | h02[5] | RW | 0 | 1 = On, 0 = Off (Charge pump on (only in NON-LDO Mode) |
| BYPLDO | h02[4] | RW | 0 | 1 = On, 0 = Off (Bypass LDO (only in Standby, Zero Power) |
| SNLDOM | h02[3] | RW | 0 | 1 = On, 0 = Off (Select Non-LDO Mode) |
| SMM | h02[2] | RW | 0 | 1 = Mono, 0 = Stereo (Select Stereo or Mono Mode) |
| PM | h02[1:0] | RW | 0 | PM[1:0]<br>00 Zero Power Mode<br>01 Standby Mode<br>11 Operating Mode<br>10 Reserved |

**Table 3–2:** Register Description, continued

| Name | Sub-Address | Dir | Default after Reset | Function |
|---|---|---|---|---|
| **I2S Interface Control Register** | **h03** | **RW** | **h00** | |
| – | h03[7:5] | RW | 0 | Reserved |
| POL | h03[4] | RW | 0 | Invert Polarity of Word Strobe Input<br>POL=0 - Left Channel → WSI=0<br>POL=1 - Right Channel → WSI=0 |
| DEL | h03[3] | RW | 0 | 1 = Delay, 0 = no Delay (Delay Bit) |
| SR | h03[2:0] | RW | 0 | SR[2:0]<br>000 32 kHz - 48 kHz Sample Rate<br>001 24 kHz - 32 kHz Sample Rate<br>010 16 kHz - 24 kHz Sample Rate<br>011 12 kHz - 16 kHz Sample Rate<br>100 8 kHz - 12 kHz Sample Rate<br>101 6 kHz - 8 kHz Sample Rate<br>110 96 kHz Sample Rate<br>111 192 kHz Sample Rate |
| **Left Headphone Volume Register** | **h04** | **RW** | **h00** | |
| – | h04[7:5] | RW | 0 | Reserved |
| LHV | h04[4:0] | RW | 0 | LHV[4:0]<br>Left Headphone Volume<br>00000 Mute<br>00001 –30 dB<br>----- in steps of 1.5 dB<br>11001 6 dB<br>11011-11111 6 dB |
| **Right Headphone Volume Register** | **h05** | **RW** | **h00** | |
| – | h05[7:5] | RW | 0 | Reserved |
| RHV | h05[4:0] | RW | 0 | RHV[4:0]<br>Right Headphone Volume<br>00000 Mute<br>00001 –30 dB<br>----- in steps of 1.5 dB<br>11001 6 dB<br>11011-11111 6 dB |

**Table 3–2:** Register Description, continued

| Name | Sub-Address | Dir | Default after Reset | Function |
|---|---|---|---|---|
| **Earpiece Volume Register** | **h06** | **RW** | **h00** | |
| – | h06[7:5] | RW | 0 | Reserved |
| EV | h06[4:0] | RW | 0 | EV[4:0]<br>Earpiece Volume<br>00000 Mute<br>00001 –30 dB<br>----- in steps of 1.5 dB<br>11001 6 dB<br>11011-11111 6 dB |
| **Loudspeaker Volume Register** | **h07** | **RW** | **h00** | |
| – | h07[7:5] | RW | 0 | Reserved |
| LV | h07[4:0] | RW | 0 | LV[4:0]<br>Loudspeaker Volume<br>00000 Mute<br>00001 –30 dB<br>----- in steps of 1.5 dB<br>11001 6 dB<br>11011-11111 6 dB |
| **Left Aux Gain Register** | **h08** | **RW** | **h00** | |
| – | h08[7:5] | RW | 0 | Reserved |
| ALV | h08[4:0] | RW | 0 | ALV[4:0]<br>Left AUX Pre-Amplifier Gain<br>00000 Mute<br>00001 –20 dB<br>----- in steps of 2 dB<br>10101 20 dB<br>10110-11111 20 dB |
| **Right AUX Gain Register** | **h09[7:5]** | **RW** | **h00** | |
| – | h09[7:5] | RW | 0 | Reserved |
| ARV | h09[4:0] | RW | 0 | ARV[4:0]<br>Right AUX Pre-Amplifier Gain<br>00000 Mute<br>00001 –20 dB<br>----- in steps of 2 dB<br>10101 20 dB<br>10110-11111 20 dB |

**Table 3–2:** Register Description, continued

| Name | Sub-Address | Dir | Default after Reset | Function |
|---|---|---|---|---|
| **AIN Gain Register** | **h0A[7:5]** | **RW** | **h00** | |
| – | h0A[7:5] | RW | 0 | Reserved |
| AIV | h0A[4:0] | RW | 0 | AIV[4:0]<br>AIN Pre-Amplifier Gain<br>00000 Mute<br>00001 –20 dB<br>----- in steps of 2 dB<br>10101 20 dB<br>10110-11111 20 dB |

## 4. Specifications

### 4.1. Outline Dimensions

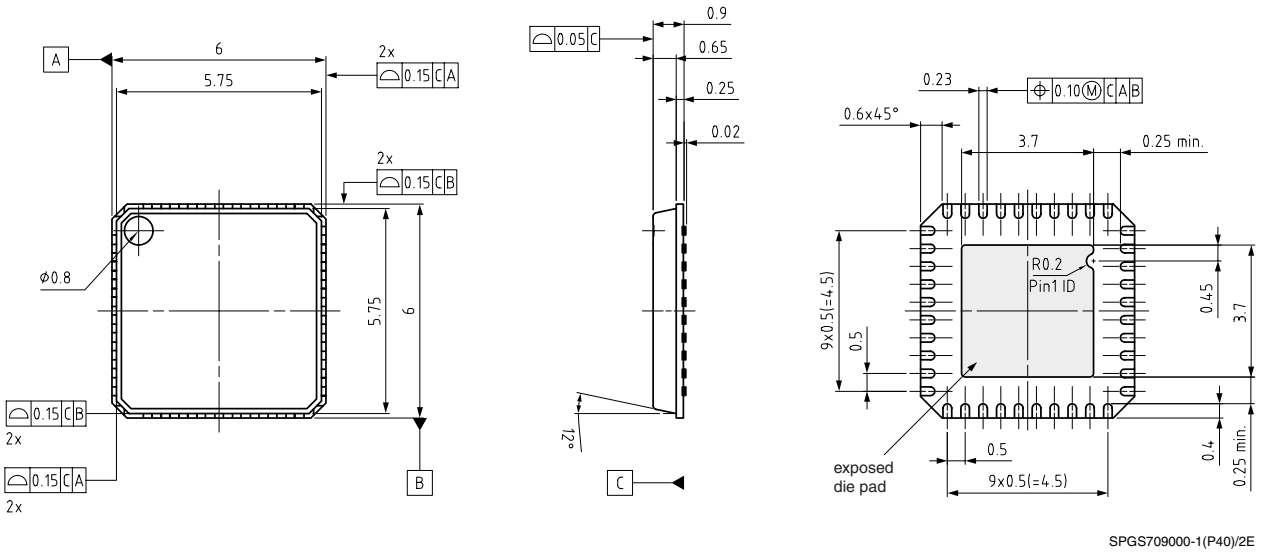



**Fig. 4–1:**
40-Pin Plastic Quad Flat No leads package
**(PQFN40)**
Weight approximately 0.096 g
Dimensions in mm

### 4.2. Pin Connections and Short Descriptions

NC = not connected
LV = leave vacant
I = Input, O = Output, I/O = Input/Output

P = Power
GND = Ground
OBL = obligatory;
connect as described in the circuit diagram

| Pin No. PQFN 40-pin | Pin Name | Type | Connection (If not used) | Short Description |
|---|---|---|---|---|
| 1 | VBAT | P | - | Power Supply |
| 2 | LSVSS1 | P | GND | Loudspeaker Driver Ground |
| 3 | LSP | O | LV | Loudspeaker Differential Positive Output |
| 4 | LSVDD | P | VBAT | Loudspeaker Power Supply Driver |
| 5 | LSN | O | LV | Loudspeaker Differential Negative Output |
| 6 | LSVSS2 | P | GND | Loudspeaker Driver Ground |
| 7 | DVDD | P | - | Digital Power Supply |
| 8 | DVSS | P | GND | Digital Ground |
| 9 | MODE | I | OBL | $I^2C$ / SPI Control Mode Selection |
| 10 | IOVDD | P | - | Digital I/O Power Supply |
| 11 | SDI | I/O | OBL | SPI / Data In ($I^2C$ Data In/Out) |
| 12 | SCLK | I | OBL | SPI / $I^2C$ CLK |
| 13 | SDO | O | LV | SPI / Data Out |
| 14 | $\overline{CS}$ | I | IOVDD | SPI Chip Select (active Low) |
| 15 | DAI | I | GND | $I^2S$ Data In |
| 16 | WSI | I | GND | $I^2S$ Word Strobe Input |
| 17 | CLI | I | GND | $I^2S$ Clock In |
| 18 | $\overline{RES}$ | I | OBL | Reset Input (active Low) |
| 19 | NC | | NC | |
| 20 | NC | | NC | |
| 21 | AIN | I | LV | Analog Mono Input |
| 22 | AUXL | I | LV | Analog AUX Input Left Channel |
| 23 | AUXR | I | LV | Analog AUX Input Right Channel |
| 24 | HPCM | O | LV | Headphone Common Output |
| 25 | HPVSS | P | GND | Headphone Driver Ground |
| 26 | HPL | O | LV | Headphone Output Left Channel |
| 27 | HPR | O | LV | Headphone Output Right Channel |
| 28 | HPVDD | P | VLDO | Headphone Driver Power Supply |

| Pin No. PQFN 40-pin | Pin Name | Type | Connection (If not used) | Short Description |
|---|---|---|---|---|
| 29 | SGND | P | GND | Ground for Audio Signal reference level, Connect to GND |
| 30 | SREF | O | OBL | Audio Signal reference level |
| 31 | CF | O | SREF | Audio Signal reference level |
| 32 | EPVSS2 | P | GND | Earpiece Driver Supply Return, Connect to GND |
| 33 | EPN | O | LV | Earpiece Differential Negative Output |
| 34 | EPVDD | P | VLDO | Earpiece Driver Power Supply |
| 35 | EPP | O | LV | Earpiece Differential Positive Output |
| 36 | EPVSS1 | P | GND | Earpiece Driver Ground |
| 37 | AVSS | P | GND | Analog Ground |
| 38 | PVDD | O | VLDO | Charge Pump Out |
| 39 | CPIN | P | OBL | Charge Pump In |
| 40 | VLDO (AVDD) | P | VBAT | LDO Output, Analog Power Supply |

**Note:** Pins CPIN, EPVDD and HPVDD must be connected to Pin VLDO

### 4.3. Pin Descriptions

#### 4.3.1. Power Supply Pins

The power supply pins are divided into functional regions: LDO region, digital region, digital input region, three analog regions. Two major applications are possible: LDO mode or Non-LDO mode. They are described in detail in Section 5.1. and Section 5.2.

**DVDD, IOVDD, DVSS**
**(see Fig. 4–8, Fig. 4–9, Fig. 4–10):**

– The DVDD and DVSS power supply pair is connected internally with all digital parts of the DAC 3560C.

– The IOVDD and DVSS power supply pair is connected internally with all digital inputs and outputs of the DAC 3560C.

– DVSS is the ground connection for all digital circuits.

**AVSS, PVDD, CPIN (see Fig. 4–3):**
**VBAT, VLDO (see Fig. 4–4):**
VBAT is the input of the internal LDO.
VLDO is the output of the LDO. If the LDO function is not used, VBAT must be connected to VLDO. At PVDD an internal supply can be generated. Pin CPIN must be connected to VLDO. This function is necessary in Non-LDO mode and external power voltages below 2.7 V. At these low supply voltages, an internal charge pump ensures proper functioning of the chip down to 2.2 V. An external capacitor of 47 nF must be connected from PVDD to VLDO. AVSS serves as ground pin for the aforementioned capacitor and must be connected to DVSS.

**HPVDD, HPVSS (see Fig. 4–6, Fig. 4–7)**
The HPVDD and HPVSS pins supply the headphone drivers. HPVDD must be connected to VLDO.
HPVSS must be connected to AVSS.

**EPVDD, EPVSS (see Fig. 4–11)**
The EPVDD and EPVSS pins supply the earpiece drivers. EPVDD must be connected to VLDO.
EPVSS must be connected to AVSS.

**LSVDD, LSVSS (see Fig. 4–12)**
The LSVDD and LSVSS pins supply the loudspeaker drivers. LSVDD must be connected to VBAT.
LSVSS must be connected to AVSS.

### 4.3.2. Analog Reference Pins

**SREF, CF (see Fig. 4–2):**
Reference for analog audio signals. SREF is used as reference for the internal op amps and drivers. There are two modes of usage:
1) LDO mode:
SREF must be blocked against SGND with a 3.3 µF (plus optional 10 nF) capacitor.
CF must be connected to SREF.
The internal reference is fixed at 1.425 V.

2) Non-LDO mode (ratiometric mode):
a) SREF and CF are connected together. Both are blocked against SGND with a 3.3 µF (+ optional 10 nF capacitor). The PSRR of SREF is reduced compared to the Bandgap mode.
b) SREF is blocked against SGND with a 1 µF (+ optional 10 nF) capacitor and CF is blocked with a 1.0 µF capacitor. PSRR is improved with respect to "a".
The internal reference is VLDO/2.

**Note:** SREF can be used as reference input for external op amps, if no current load is applied. Keep the traces at SREF and CF as short as possible to avoid system noise pickup.

**SGND (see Fig. 4–2):**
Reference ground for the internal bandgap and biasing circuits. This pin should be connected to a clean ground potential. Any external distortions on this pin will affect the analog performance of the DAC 3560C. SGND must be connected to AVSS.

### 4.3.3. Analog Audio Pins

**AUXL, AUXR, AIN (see Fig. 4–5):**

These pins provide analog stereo/mono inputs. Auxiliary input signals, e.g. the output of a conventional receiver circuit or the output of a tape recorder can be connected here.
The input gain is programmable between −20 dB and +20 dB in steps of 2 dB.
The input signals have to be connected by capacitive coupling.
Each signal can be mixed to the output of the embedded DAC.

**HPL, HPR, HPCM (see Fig. 4–6, Fig. 4–7):**
The HPL/R pins are connected to the internal headphone drivers. They can be used for single-ended stereo headphones of greater or equal than 16 Ohm. There are two modes of applying the load:

1) Load to ground: Each channel must be coupled capacitively.

2) Load to HPCM: Channels can be coupled directly to HPCM. The common mode buffer at HPCM must be enabled before activating the drivers.

**EPP, EPN (see Fig. 4–11):**
The EPP/N pins are connected to the internal earpiece driver. They can be used for differential mono earpiece speakers of greater than, or equal to, 16 Ohm.

**LSP, LSN (see Fig. 4–12):**
The LSP/N pins are connected to the internal loudspeaker driver. They can be used for differential mono loudspeakers of greater or equal than 4 Ohm.

All analog outputs show a programmable gain range of −30 dB to +6 dB plus Mute.

**Note:** Any occurrence of a short circuit at these pins may result in initialization of the built-in temperature protection unit, which turns off the output drivers. When the short-circuit condition is removed, the drivers will be turned on again.

### 4.3.4. Digital Audio Input Pins

**CLI, DAI , WSI (see Fig. 4–8):**
These three pins are inputs for the digital audio data DAI, frame indication signal WSI, and bit clock CLI. The digital audio data is transmitted in an $I^2S$-compatible format. Audio word lengths of 16 and 32 bits are supported, as well as SONY and Philips $I^2S$ protocol.

### 4.3.5. Control Interface Pins

**SCLK, SDI, SDO, MODE, $\overline{CS}$**
**(see Fig. 4–8, Fig. 4–9, Fig. 4–10):**
Two protocol control modes are possible:

1) $I^2C$ mode:
SCLK and SDI provide the connection to the serial control interface.

2) SPI mode:
Two additional signals are needed:
$\overline{CS}$ serves as the interface chip select.
SDO sends out data after a read command.

MODE toggles between the two control modes.

### 4.3.6. Other Pins

**$\overline{RES}$ (see Fig. 4–8):**
This pin may be used to reset the chip. After power-up it should be raised from DVSS potential to IOVDD level. Signal function is active low.

### 4.4. Pin Configurations

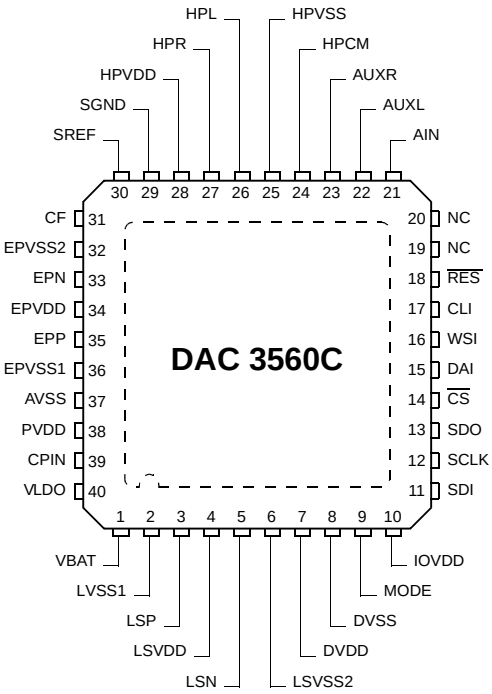



**Fig. 4–2:** PQFN40 package

### 4.5. Pin Circuits

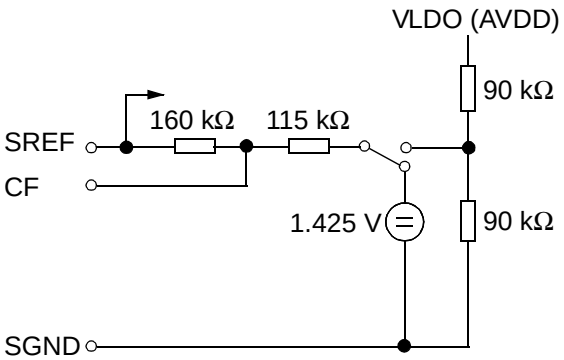



**Fig. 4–3:** Reference Pins: SREF, CF, SGND, VLDO

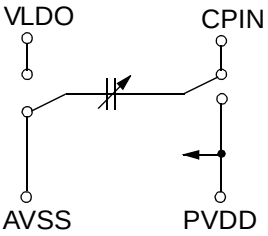



**Fig. 4–4:** Supply Pins: CPIN, PVDD

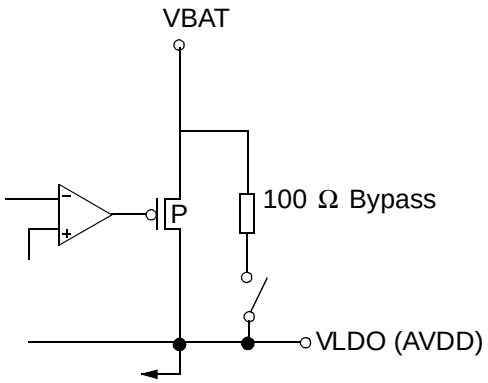



**Fig. 4–5:** Supply Pins: VLDO, VBAT

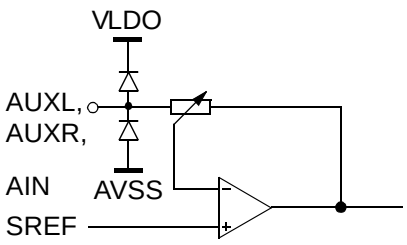



**Fig. 4–6:** Input Pins: AUXL, AUXR, AIN

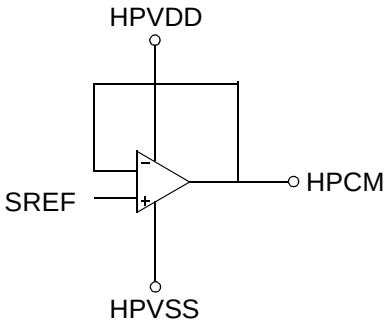



**Fig. 4–7:** Output Pin: HPCM

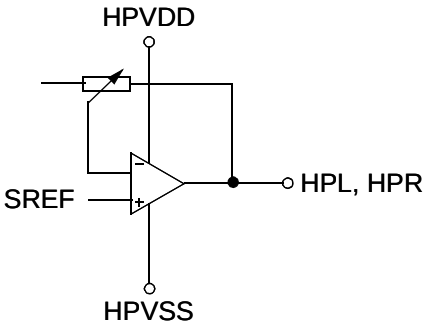



**Fig. 4–8:** Output Pins: HPL, HPR

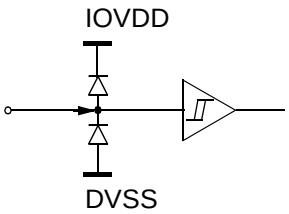



**Fig. 4–9:** Input Pins: Mode, $\overline{CS}$, DAI, WSI, CLI, $\overline{RES}$

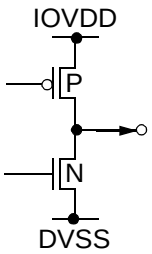



**Fig. 4–10:** Output Pin: SDO

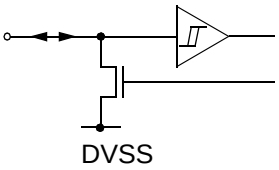



**Fig. 4–11:** In/Out Pins: SDI, SCLK

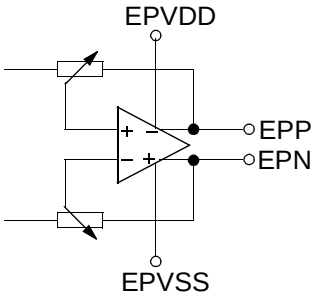



**Fig. 4–12:** Output Pins: EPP, EPN, EPVDD, EPVSS

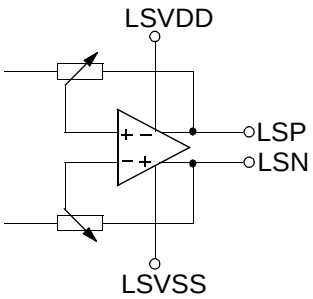



**Fig. 4–13:** Output Pins: LSP, LSN, LSVDD, LSVSS

### 4.6. Electrical Characteristics

#### 4.6.1. Absolute Maximum Ratings

| Symbol | Parameter | Pin Name | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{SUP}$ | Supply Voltage | VBAT, LSVDD, VLDO, HPVDD, EPVDD, CPIN, DVDD, IOVDD | –0.3 | 6 | V |
| $V_{Iana}$ | Analog Input Voltages | AIN, AUXL, AUXR, SREF, CF | –0.3 | VLDO+0.3 | V |
| $V_{Idig}$ | Digital Input Voltages | MODE, SDO, SDI, SCLK, CS, DAI, WSI, CLI, RES | –0.3 | IOVDD+0.3 | V |
| $V_{II2C}$ | | SDI, SCLK | –0.3 | 6 | V |
| $I_{Iana}$ | Analog Input Currents | AIN, AUXL, AUXR, SREF, CF | –5 | 5 | mA |
| $I_{Idig}$ | Digital Input Currents | MODE, SDO, SDI, SCLK, CS, DAI, WSI, CLI, RES | –5 | 5 | mA |
| $I_{Odig}$ | Digital Output Currents | SDO, SDI, SCLK | –50 | 50 | mA |
| $I_{OLDO}$ | Analog Output Currents | LDO | internally limited | 50 | mA |
| $I_{OHP}$ | | HPL, HPR, HPCM | | internally limited | mA |
| $I_{OEP}$ | | EPN, EPP | | | |
| $I_{OLS}$ | | LSP, LSN | | | |
| $T_S$ | Storage Temperature | | –40 | 125 | °C |
| $T_J$ | Junction Temperature | | –40 | 125 | °C |
| $P_{TOT}$ | Continuous Power Dissipation at TA = 85 °C, exposed pad soldered to PCB | | | 1 | W |

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

**Note:** Positive currents flow into the device

### 4.6.2. Recommended Operating Conditions

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient Operating Temperature<br>-Operating Conditions<br>-Extended Temperature Range[1)] | | <br>0<br>–40 | | <br>85<br>85 | <br>°C<br>°C |
| $V_{SUPA1}$ | Analog Supply Voltage (Non-LDO mode)<br>Charge pump: on | VBAT, LSVDD, VLDO, HPVDD, EPVDD, CPIN | 2.2 | | 3.4 | V |
| | Analog Supply Voltage (Non-LDO mode)<br>Charge pump: off | | 2.7 | | 5.5 | V |
| $V_{SUPA2}$ | Analog Supply Voltage (LDO mode) | VBAT, LSVDD | 3 | | 5.5 | V |
| $V_{SUPD}$ | Digital Supply Voltage | DVDD | 2.2 | | 5.5 | V |
| $V_{SUPIO}$ | Digital Interface Voltage | IOVDD | 1.8 | | 5.5 | V |
| $C_{LDOout}$ | LDO Output Capacitor | VLDO, use Ceramic X7R, X5R | 0.8 | 1.0 | 1.3 | µF |
| $C_{LDOin}$ | LDO Input Capacitor | VBAT | 0.47 | | | µF |
| $C_{Pout}$ | Charge Pump Output Capacitor | PVDD, VLDO | | 47 | | nF |
| $C_{Ain}$ | Analog Input Coupling Capacitor | AUXL, AUXR, AIN | 470 | | | nF |
| $C_{Sref}$ | SREF Bypass Capacitor | SREF | 3.3 | | | µF |
| $R_{LHP}$ | Headphone Load Resistance | HPL, HPR, HPCM | 16 | 32 | | Ω |
| $R_{LEP}$ | Earpiece Load Resistance | EPP, EPN | 16 | 32 | | Ω |
| $R_{LS}$ | Loudspeaker Load Resistance | LSP, LSN | 4 | 8 | | Ω |

[1)] The functionality of the device in the “Extended Temperature Range” was checked by electrical characterization on sample base. Data sheet parameters are valid for “operating conditions” only.

### 4.6.3. Characteristics (LDO Mode)

Unless noted otherwise: LSVDD = VBAT = 3.6 V, EPVDD = HPVDD = CPIN = PVDD = VLDO = 2.85 V (LDO-mode), $T_A$ = 0 °C ...85 °C. Typical values are at $T_A$ = 25 °C.

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **POWER MANAGEMENT, LDO** | | | | | | | |
| $V_{LDO}$ | LDO Output Voltage in Operational Mode | VLDO | 2.75 | 2.85 | 2.95 | V | no load connected |
| $V_{LDO}$ | LDO Output Voltage in Standby Mode | VLDO | 2.75 | 2.85 | 2.95 | V | LDO not bypassed, no load connected |
| | | | VBAT | | | V | LDO bypassed with internal 100Ω switch, no load connected |
| $V_{LDO}$ | LDO Output Voltage in Zero Power Mode | VLDO | HIGH-Z | | | V | LDO not bypassed |
| | | | VBAT | | | V | LDO bypassed with internal 100Ω switch, no load connected |
| $I_{LDO}$ | LDO Output Current | VLDO | | | 260 | mA | |
| $V_{Drop}$ | LDO Drop Out Voltage | VBAT, VLDO | | 70 | | mV | $I_{load}$ = 100 mA |
| $I_{Short}$ | LDO Short Circuit Current | VLDO | | 650 | | mA | VLDO = 0V, Standby or Operational Mode, LDO not bypassed |
| $I_{SupTot}$ | Supply Current | VBAT, LSVDD, VLDO, EPVDD, HPVDD, CPIN, PVDD, IOVDD, DVDD | | | 10 | µA | Zero Power Mode |
| | | | | 170 | | µA | Standby Mode, LDO bypassed, HPCM-Output enabled |
| | | | | 350 | | µA | Standby Mode, LDO bypassed, HPCM-Output off |
| | | | | 450 | | µA | Standby Mode, LDO on, HPCM-Output enabled |
| | | | | 620 | | µA | Standby Mode, LDO on, HPCM-Output off |
| | | | See Table 4–1. | | | | Operational Mode |
| $T_{TS}$ | Thermal Shutdown Temperature | | 125 | 140 | 160 | °C | |
| $H_{TS}$ | Thermal Shutdown Hysteresis | | | 20 | | °C | |
| **ANALOG AUDIO INPUTS - AIN, AUXL, AUXR** | | | | | | | |
| $V_{AI1}$ | 0 dB (Full Scale) Input Level | AIN, AUXL, AUXR | | 2.04 | | $V_{pp}$ | Gains set to 0 dB |
| $V_{AI2}$ | Input Clipping Level | AIN, AUXL, AUXR | | 2.85 | | $V_{pp}$ | Gains set to –20 dB |
| $R_I$ | Input Resistance | AIN, AUXL, AUXR | 9 | 12.5 | 15 | kΩ | Gain = +20 dB |
| | | | 57 | 69 | 83 | | Gain = 0 dB |
| | | | 100 | 125 | 150 | | Gain = –20 dB |
| $G_{AI}$ | Gain Setting Range | AIN, AUXL, AUXR | –20 | | 20 | dB | |
| $d_{GAI}$ | Gain Step Size | AIN, AUXL, AUXR | | ±2 | | dB | |

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $E_{GAI}$ | Gain Step Size Error | AIN, AUXL, AUXR | −0.5 | | 0.5 | dB | |
| **ANALOG AUDIO OUTPUTS – HEADPHONE, EARPIECE, LOUDSPEAKER** | | | | | | | |
| $G_{AO}$ | Volume Range | HPL, HPR, EPP, EPN, LSP, LSN | −30 | | 6 | dB | |
| $dG_{AO}$ | Volume Step Size | HPL, HPR, EPP, EPN, LSP, LSN | | ±1.5 | | dB | |
| $E_{GAO}$ | Volume Step Size Error | HPL, HPR, EPP, EPN, LSP, LSN | −0.5 | | 0.5 | dB | |
| $P_{HP}$ | Headphone Output Power | HPL, HPR, (HPCM) | | 25 (22) | | mW | THD < 0.1%, f=1 kHz, $R_L$= 32 Ω |
| $P_{EP}$ | Earpiece Output Power | EPP, EPN | | 100 | | mW | THD < 0.2%, f=1 kHz, $R_L$= 32 Ω (one channel) |
| $P_{LS}$ | Loudspeaker Output Power | LSP, LSN | | 410 | | mW | THD < 1%, f=1 kHz, $R_L$= 8 Ω |
| $I_{HPshort}$ | Headphone Short-circuit Current | HPL, HPR, HPCM, VLDO, AVSS | 0.1 | 0.45 | | A | not tested |
| $I_{EPshort}$ | Earpiece Short-circuit Current | EPP, EPN, VLDO, AVSS | 0.15 | 0.5 | | A | not tested |
| $I_{LSshort}$ | Loudspeaker Short-circuit Current | LSP, LSN, VLDO, AVSS | 0.5 | 1.2 | | A | not tested |
| **REFERENCES** | | | | | | | |
| $V_{OREF1}$ | Output Signal Reference Level | HPL, HPR, HPCM, EPP, EPN | | 1.425 | | V | SREF settled |
| $V_{OREF2}$ | Output Signal Reference Level | LSP, LSN | | 1.5 | | V | SREF settled |
| **SIGNAL CHAINS – DYNAMIC PERFORMANCE** | | | | | | | |
| $F_{sample}$ = 48 kHz with 24-Bit data,<br>Bandwidth = 20 Hz…20 kHz,<br>Values in dB are unweighted, values in dBA are A-weighted. | | | | | | | |
| $V_{AOHP}$ | 0dB (full scale) Output Level Headphone | HPL, HPR | | 2.04 | | $V_{pp}$ | Gains, Volumes = 0 dB. No load connected. |
| $V_{AOEP}$ | 0dB (full scale) Output Level Earpiece | EPP, EPN, | | 4.08 | | $V_{pp}$ | Gains, Volumes = 0 dB. No load connected. |
| $V_{AOLS}$ | 0dB (full scale) Output Level Loudspeaker | LSP, LSN | | 4.08 | | $V_{pp}$ | Gains, Volumes = 0 dB. No load connected. |
| $DR_{DA}$<br>$DR_{HP}$ | Dynamic Range, Digital to Analog Out | HPL, HPR, (HPCM) , EPP, EPN, LSP, LSN | | 98<br>94 | | dBA<br>dB | Digital to Headphone |
| $DR_{DA}$<br>$DR_{EP}$ | | | | 99<br>95 | | dBA<br>dB | Digital to Earpiece |
| $DR_{DA}$<br>$DR_{LS}$ | | | | 99<br>95 | | dBA<br>dB | Digital to Loudspeaker |
| $DR_{AA}$<br>$DR_{HP}$ | Dynamic Range, Analog to Analog Out | AIN, AUXL, AUXR, HPL, HPR, HPCM, EPP, EPN, LSP, LSN | | 98<br>94 | | dBA<br>dB | Analog to Headphone, DAC off |
| $DR_{AA}$<br>$DR_{EP}$ | | | | 99<br>96 | | dBA<br>dB | Analog to Earpiece, DAC and headphone off |
| $DR_{AA}$<br>$DR_{LS}$ | | | | 98<br>96 | | dBA<br>dB | Analog to Loudspeaker, DAC and headphone off |

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $THD_{HP}$ | THD+N | HPL, HPR, (HPCM) | | –76 (–68) | | dB | Headphone, $R_L$ = 32 Ω, $P_{OUT}$ = 15 mW |
| $THD_{EP}$ | | EPP, EPN | | –69 | | dB | Earpiece, $R_L$ = 32 Ω, $P_{OUT}$ = 50 mW |
| $THD_{LS}$ | | LSP, LSN | | –63 | | dB | Loudspeaker, $R_L$ = 8 Ω, $P_{OUT}$ = 200 mW |
| LM | Mute Level | HPL, HPR, (HPCM), EPP, EPN, LSP, LSN | | –108 | | dBV | Headphone, volumes muted, Earpiece, Loudspeaker |
| $PSRR_{HP}$ | PSRR | VBAT, HPL, HPR, (HPCM) | | 115 | | dB | Headphone, f = 1 kHz, VBAT > 3 V, including LDO-Isolation $V_{RIPPLE,peak}$ = 0.25 V Zero-Audio Signal |
| $PSRR_{EP}$ | PSRR | VBAT, EPP, EPN | | 105 | | dB | Earpiece, f = 1 kHz, VBAT > 3 V, including LDO-Isolation $V_{RIPPLE,peak}$ = 0.25 V Zero-Audio Signal |
| $PSRR_{LS}$ | PSRR | VBAT, LSP, LSN | tbd | 93 | | dB | Loudspeaker, f = 1 kHz, VBAT > 3 V $V_{RIPPLE,peak}$ = 0.25 V Zero-Audio Signal |

### 4.6.4. Characteristics (Non-LDO Mode)

Unless noted otherwise: LSVDD = VBAT = EPVDD = HPVDD = CPIN = VLDO = 2.2 V... 5.5 V (Non-LDO-mode), $T_A$ = 0 °C ...85 °C. Typical values are at $T_A$ = 25 °C.

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **POWER MANAGEMENT, LDO** | | | | | | | |
| $I_{SupTot}$ | Supply Current at 2.2 V | VBAT, LSVDD, VLDO, EPVDD, HPVDD, CPIN, PVDD, IOVDD, DVDD | | | 10 | µA | Zero Power Mode |
| | | | | 185 | | µA | Standby Mode, HPCM-Output enabled |
| | | | | 355 | | µA | Standby Mode, HPCM-Output off |
| | | | | | | | |
| $I_{SupTot}$ | Supply Current at 5 V | VBAT, LSVDD, VLDO, EPVDD, HPVDD, CPIN, PVDD, IOVDD, DVDD | | | 10 | µA | Zero Power Mode |
| | | | | 235 | | µA | Standby Mode, HPCM-Output enabled |
| | | | | 420 | | µA | Standby Mode, HPCM-Output off |
| | | | | | | | |
| **ANALOG AUDIO INPUTS - AIN, AUXL, AUXR** | | | | | | | |
| $V_{AI1}$ | 0 dB (Full Scale) Input Level | AIN, AUXL, AUXR | | 1.43 x $V_{LDO}$/2 | | $V_{pp}$ | Gains set to 0 dB |
| $V_{AI2}$ | Input Clipping Level | AIN, AUXL, AUXR | | $V_{LDO}$ | | $V_{pp}$ | Gains set to –20 dB |
| **ANALOG AUDIO OUTPUTS – HEADPHONE, EARPIECE, LOUDSPEAKER** | | | | | | | |
| $P_{HP}$ | Headphone Output Power at 2.2 V | HPL, HPR, (HPCM) | | 12 | | mW | THD < 0.1%, f=1 kHz, $R_L$= 32 Ω |
| $P_{EP}$ | Earpiece Output Power at 2.2 V | EPP, EPN | | 50 | | mW | THD < 0.2%, f=1 kHz, $R_L$= 32 Ω |
| $P_{LS}$ | Loudspeaker Output Power at 2.2 V | LSP, LSN | | 170 | | mW | THD < 1%, f=1 kHz, $R_L$= 8 Ω |
| $P_{HP}$ | Headphone Output Power at 5 V | HPL, HPR, (HPCM) | | 78 | | mW | THD < 0.1%, f=1 kHz, $R_L$= 32 Ω |
| $P_{EP}$ | Earpiece Output Power at 5 V | EPP, EPN | | 300 | | mW | THD < 0.2%, f=1 kHz, $R_L$= 32 Ω |
| $P_{LS}$ | Loudspeaker Output Power at 5 V | LSP, LSN | | 1.1 | | W | THD < 1%, f=1 kHz, $R_L$= 8 Ω |
| **REFERENCES** | | | | | | | |
| $V_{OREF1}$ | Output Signal Reference Level | HPL, HPR, HPCM, EPP, EPN | | $V_{LDO}$/2 | | V | SREF settled |
| $V_{OREF2}$ | Output Signal Reference Level | LSP, LSN | | $V_{LDO}$/2 | | V | SREF settled |
| **SIGNAL CHAINS – DYNAMIC PERFORMANCE** | | | | | | | |
| $F_{sample}$ = 48 kHz with 24-Bit data,<br>Bandwidth = 20 Hz…20 kHz,<br>Values in dB are unweighted, values in dBA are A-weighted. | | | | | | | |
| $V_{AOHP}$ | 0 dB (Full scale) Output Level Headphone | HPL, HPR | | 1.43 x $V_{LDO}$/2 | | $V_{pp}$ | Gains, Volumes = 0 dB. No load connected. |

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{AOEP}$ | 0 dB (Full scale) Output Level Earpiece | EPP, EPN, | | 2.86 x $V_{LDO}/2$ | | $V_{pp}$ | Gains, Volumes = 0 dB. No load connected. |
| $V_{AOLS}$ | 0 dB (Full scale) Output Level Loudspeaker | LSP, LSN | | 2.86 x $V_{LDO}/2$ | | $V_{pp}$ | Gains, Volumes = 0 dB. No load connected. |
| $DR_{DA}$<br>$DR_{HP}$ | Dynamic Range, Digital to Analog Out at 2.2 V | HPL, HPR, (HPCM), EPP, EPN, LSP, LSN | | 96<br>93 | | dBA<br>dB | Digital to Headphone |
| $DR_{DA}$<br>$DR_{EP}$ | | | | 98<br>94 | | dBA<br>dB | Digital to Earpiece |
| $DR_{DA}$<br>$DR_{LS}$ | | | | 98<br>94 | | dBA<br>dB | Digital to Loudspeaker |
| $DR_{DA}$<br>$DR_{HP}$ | Dynamic Range, Digital to Analog Out at 5 V | HPL, HPR, (HPCM), EPP, EPN, LSP, LSN | | 103<br>99 | | dBA<br>dB | Digital to Headphone |
| $DR_{DA}$<br>$DR_{EP}$ | | | | 102<br>98 | | dBA<br>dB | Digital to Earpiece |
| $DR_{DA}$<br>$DR_{LS}$ | | | | 94<br>91 | | dBA<br>dB | Digital to Loudspeaker |
| $DR_{AA}$<br>$DR_{HP}$ | Dynamic Range, Analog to Analog Out at 2.2 V | AIN, AUXL, AUXR, HPL, HPR, HPCM, EPP, EPN, LSP, LSN | | 96<br>92 | | dBA<br>dB | Analog to Headphone, DAC off |
| $DR_{AA}$<br>$DR_{EP}$ | | | | 98<br>94 | | dBA<br>dB | Analog to Earpiece, DAC and headphone off |
| $DR_{AA}$<br>$DR_{LS}$ | | | | 95<br>92 | | dBA<br>dB | Analog to Loudspeaker, DAC and headphone off |
| $DR_{AA}$<br>$DR_{HP}$ | Dynamic Range, Analog to Analog Out at 5 V | AIN, AUXL, AUXR, HPL, HPR, HPCM, EPP, EPN, LSP, LSN | | 104<br>100 | | dBA<br>dB | Analog to Headphone, DAC off |
| $DR_{AA}$<br>$DR_{EP}$ | | | | 103<br>99 | | dBA<br>dB | Analog to Earpiece, DAC and headphone off |
| $DR_{AA}$<br>$DR_{LS}$ | | | | 94<br>91 | | dBA<br>dB | Analog to Loudspeaker, DAC and headphone off |
| $THD_{HP}$ | THD+N at 2.2 V | HPL, HPR | | –71 | | dB | Headphone, $R_L$= 32 Ω, $P_{OUT}$ = 8 mW |
| $THD_{HP}$ | | HPL, HPR, (HPCM) | | –67 | | dB | Headphone + HPCM, $R_L$= 32 Ω, $P_{OUT}$ = 8 mW |
| $THD_{EP}$ | | EPP, EPN | | –69 | | dB | Earpiece, $R_L$= 32 Ω, $P_{OUT}$ = 30 mW |
| $THD_{LS}$ | | LSP, LSN | | –62 | | dB | Loudspeaker, $R_L$=8 Ω, $P_{OUT}$ = 130 mW |
| $THD_{HP}$ | THD+N at 5 V | HPL, HPR | | –82 | | dB | Headphone, $R_L$= 32 Ω, $P_{OUT}$ = 50 mW |
| $THD_{HP}$ | | HPL, HPR, (HPCM) | | –74 | | dB | Headphone + HPCM, $R_L$= 32 Ω, $P_{OUT}$ = 50 mW |
| $THD_{EP}$ | | EPP, EPN | | –76 | | dB | Earpiece, $R_L$= 32 Ω, $P_{OUT}$ = 140 mW |
| $THD_{LS}$ | | LSP, LSN | | –63 | | dB | Loudspeaker, $R_L$=8 Ω, $P_{OUT}$ = 600 mW |
| $PSRR_{HP}$ | PSRR | VBAT, HPL, HPR, (HPCM) | | 68 | | dB | Headphone, f = 1 kHz, |
| $PSRR_{EP}$ | | VBAT, EPP, EPN | | 70 | | dB | Earpiece, f = 1 kHz |
| $PSRR_{LS}$ | | VBAT, LSP, LSN | | 70 | | dB | Loudspeaker, f = 1 kHz |

### 4.6.5. Terminology

1. Dynamic range (dB): DR is a measure of the difference between the highest and lowest portions of a signal. Normally, a THD+N measurement at 60 dB below full scale. The measured signal is then corrected by adding the 60 dB to it.
   (e.g. THD+N at −60 dB = −35 dB, DR = 95 dB).
2. THD+N (dB): Is a ratio, of the RMS values of (Noise + Distortion)/Signal at a given output level or output power.
3. Channel Separation (dB): Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full-scale signal down one channel and measuring the other.

### 4.6.6. I²C Bus Characteristics

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{I2CIL}$ | I²C BUS Input Low Voltage | SCLK, SDI | | | 0.3 | IOVDD | |
| $V_{I2CIH}$ | I²C BUS Input High Voltage | | 0.65 | | | IOVDD | |
| $t_{I2C1}$ | I²C START Condition Setup Time | | 120 | | | ns | |
| $t_{I2C2}$ | I²C STOP Condition Setup Time | | 120 | | | ns | |
| $t_{I2C5}$ | I²C Data Setup Time before Rising Edge of Clock | | 55 | | | ns | |
| $t_{I2C6}$ | I²C Data Hold Time after Falling Edge of Clock | | 55 | | | ns | |
| $t_{I2C3}$ | I²C Clock Low Pulse Time | SCLK | 500 | | | ns | |
| $t_{I2C4}$ | I²C Clock High Pulse Time | | 500 | | | ns | |
| $f_{I2C}$ | I²C BUS Frequency | | | | 1.0 | MHz | |
| $V_{I2COL}$ | I²C Data Output Low Voltage | SCLK, SDI | | | 0.4 | V | $I_{I2COL}$ = 3 mA |
| $I_{I2COH}$ | I²C Data Output High Leakage Current | | | | 1.0 | µA | $V_{I2COH}$ = 5 V |
| $t_{I2COL1}$ | I²C Data Output Hold Time after Falling Edge of Clock | | 15 | | | ns | |
| $t_{I2COL2}$ | I²C Data Output Setup Time before Rising Edge of Clock | | 100 | | | ns | $f_{I2C}$ = 1 MHz |

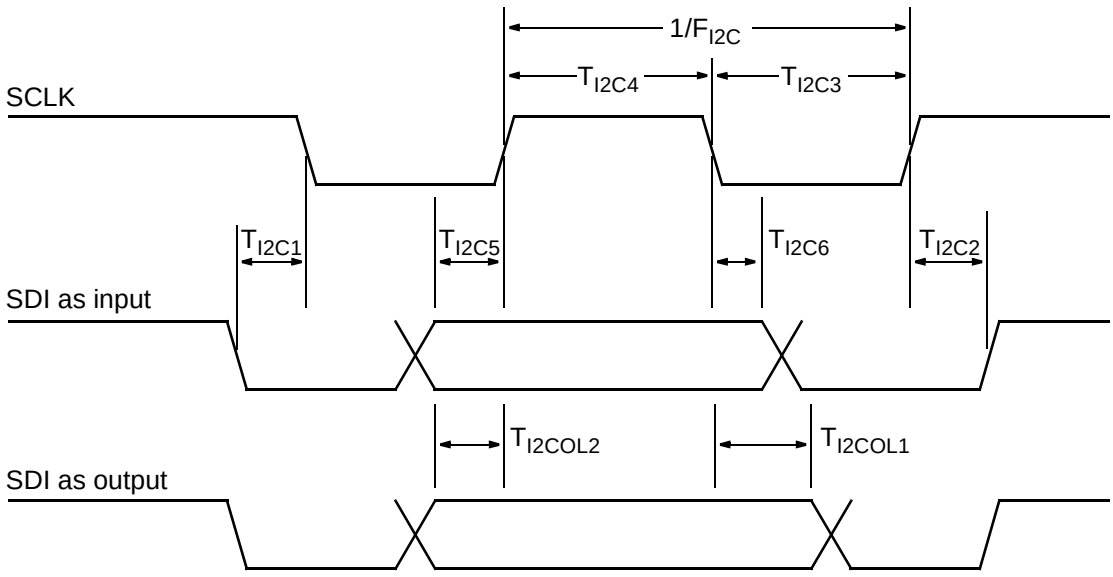
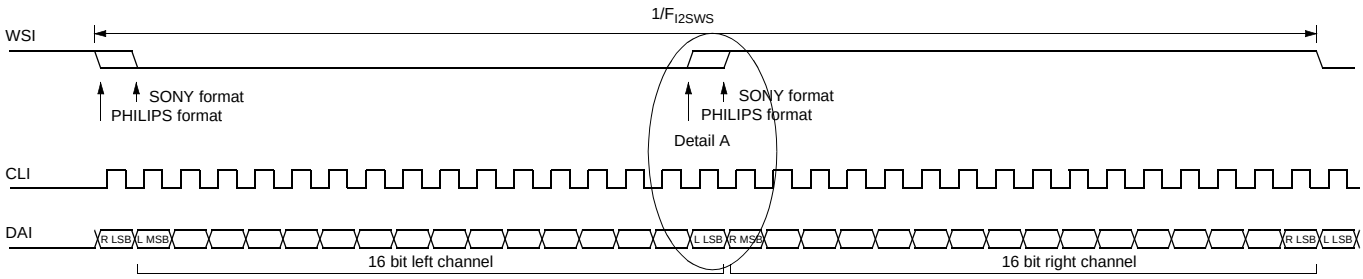



**Fig. 4–14:** I²C bus timing diagram

### 4.6.6.1. $I^2S$ Bus Characteristics

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{I2SIL}$ | Input Low Voltage | DAI CLI WSI | | | 0.2 | IOVDD | |
| $V_{I2SIH}$ | Input High Voltage | | 0.65 | | | IOVDD | |
| $Z_{I2SI}$ | Input Impedance | | | | 5 | pF | |
| $I_{LEAKI2S}$ | Input Leakage Current | | –1 | | 1 | µA | 0 V < $U_{INPUT}$ < IOVDD |
| $t_{I2S1}$ | $I^2S$ Input Setup Time before Rising Edge of CLI | DAI WSI | 10 | | | ns | for details see Fig. 4–15 ( $I^2S$ interface) |
| $t_{I2S2}$ | $I^2S$ Input Hold Time after Rising Edge of CLI | | 20 | | | ns | |
| $R_{CLI}$ | $I^2S$ Clock Input Ratio | | 0.9 | | 1.1 | | |
| $F_{CLI}$ | $I^2S$ Clock Frequency | CLI,DAI | | | 12.3 | MHz | 32 bit, $F_{sample}$ = 192 kHz |




Detail A

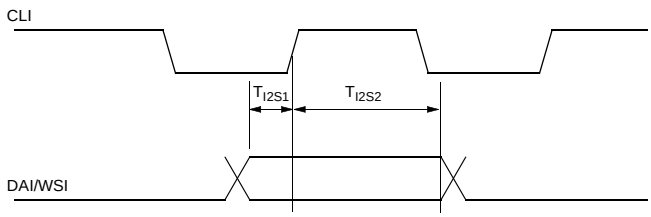



**Fig. 4–15:** $I^2S$ timing diagram

### 4.6.6.2. SPI-Bus Characteristics

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{SPIIL}$ | Input Low Voltage | SDI<br>SCLK | | | 0.2 | IOVDD | |
| $V_{SPIIH}$ | Input High Voltage | | 0.65 | | | IOVDD | |
| $Z_{SPII}$ | Input Impedance | | | | 5 | pF | |
| $I_{LEAKSPI}$ | Input Leakage Current | | –1 | | 1 | µA | 0 V < $U_{INPUT}$< IOVDD |
| $t_{SPI1}$ | SPI Input Setup Time before Rising Edge of SCLK | SDI<br>$\overline{CS}$ | 10 | | | ns | |
| $t_{SPI2}$ | SPI Input Hold Time after Rising Edge of SCLK | | 40 | | | ns | |
| $R_{CLI}$ | SPI Clock Input Ratio | | 0.9 | | 1.1 | | |
| $V_{SPIOL}$ | SPI Output Low Voltage | SDO | | | 0.4 | V | $I_{SPIOL}$ = 0.5 mA, IOVDD= 1.8 V |
| $V_{SPIOH}$ | SPI Output High Voltage | | 1.2 | | | V | $I_{SPIOH}$ = –0.5 mA IOVDD = 1.8 V |
| $f_{SCLK1}$ | SPI Clock Frequency, read access | SCLK, SDI, SDO | | 7 | tbd | MHz | $C_L$ = 20 pF, IOVDD = 3.3 V |
| | | | | tbd | tbd | MHz | $C_L$ = 20 pF, IOVDD = 1.8 V |
| $f_{SCLK2}$ | SPI Clock Frequency, write access | SCLK, SDI | | 14 | tbd | MHz | $C_L$ = 20 pF, IOVDD = 3.3 V |
| | | | | tbd | tbd | MHz | $C_L$ = 20 pF, IOVDD = 1.8 V |

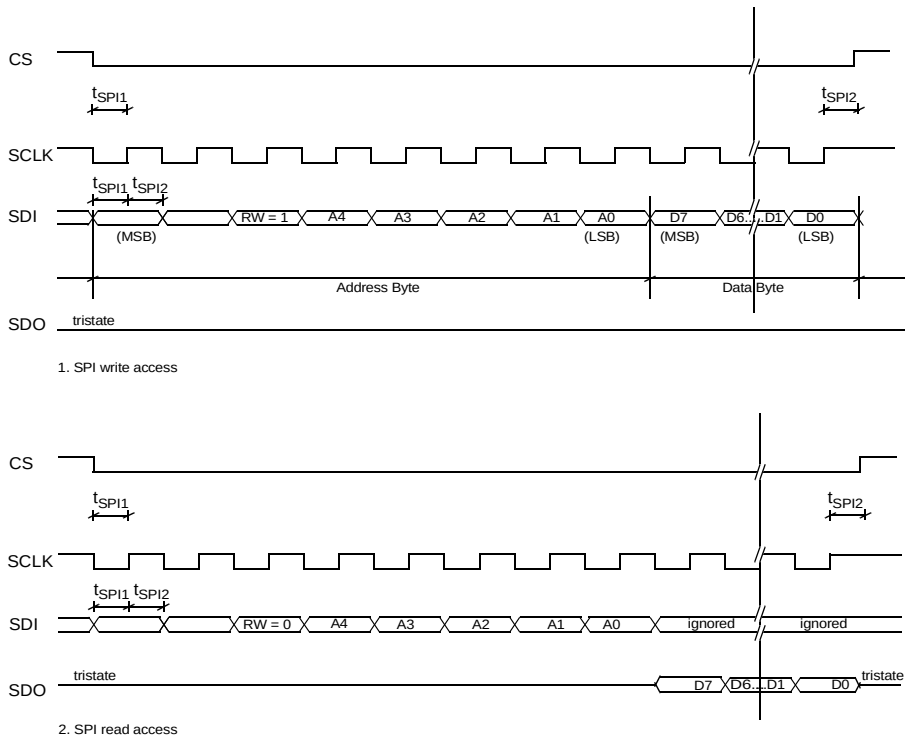



**Fig. 4–16:** SPI write and read access

### 4.6.7. Power Consumption (LDO Mode)

LSVDD=VBAT= 3.6 V, EPVDD=HPVDD=CPIN=PVDD=VLDO= 2.85 V, DVDD = 2.2 V, IOVDD = 1.8 V.
Typical Values, Operational Mode.

**Table 4–1:** Current Consumption Examples (Operational Mode)

| Control Bits | A | B | C | D | E | F | G | H | I | Description |
|---|---|---|---|---|---|---|---|---|---|---|
| SMM | | | X | X | X | X | | | | Select mono mode |
| PDAC | X | X | X | X | | | | | X | Power DAC |
| PAIN | | | | | X | X | | | X | Power AIN input |
| PAUX | | | | | | | X | X | X | Power AUX input |
| PL | | | X | | X | | | | X | Power Loudspeaker |
| PEP | | | | X | | X | | | X | Power Earpiece |
| PRHP | X | X | | | | | X | X | X | Power Headphone Left |
| PLHP | X | X | | | | | X | X | X | Power Headphone Right |
| ENHPC | | X | | | | | | X | X | Enable Headphone Common Driver |
| Current Consumption | | | | | | | | | | Unit |
| Analog [1)] | 7.5 | 8.7 | 4.3 | 4.7 | 3.1 | 3.4 | 6.1 | 7.3 | 13 | mA |
| DVDD [2)] | 0.32 | | 0.2 | | 0 | 0 | 0 | 0 | 0.32 | mA |
| IOVDD [2)] | < 10 | | | | | | | | | µA |

All figures are quiescent currents with zero audio signal, no load connected.

[1)] Including all analog supply pins: VBAT, LSVDD, VLDO, EPVDD, HPVDD, CPIN, PVDD
[2)] $I^2S$ digital audio data received with $f_{sample}$ = 48 kHz, 16-bit word length, CLI=1.536 Mhz.

A) Stereo D/A → Headphone L/R
B) Stereo D/A → Headphone L/R + Headphone Common
C) Mono D/A → Loudspeaker
D) Mono D/A → Earpiece
E) AIN → Loudspeaker
F) AIN → Earpiece
G) AUX → Headphone L/R
H) AUX → Headphone L/R + Headphone Common
I) All signal chains on, stereo mode

## 5. Detailed Mode Description

The DAC 3560C features many modes of operation, which can be set for a targeted application using the internal registers. Also, some external components and pin-to-pin connections may differ from application to application – mainly depending on whether the internal LDO is used or not. A detailed description of these features is given below.

### 5.1. LDO Mode, Using the internal Low-Dropout Regulator

The SNLDOM-Function bit in the MODE Control Register controls the operation of the DAC 3560C with, or without, use of the internal LDO. The default setting selects the LDO mode. The LDO then delivers a stable 2.85 V at its output when the device is in Stand-by or Operational Mode. The signal reference level for the audio outputs is 1.425 V (Pin SREF) except for the loudspeaker output, which has a reference level of 1.5 V. The LDO is intended to supply the headphone and the earpiece driver. Connect the supply pins of these drivers (HPVDD, EPVDD) to the LDO output (VLDO). Also connect the pins from the charge pump (CPIN, PVDD) to the LDO output. The charge pump is disabled when the DAC 3560C is in LDO Mode. Using the LDO increases the PSRR of the headphone and earpiece outputs in respect to the battery line (VBAT) to more than 100 dB. The input voltage range for full performance of the LDO is 5.5 V to 3.0 V.

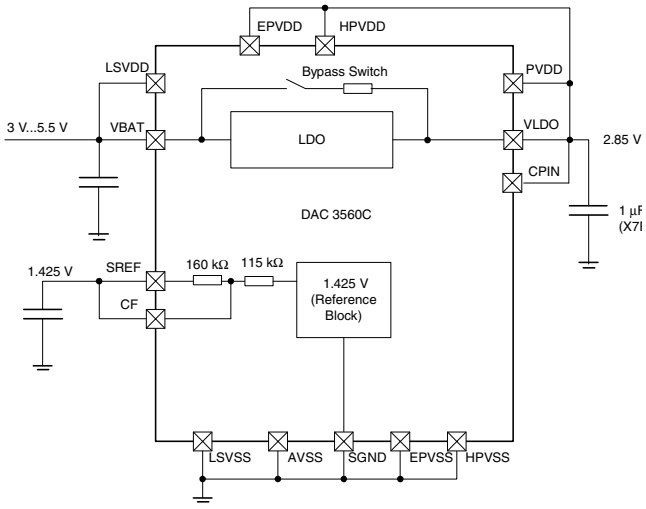



**Fig. 5–1:** Simplified application diagram using the DAC 3560C in LDO-Mode.

Lowering the input voltage further will – depending on load – reduce the PSRR until the LDO is out of regulation.

The LDO output can be bypassed using the BYPLDO-Function bit in the MODE Control Register. Selecting this bit closes an internal 100 Ω switch between the LDOs input and output pin. This function is only available in Zero Power and Standby Mode. The LDO is then turned off. Use this function to reduce the quiescent current in Standby Mode.

### 5.2. Non-LDO Mode, Using the DAC 3560C without the LDO

Selecting the SNLDOM-Function Bit in the MODE Control Register disables the LDO and configures the DAC 3560C for a supply voltage range from 2.2 V to 5.5 V. The signal reference level for the audio outputs is formed by a resistive voltage divider to VBAT/2. A second filter capacitor can be connected to pin CF to form a second order noise filter. Connect the LDO output pin (VLDO) directly to the battery line (VBAT) as well as the supply pins of the audio drivers (HPVDD EPVDD, LSVDD) and the charge pump input (CPIN).

When using the LDO, connect an 1-µF ceramic capacitor (X7R, X5R) to the LDO output to ensure a stable operation of the LDO.

The DAC 3560C utilizes an internal charge pump circuit to keep internal circuits operating at low supply voltages. The charge pump must be used, if the supply voltage at VBAT is below 2.7 V. Connect an additional capacitor between pin PVDD and pin VLDO to allow the internal charge pump to work properly.

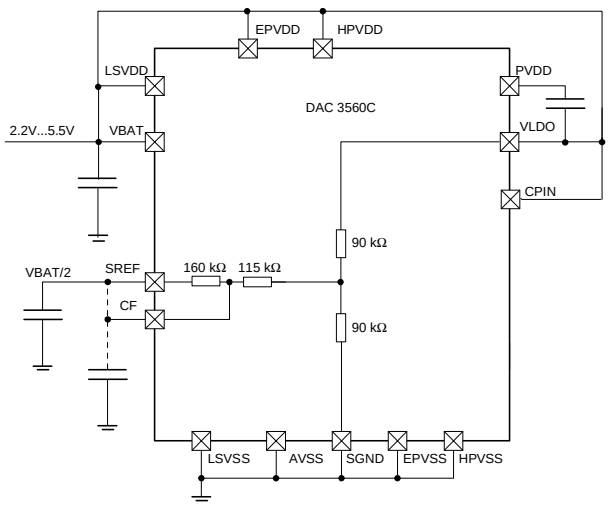



**Fig. 5–2:** Simplified application diagram using the DAC 3560C in Non-LDO-Mode

### 5.3. Headphone Common Driver

The DAC 3560C has driver outputs for earpiece, loudspeaker and headphone connection. While the earpiece and loudspeaker outputs are of the differential type, the headphone driver outputs are single-ended. Single-ended drivers usually require a large coupling capacitor to block the DC bias from the headphone. The DAC 3560C provides a headphone common output (HPCM), which eliminates the need for bulky DC-blocking capacitors.

Selecting the ENHPC-Bit in the BLOCK Control Register enables the headphone common driver output (HPCM). The HPCM-driver is then turned on with the left or right headphone and delivers the audio signal reference level at the output (1.425 V or VLDO/2).

Capacitive coupling is also possible for all driver outputs. Make sure that the ENHPC-Bit in the BLOCK Control Register is set correctly before setting the device in Standby or Operational Mode, otherwise the DAC 3560C might fail to bias DC-Blocking capacitors at the headphone outputs.

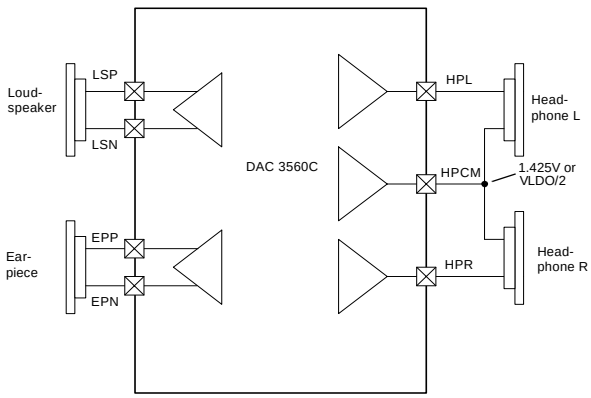



**Fig. 5–3:** Headphone connection, using the headphone common driver output.

### 5.4. Stereo, Mono Mode Operation of the DAC 3560C

Selecting the SMM-Function Bit in the MODE Control Register configures the DAC 3560C for mono or stereo operation.

Selecting mono mode will turn off the right DAC-channel. The $I^2S$ audio data format is still the same as for stereo operation but right channel audio data are dropped internally. The right headphone driver will be routed to the left signal chain. Use the Mono Mode to reduce the current consumption if no stereo signal processing is required.

For both modes, stereo or mono, the DAC 3560C supports side tone mixing from the auxiliary inputs (AUXL, AUXR, AIN). It is also possible to use the DAC 3560C without digital audio from the DAC, if only an analog-in to analog-out function is needed. See Table 5–1 for side tone capabilities of the DAC 3560C. Please also refer to the functional block diagram (see Fig. 1–1 on page 5), to see how audio signals are mixed.

**Table 5–1:** Mixing Possibilities: All Audio Inputs/ Outputs active. Volumes, Gains set to 0 dB

| Output | Stereo Mode | Mono Mode |
|---|---|---|
| Left Headphone Output | Ain + AuxL +DacL | Ain +(AuxL+AuxR)/2 + DacL |
| Right Headphone Output | Ain + AuxR +DacR | Ain +(AuxL+AuxR)/2 + DacL |
| Loudspeaker Output | Ain +(AuxL+AuxR)/2 +(DacL+DacR)/2 | Ain +(AuxL+AuxR)/2 + DacL |
| Earpiece Output | Ain +(AuxL+AuxR)/2 +(DacL+DacR)/2 | Ain +(AuxL+AuxR)/2 + DacL |

**Note:** Please note that the sum of all input signals (DAC, AUX, AUXR, AIN), must not exceed the 0 db (Full Scale Level), otherwise signal degradation will occur due to clipping.

### 5.4.1. Digital Supply

The DAC 3560C has two supply pins for the digital part of the IC. The IOVDD Pin supplies the digital I/O cells. The usable voltage range is 1.8 V to 5.5 V, allowing direct connection to modern microcontrollers. Pin DVDD supplies the internal digital core of the IC with a voltage range from 2.2 V to 5.5 V. Use the lowest voltage available to reduce the digital supply current. Do not connect IOVDD or DVDD to the LDO-Output when using the LDO, as this will result in a deadlock situation for the DAC 3560C.

### 5.4.2. Power On/Off Sequence

The DAC 3560C has three power states – Zero Power, Standby and Operational Mode, that permit powering on the device without clicks and pops, while giving the lowest current consumption possible. The power states of the DAC 3560C are controlled by function bits PM[1:0] in the Mode Control Register, selectable via the $I^2C$/SPI control interface.

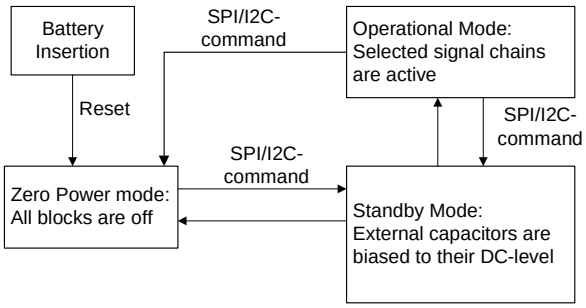



**Fig. 5–4:** Power States

**Zero Power Mode:**

When the battery voltage is initially applied, the DAC 3560C must be reset with a low signal at Pin $\overline{\text{RES}}$, in order to clear all internal registers to their default values, which sets the DAC 3560C into a defined state (Zero Power Mode).

In Zero Power Mode, all blocks are forced off and the current consumption of the device is zero.

After releasing the $\overline{\text{RES}}$ pin, it is possible to program all registers of the DAC 3560C. However, all register contents are suppressed except the BYPLDO-function bit from the Mode Control Register, which allows bypassing the LDO output with an internal 100 Ω switch to VBAT. The following bits:

– SNLDOM: (For using the device with or without the LDO)

– ENHPC: (For using or not using the headphone common driver)

should be set before entering the next power state (Standby Mode).

**Standby Mode:**

In Standby Mode, external capacitors are biased to their DC level (signal reference level). Only circuitries to bias the external capacitors are enabled, resulting in a low-current consumption.

Allow the signal reference level (Pin SREF, CF) to settle before changing to Operational Mode.

If the LDO is enabled (bit SNLDOM=0) it delivers a stable 2.85 V at the output (VLDO). Bypassing the LDO with an internal 100 Ω switch to VBAT is also possible. The LDO is then disabled. Use this function to reduce the quiescent current in Standby Mode.

All registers are programmable during Standby Mode, but the content of the Block Control register is suppressed. It is recommended to keep all output volumes in their mute position before changing to Operational Mode in order to avoid audible clicks and pops.

**Operational Mode:**

In Operational Mode, the content of the Block Control register will become transparent, so that all selected blocks and their signal chains are active.

Programming all registers is possible allowing changing signal paths on the fly. However, it is recommended to ramp down the output volumes before, in order to avoid audible clicks and pops.

**Power-Down Sequence:**

Powering down the DAC 3560C from Operational Mode or Standby Mode can be achieved by selecting Zero Power Mode from the Mode Register. All register values remain unchanged. It is possible to clear all register values to their default values by a write access to the RESET Register.

## 6. Application Circuit

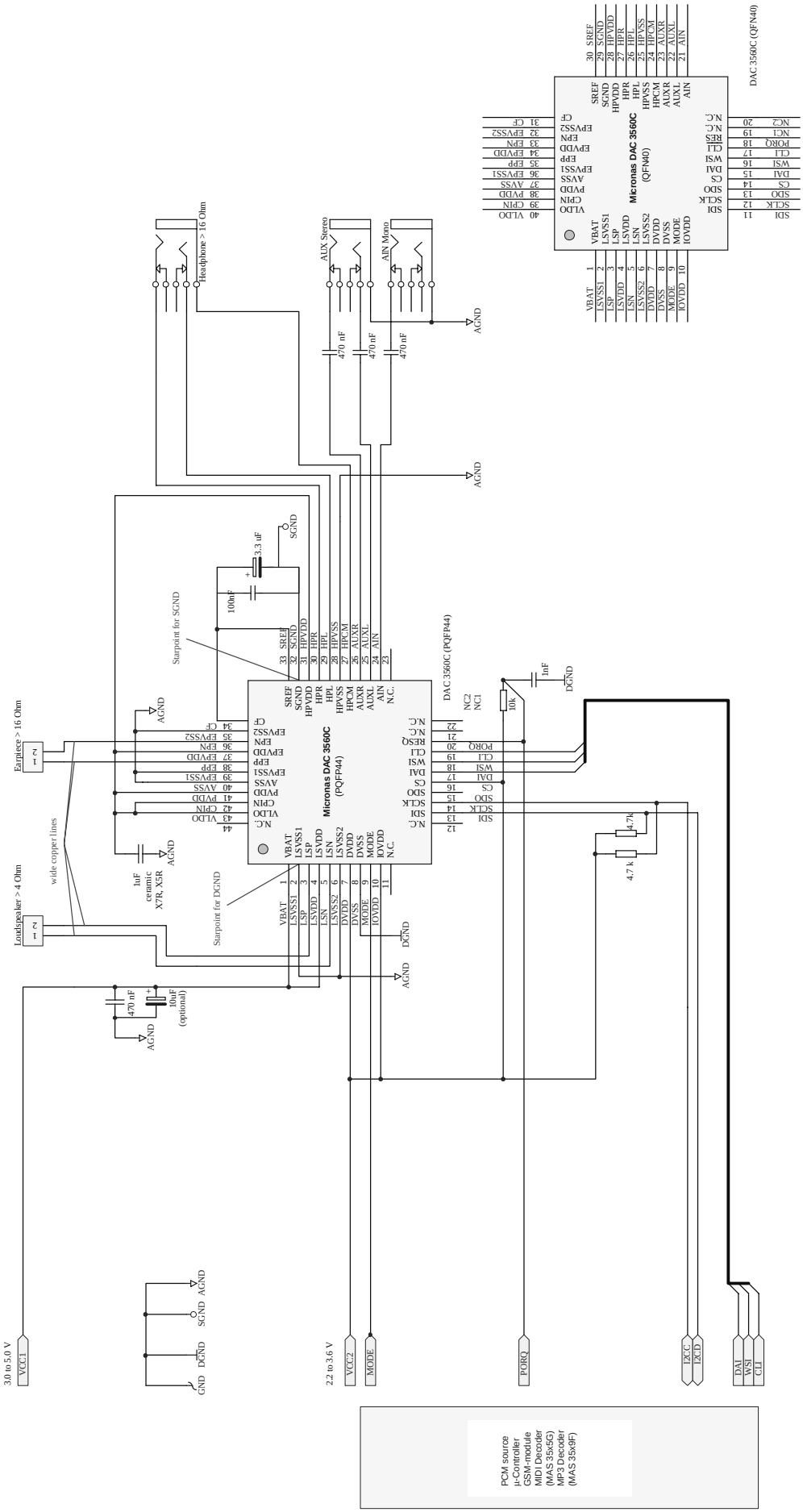



**Fig. 6–1:** Application circuit in LDO Mode, I²C-Control

## 7. Data Sheet History

1. Advance Information: “DAC 3560C Audio-Subsystem for Portable Applications”, Feb. 5, 2003, 6251-588-1AI. First release of the advance information.

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Internet: www.micronas.com

Printed in Germany
Order No. 6251-588-1AI