14-Bit 400-MSPS Digital-to-Analog Converter

FEATURES

- **400-MSPS Update Rate**
- **Controlled Baseline**
  - **– One Assembly**
  - **– One Test Site**
  - **– One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **LVDS-Compatible Input Interface**
- **Spurious-Free Dynamic Range (SFDR) to Nyquist**
  - **– 69 dBc at 70 MHz IF, 400 MSPS**
- **W-CDMA Adjacent Channel Power Ratio (ACPR)**
  - **– 73 dBc at 30.72-MHz IF, 122.88 MSPS**
  - **– 71 dBc at 61.44-MHz IF, 245.76 MSPS**
- **Differential Scalable Current Outputs: 2 mA to 20 mA**
- **On-Chip 1.2-V Reference**
- **Single 3.3-V Supply Operation**
- **Power Dissipation: 660 mW at f_{CLK} = 400 MSPS, f_{OUT} = 20 MHz**
- **Package: 48-Pin PowerPAD™ Thermally-Enhanced Thin Quad Flat Pack (HTQFP) T_{JA} = 29.1°C/W**

APPLICATIONS

- **Cellular Base Transceiver Station Transmit Channel:**
  - **– CDMA: WCDMA, CDMA2000, IS-95**
  - **– TDMA: GSM, IS-136, EDGE/GPRS**
  - **– Supports Single-Carrier and Multicarrier Applications**
- **Test and Measurement: Arbitrary Waveform Generation**
- **Military Communications**

DESCRIPTION/ORDERING INFORMATION

The DAC5675 is a 14-bit resolution high-speed digital-to-analog converter (DAC). The DAC5675 is designed for high-speed digital data transmission in wired and wireless communication systems, high-frequency direct-digital synthesis (DDS), and waveform reconstruction in test and measurement applications. The DAC5675 has excellent spurious-free dynamic range (SFDR) at high intermediate frequencies, which makes it well-suited for multicarrier transmission in TDMA- and CDMA-based cellular base transceiver stations (BTSs).

The DAC5675 operates from a single-supply voltage of 3.3 V. Power dissipation is 660 mW at f_{CLK} = 400 MSPS, f_{OUT} = 70 MHz. The DAC5675 provides a nominal full-scale differential current output of 20 mA, supporting both single-ended and differential applications. The output current can be directly fed to the load with no additional external output buffer required. The output is referred to the analog supply voltage AV_{DD}.

The DAC5675 comprises a low-voltage differential signaling (LVDS) interface for high-speed digital data input. LVDS features a low differential voltage swing with a low constant power consumption across frequency, allowing for high-speed data transmission with low noise levels; that is, with low electromagnetic interference (EMI). LVDS is typically implemented in low-voltage digital CMOS processes, making it the ideal technology for high-speed interfacing between the DAC5675 and high-speed low-voltage CMOS ASICs or FPGAs. The DAC5675 current-source-array architecture supports update rates of up to 400 MSPS. On-chip edge-triggered input latches provide for minimum setup and hold times, thereby relaxing interface timing.

The DAC5675 has been specifically designed for a differential transformer-coupled output with a 50-Ω doubly-terminated load. With the 20-mA full-scale output current, both a 4:1 impedance ratio (resulting in an output power of 4 dBm) and 1:1 impedance ratio transformer (–2 dBm) is supported. The last configuration is preferred for optimum performance at high output frequencies and update rates. The outputs are terminated to AVDD and have voltage compliance ranges from AV_{DD} – 1 to AV_{DD} + 0.3 V.

An accurate on-chip 1.2-V temperature-compensated bandgap reference and control amplifier allows the user to adjust this output current from 20 mA down to 2 mA. This provides 20-dB gain range control capabilities. Alternatively, an external reference voltage may be applied. The DAC5675 features a SLEEP mode, which reduces the standby power to approximately 18 mW.

The DAC5675 is available in a 48-pin PowerPAD™ thermally-enhanced thin quad flat pack (HTQFP). This package increases thermal efficiency in a standard size IC package. The device is specified for operation over the military temperature range of –55°C to 125°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC5675-EP	48 HTQFP	PHP	DAC5675-EP	DAC5675MPHPREP	Tape and reel, 1000
				DAC5675MPHPEP	Tray, 250

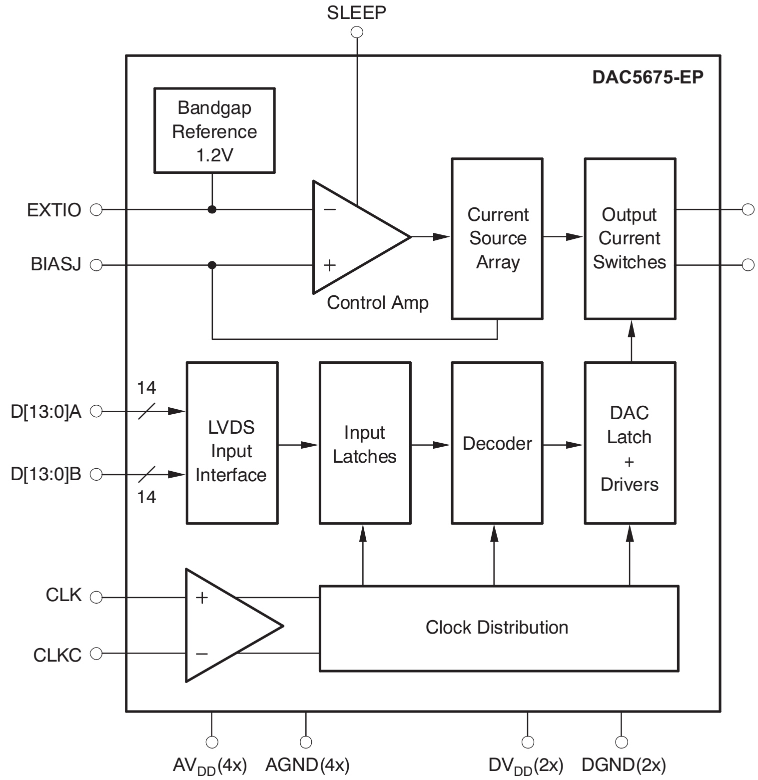
(1) For the most current package and ordering information, see the *Package Option Addendum* located at the end of this data sheet.

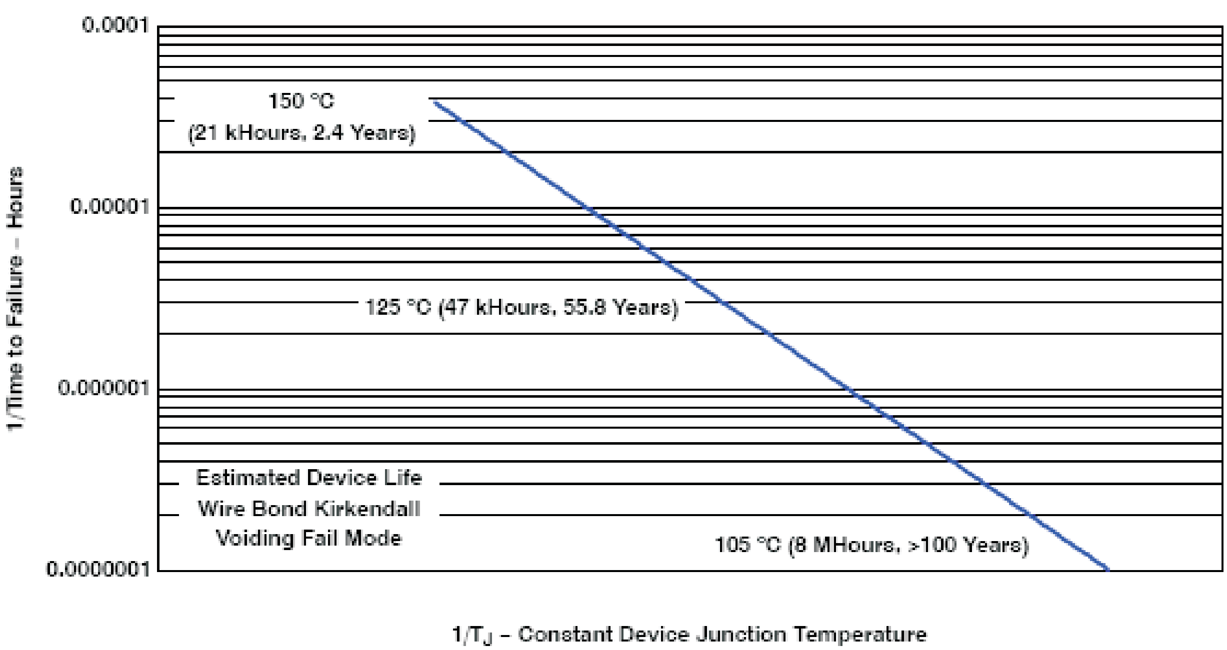
TQFP-48 PACKAGE THERMAL CHARACTERISTICS

PARAMETER		SAME PACKAGE FORM WITHOUT PowerPAD	PowerPAD CONNECTED TO PCB THERMAL PLANE(1)
$R_{\theta JA}$	Thermal resistance, junction to ambient(1)(2)	108.71°C/W	29.11°C/W
$R_{\theta JC}$	Thermal resistance, junction to case(1)(2)	18.18°C/W	1.14°C/W

(1) Airflow is at 0 LFM (no airflow).
(2) Specified with the PowerPAD bond pad on the backside of the package soldered to a 2-oz CU plate PCB thermal plane

FUNCTIONAL BLOCK DIAGRAM





Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		DAC5675-EP	UNIT
Supply voltage range	AV_{DD}[2]	–0.3 to 3.6	V
	DV_{DD}[3]	–0.3 to 3.6	
	AV_{DD} to DV_{DD}	–3.6 to 3.6	
Voltage between AGND and DGND		–0.3 to 0.5	V
CLK, CLKC[2]		–0.3 to AV_{DD} + 0.3	V
Digital input D[13:0]A, D[13:0]B[3], SLEEP, DLLOFF		–0.3 to DV_{DD} + 0.3	V
IOUT1, IOUT2[2]		–1 to AV_{DD} + 0.3	V
EXTIO, BIASJ[2]		–1 to AV_{DD} + 0.3	V
Peak input current (any input)		20	mA
Peak total input current (all inputs)		–30	mA
Operating free-air temperature range, T_A		–55 to 125	°C
Storage temperature range		–65 to 150	°C
Lead temperature 1,6 mm (1/16 in) from the case for 10 s		260	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND
(3) Measured with respect to DGND

DC Electrical Characteristics

over operating free-air temperature range, typical values at 25°C, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			14			Bit
DC Accuracy(1)						
INL	Integral nonlinearity	T_{MIN} to T_{MAX}	–4	±1.5	4.6	LSB
DNL	Differential nonlinearity		–2	±0.6	2.2	LSB
Monotonicity				Monotonic 12b Level		
Analog Output						
$I_{O(FS)}$	Full-scale output current		2		20	mA
	Output compliance range	AV_{DD} = 3.15 V to 3.45 V, $I_{O(FS)}$ = 20 mA	AV_{DD} – 1		AV_{DD} + 0.3	V
	Offset error			0.01		%FSR
	Gain error	Without internal reference	–10	5	10	%FSR
		With internal reference	–10	2.5	10	
	Output resistance			300		kΩ
	Output capacitance			5		pF
Reference Output						
$V_{(EXTIO)}$	Reference voltage		1.17	1.23	1.29	V
	Reference output current(2)			100		nA
Reference Input						
$V_{(EXTIO)}$	Input reference voltage		0.6	1.2	1.25	V
	Input resistance			1		MΩ
	Small-signal bandwidth			1.4		MHz
	Input capacitance			100		pF
Temperature Coefficients						
	Offset drift			12		ppm of FSR/°C
$\Delta V_{(EXTIO)}$	Reference voltage drift			±50		ppm/°C
Power Supply						
AV_{DD}	Analog supply voltage		3.15	3.3	3.6	V
DV_{DD}	Digital supply voltage		3.15	3.3	3.6	V
$I_{(AVDD)}$	Analog supply current(3)			115		mA
$I_{(DVDD)}$	Digital supply current(3)			85		mA
P_D	Power dissipation	Sleep mode		18		mW
		AV_{DD} = 3.3 V, DV_{DD} = 3.3 V		660	900	
APSRR	Analog and digital power-supply rejection ratio	AV_{DD} = 3.15 V to 3.45 V	–0.9	±0.1	0.9	%FSR/V
DPSRR			–0.9	±0.1	0.9	

(1) Measured differential at I_{OUT1} and I_{OUT2}: 25 Ω to AV_{DD}
(2) Use an external buffer amplifier with high impedance input to drive any external load.
(3) Measured at f_{CLK} = 400 MSPS and f_{OUT} = 70 MHz

AC Electrical Characteristics

over operating free-air temperature range, typical values at 25°C, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA, differential transformer-coupled output, 50-Ω doubly-terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analog Output							
f_{CLK}	Output update rate					400	MSPS
$t_{s(DAC)}$	Output setting time to 0.1%	Transition: code x2000 to x23$_{FF}$			12		ns
t_{PD}	Output propagation delay				1		ns
$t_{r(IOUT)}$	Output rise time, 10% to 90%				2		ns
$t_{f(IOUT)}$	Output fall time, 90% to 10%				2		ns
	Output noise	$IOUT_{FS}$ = 20 mA			55		pA/√Hz
		$IOUT_{FS}$ = 2 mA			30		
AC Linearity							
THD	Total harmonic distortion	f_{CLK} = 100 MSPS,	f_{OUT} = 19.9 MHz		73		dBc
		f_{CLK} = 160 MSPS,	f_{OUT} = 41 MHz		72		
		f_{CLK} = 200 MSPS,	f_{OUT} = 70 MHz		68		
		f_{CLK} = 400 MSPS	f_{OUT} = 20.1 MHz		72		
			f_{OUT} = 70 MHz		71		
			f_{OUT} = 140 MHz		58		
SFDR	Spurious-free dynamic range to Nyquist	f_{CLK} = 100 MSPS,	f_{OUT} = 19.9 MHz		73		dBc
		f_{CLK} = 160 MSPS,	f_{OUT} = 41 MHz		73		
		f_{CLK} = 200 MSPS,	f_{OUT} = 70 MHz		70		
		f_{CLK} = 400 MSPS	f_{OUT} = 20.1 MHz		73		
			f_{OUT} = 70 MHz		74		
			f_{OUT} = 140 MHz		60		
SFDR	Spurious-free dynamic range within a window, 5-MHz span	f_{CLK} = 100 MSPS,	f_{OUT} = 19.9 MHz		88		dBc
		f_{CLK} = 160 MSPS,	f_{OUT} = 41 MHz		87		
		f_{CLK} = 200 MSPS,	f_{OUT} = 70 MHz		82		
		f_{CLK} = 400 MSPS	f_{OUT} = 20.1 MHz		87		
			f_{OUT} = 70 MHz		82		
			f_{OUT} = 140 MHz		75		
ACPR	Adjacent channel power ratio WCDMA with 3.84 MHz BW, 5-MHz channel spacing	f_{CLK} = 122.88 MSPS, IF = 30.72 MHz, See Figure 9			73		dB
		f_{CLK} = 245.76 MSPS, IF = 61.44 MHz, See Figure 10			71		
		f_{CLK} = 399.32 MSPS, IF = 153.36 MHz, See Figure 12			65		
IMD	Two-tone intermodulation to Nyquist (each tone at –6 dBfs)	f_{CLK} = 400 MSPS, f_{OUT1} = 70 MHz, f_{OUT2} = 71 MHz			73		dBc
		f_{CLK} = 400 MSPS, f_{OUT1} = 140 MHz, f_{OUT2} = 141 MHz			62		
	Four-tone intermodulation, 15-MHz span, missing center tone (each tone at –16 dBfs)	f_{CLK} = 156 MSPS, f_{OUT} = 15.6, 15.8, 16.2, 16.4 MHz			82		
		f_{CLK} = 400 MSPS, f_{OUT} = 68.1, 69.3, 71.2, 72 MHz			74		

Digital Specifications

over operating free-air temperature range, typical values at 25°C, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS Interface: Nodes D[13:0]A, D[13:0]B						
V_{ITH+}	Positive-going differential input voltage threshold	See LVDS Min/Max Threshold Voltages table		100		mV
V_{ITH-}	Negative-going differential input voltage threshold			–100		mV
Z_T	Internal termination impedance		90	110	132	Ω
C_I	Input capacitance			2		pF
CMOS Interface (SLEEP)						
V_{IH}	High-level input voltage		2	3.3		V
V_{IL}	Low-level input voltage			0	0.8	V
I_{IH}	High-level input current		–100		100	μA
I_{IL}	Low-level input current		–10		10	μA
	Input capacitance			2		pF
Clock Interface (CLK, CLKC)						
|CLK-CLKC|	Clock differential input voltage		0.4		0.8	V_{PP}
$t_{w(H)}$	Clock pulse width high			1.25		ns
$t_{w(L)}$	Clock pulse width low			1.25		ns
	Clock duty cycle		40%		60%	
V_{CM}	Common-mode voltage range			2 ± 20%		V
	Input resistance	Node CLK, CLKC		670		Ω
	Input capacitance	Node CLK, CLKC		2		pF
	Input resistance	Differential		1.3		kΩ
	Input capacitance	Differential		1		pF
Timing						
t_{SU}	Input setup time			1.5		ns
t_H	Input hold time			0.25		ns
t_{LPH}	Input latch pulse high time			2		ns
t_{DD}	Digital delay time	DLL disabled, DLLOFF = 1		3		clk

Timing Information

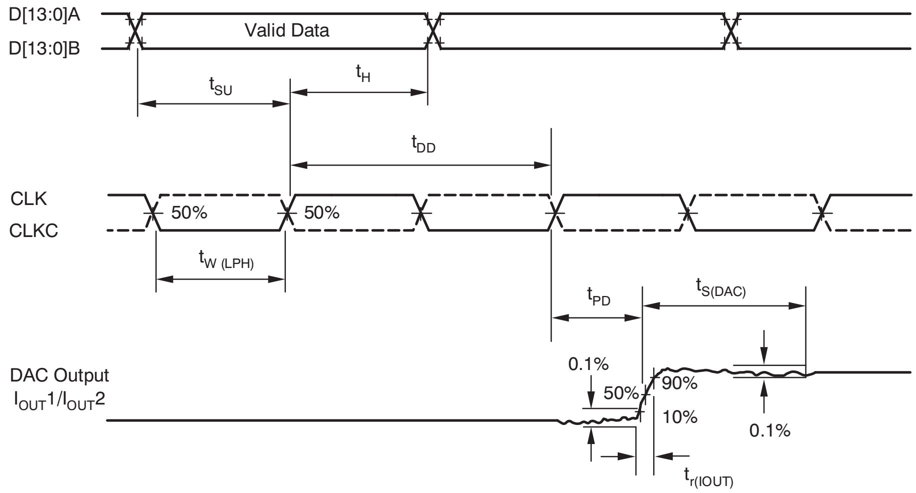


Figure 1. Timing Diagram

Electrical Characteristics[(1)]

over operating free-air temperature range, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA (unless otherwise noted)

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	LOGICAL BIT BINARY EQUIVALENT	COMMENT
V_A (V)	V_B (V)	$V_{A,B}$ (mV)	V_{COM} (V)		
1.25	1.15	100	1.2	1	Operation with minimum differential voltage (±100 mV) applied to the complementary inputs versus common-mode range
1.15	1.25	–100	1.2	0	
2.4	2.3	100	2.35	1	
2.3	2.4	–100	2.35	0	
0.1	0	100	0.05	1	
0	0.1	–100	0.05	0	
1.5	0.9	600	1.2	1	Operation with maximum differential voltage (±600 mV) applied to the complementary inputs versus common-mode range
0.9	1.5	–600	1.2	0	
2.4	1.8	600	2.1	1	
1.8	2.4	–600	2.1	0	
0.6	0	600	0.3	1	
0	0.6	–600	0.3	0	

(1) Specifications subject to change.

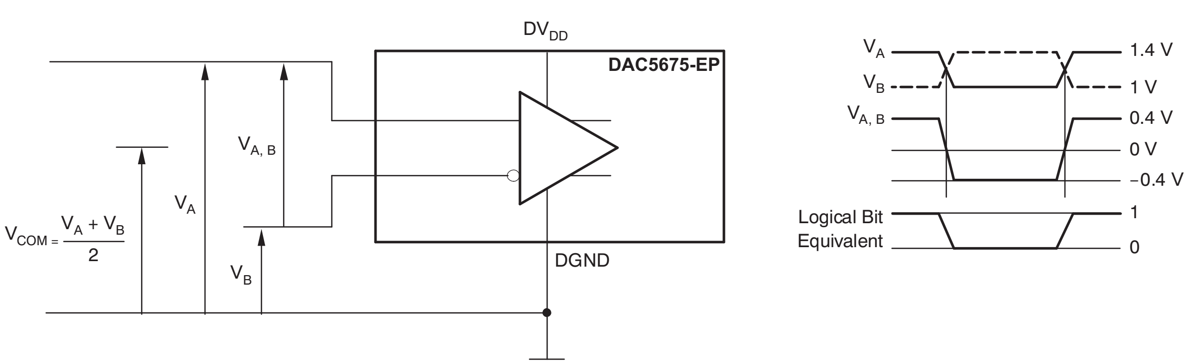
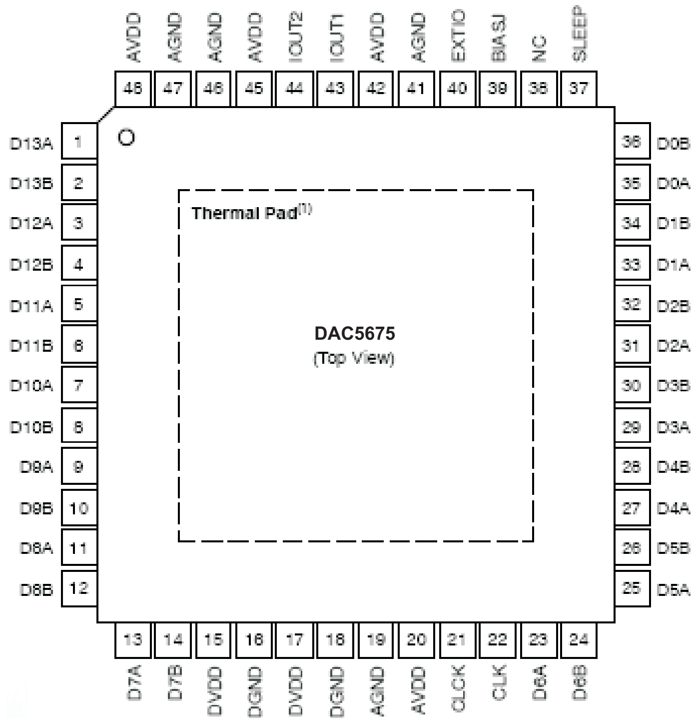


Figure 2. LVDS Timing Test Circuit and Input Test Levels

DEVICE INFORMATION

**PHP PACKAGE
(TOP VIEW)**



A. Thermal pad size: 4,5mm × 4,5mm (min), 5,5mm × 5,5mm (max)

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	19, 41, 46, 47	I	Analog negative supply voltage (ground). Pin 47 is internally connected to the heat slug.
AV_{DD}	20, 42, 45, 48	I	Analog positive supply voltage
BIASJ	39	O	Full-scale output current bias
CLK	22	I	External clock input
CLKC	21	I	Complementary external clock
D[13:0]A	1, 3, 5, 7, 9, 11, 13, 23, 25, 27, 29, 31, 33, 35	I	LVDS positive input, data bits 13–0. D13A is the most significant data bit (MSB). D0A is the least significant data bit (LSB).
D[13:0]B	2, 4, 6, 8, 10, 12, 14, 24, 26, 28, 30, 32, 34, 36	I	LVDS negative input, data bits 13–0.. D13B is the most significant data bit (MSB). D0B is the least significant data bit (LSB).
DGND	16, 18	I	Digital negative supply voltage (ground)
DV_{DD}	15, 17	I	Digital positive supply voltage
EXTIO	40	I/O	Internal reference output or external reference input. Requires a 0.1-µF decoupling capacitor to AGND when used as reference output.
IOUT1	43	O	DAC current output. Full-scale when all input bits are set 1. Connect the reference side of the DAC load resistors to AV_{DD}.
IOUT2	44	O	DAC complementary current output. Full-scale when all input bits are 0. Connect the reference side of the DAC load resistors to AV_{DD}.
NC	38		Not connected in chip. Can be high or low.
SLEEP	37	I	Asynchronous hardware power-down input. Active high. Internal pulldown.

TYPICAL CHARACTERISTICS

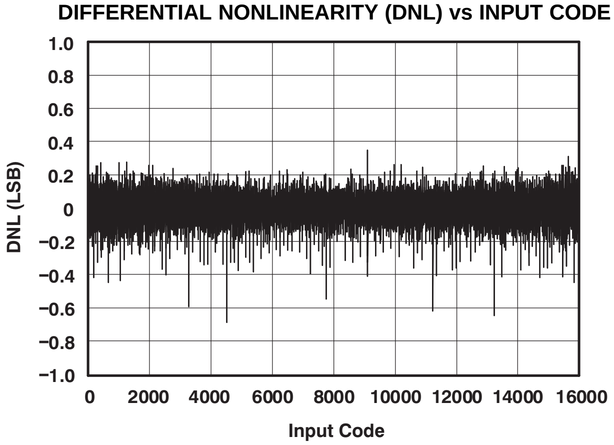


Figure 3.

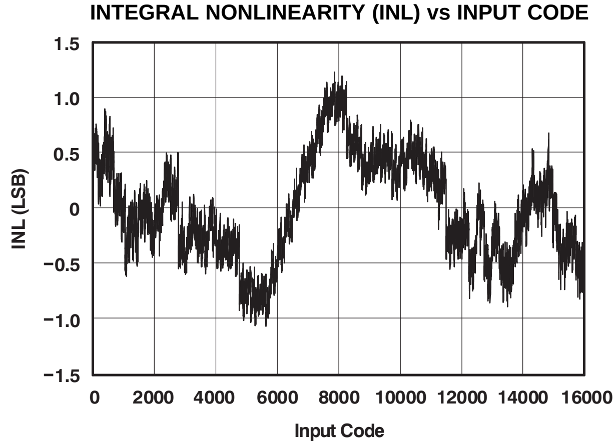


Figure 4.

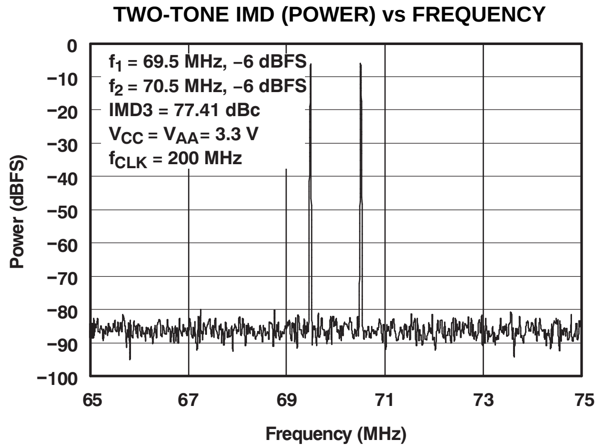


Figure 5.

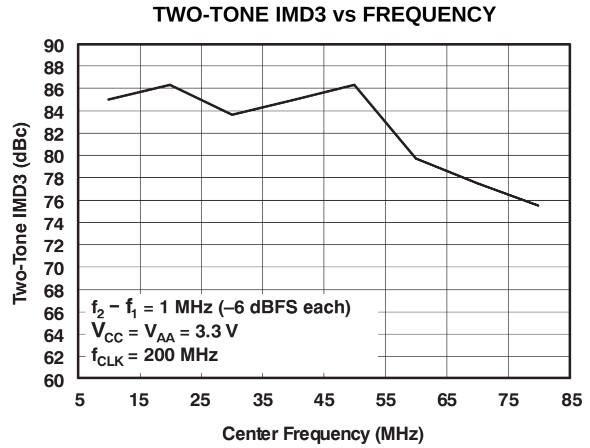


Figure 6.

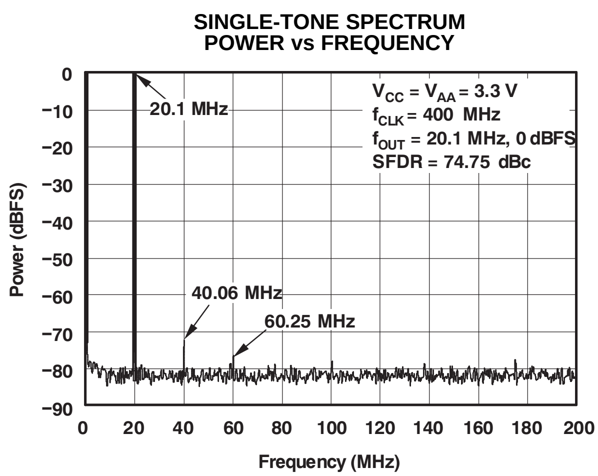


Figure 7.

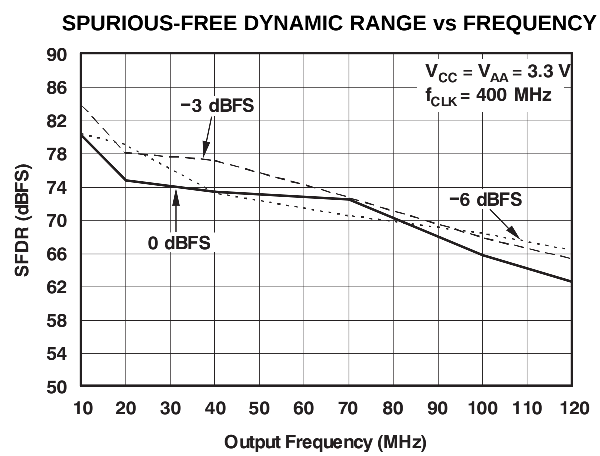


Figure 8.

TYPICAL CHARACTERISTICS (continued)

SPURIOUS-FREE DYNAMIC RANGE vs FREQUENCY

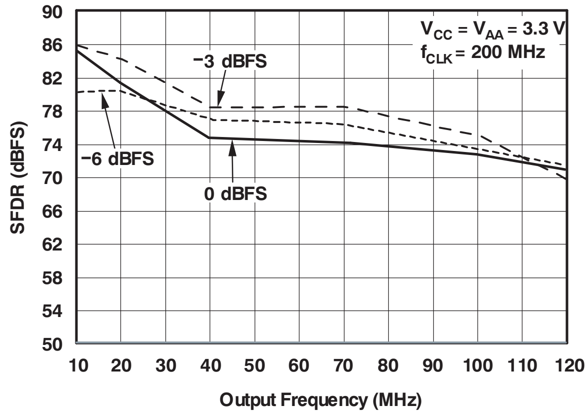


Figure 9.

W-CDMA TM1 SINGLE CARRIER POWER vs FREQUENCY

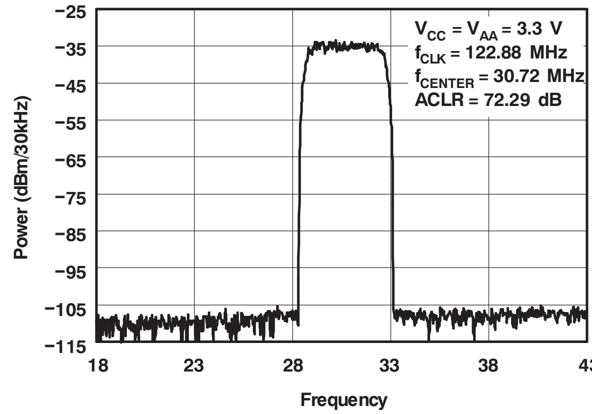


Figure 10.

W-CDMA TM1 DUAL CARRIER POWER vs FREQUENCY

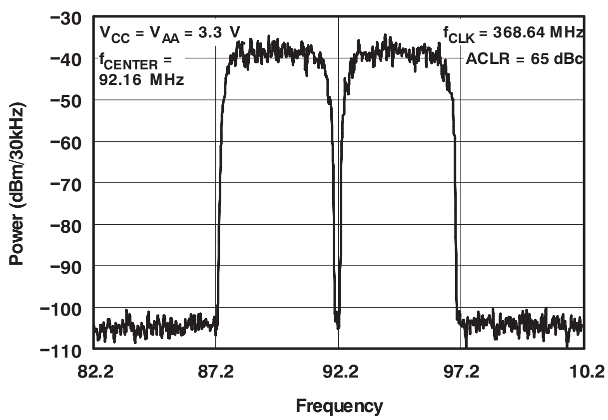


Figure 11.

W-CDMA TM1 SINGLE CARRIER ACLR vs OUTPUT FREQUENCY

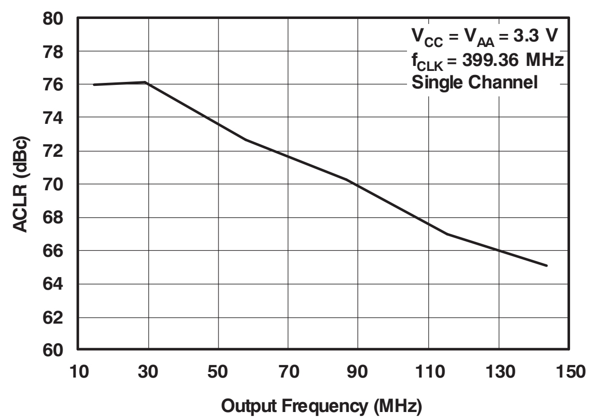


Figure 12.

APPLICATION INFORMATION

Detailed Description

Figure 13 shows a simplified block diagram of the current steering DAC5675. The DAC5675 consists of a segmented array of NPN-transistor current sources, capable of delivering a full-scale output current up to 20 mA. Differential current switches direct the current of each current source to either one of the complementary output nodes IOUT1 or IOUT2. The complementary current output enables differential operation, canceling out common-mode noise sources (digital feedthrough, on-chip, and PCB noise), dc offsets, and even-order distortion components, and doubling signal output power.

The full-scale output current is set using an external resistor (R_{BIAS}) in combination with an on-chip bandgap voltage reference source (1.2 V) and control amplifier. The current (I_{BIAS}) through resistor R_{BIAS} is mirrored internally to provide a full-scale output current equal to 16 times I_{BIAS}. The full-scale current is adjustable from 20 mA down to 2 mA by using the appropriate bias resistor value.

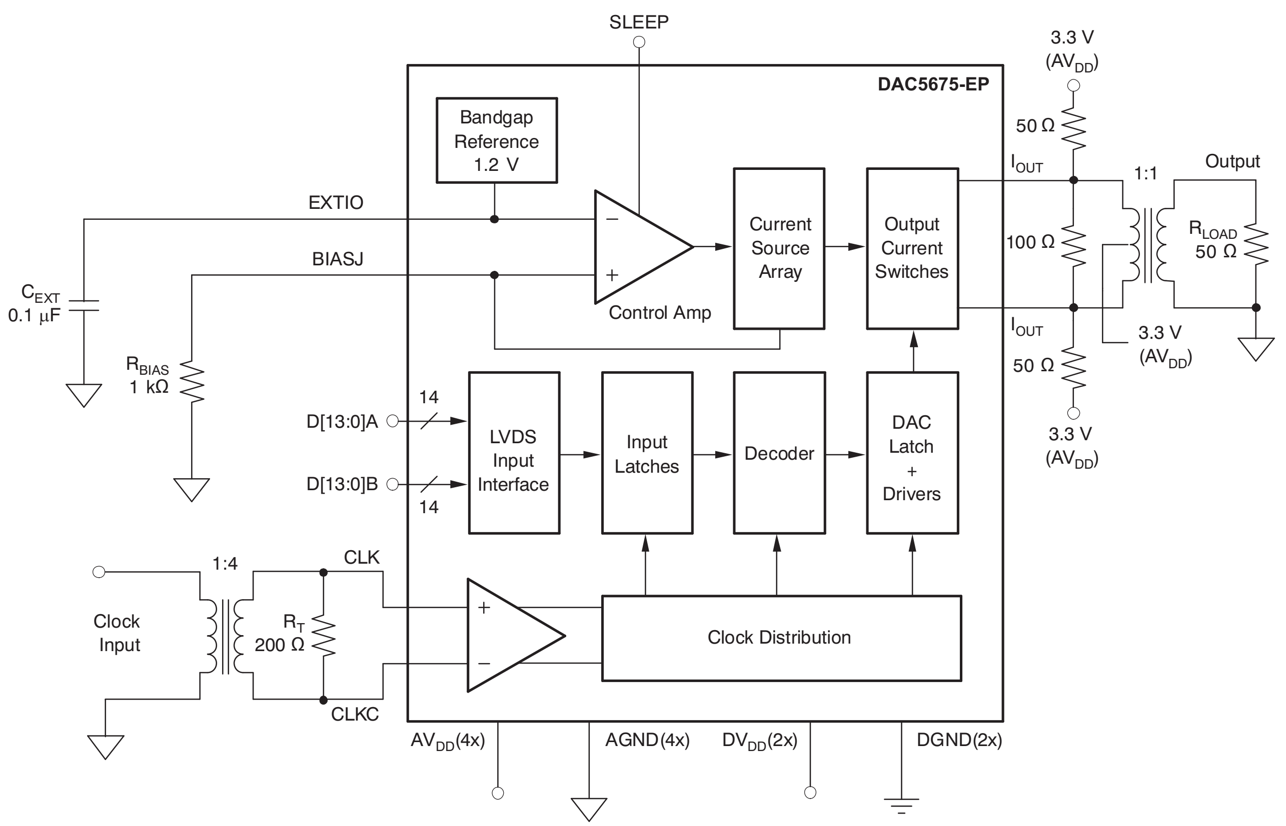


Figure 13. Application Schematic

APPLICATION INFORMATION (continued)

Digital Inputs

The DAC5675 uses a low-voltage differential signaling (LVDS) bus input interface. The LVDS features a low differential voltage swing with low constant power consumption (4 mA per complementary data input) across frequency. The differential characteristic of LVDS allows for high-speed data transmission with low electromagnetic interference (EMI) levels. The LVDS input minimum and maximum input threshold table lists the LVDS input levels. Figure 14 shows the equivalent complementary digital input interface for the DAC5675, valid for pins D[13:0]A and D[13:0]B. Note that the LVDS interface features internal 110-Ω resistors for proper termination. Figure 2 shows the LVDS input timing measurement circuit and waveforms. A common-mode level of 1.2 V and a differential input swing of 0.8 V_{PP} is applied to the inputs.

Figure 15 shows a schematic of the equivalent CMOS/TTL-compatible digital inputs of the DAC5675, valid for the SLEEP pin.

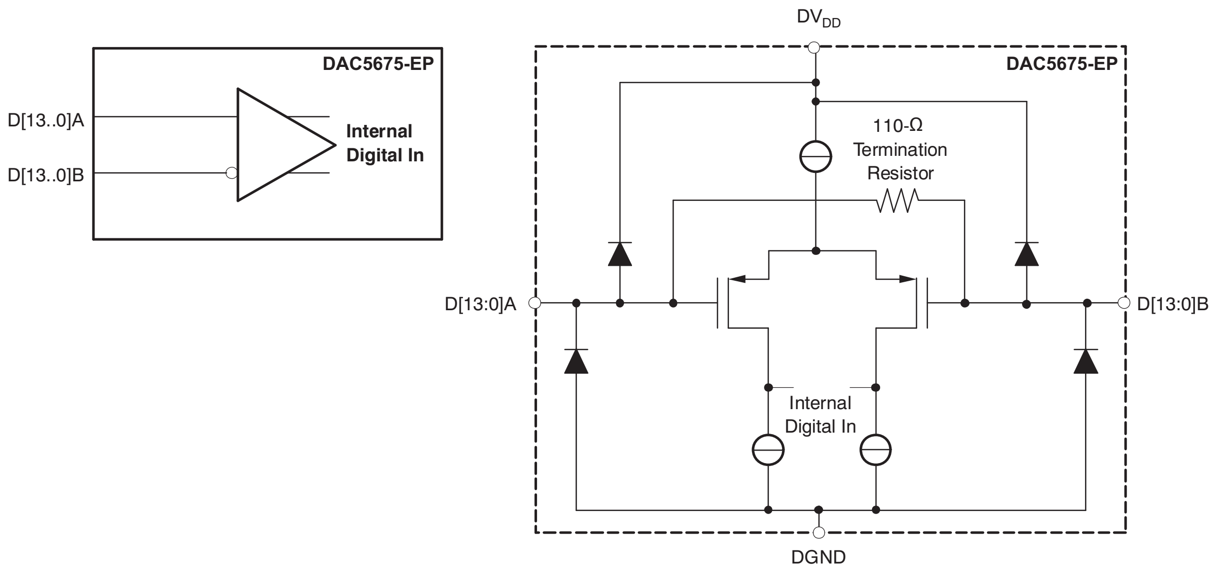


Figure 14. LVDS Digital Equivalent Input

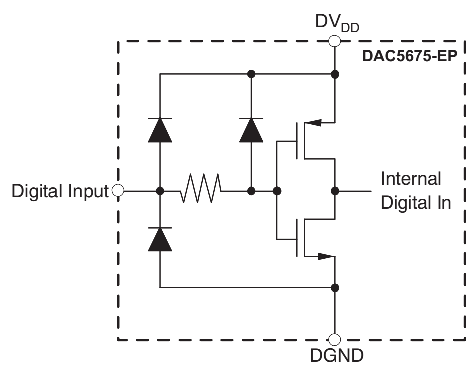


Figure 15. CMOS/TTL Digital Equivalent Input

Clock Input

The DAC5675 features differential LVPECL-compatible clock inputs (CLK, CLKC). Figure 16 shows the equivalent schematic of the clock input buffer. The internal biasing resistors set the input common-mode voltage to approximately 2 V, while the input resistance is typically 670 Ω. A variety of clock sources can be ac-coupled to the device, including a sine-wave source (see Figure 17).

APPLICATION INFORMATION (continued)

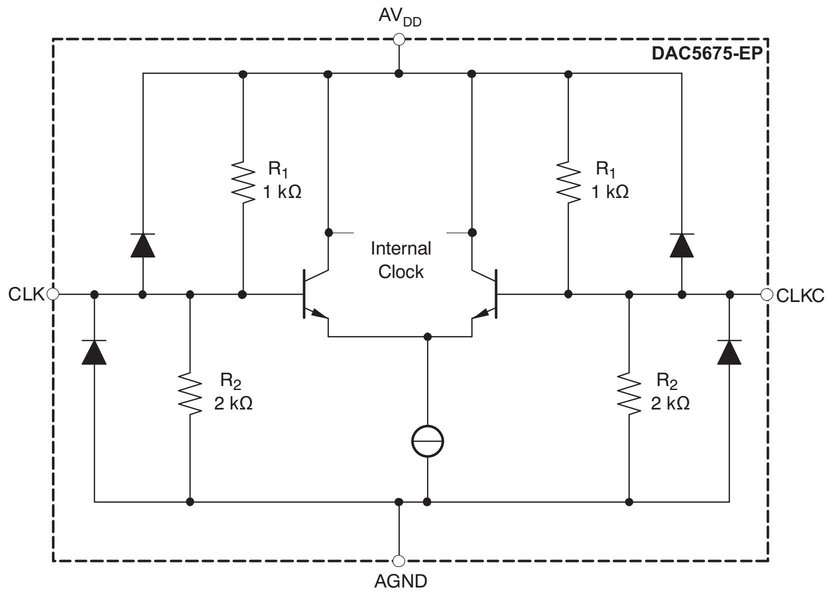


Figure 16. Clock Equivalent Input

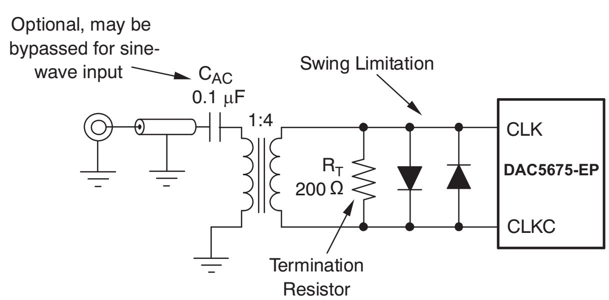


Figure 17. Driving the DAC5675 With a Single-Ended Clock Source Using a Transformer

To obtain best ac performance, the DAC5675 clock input should be driven with a differential LVPECL or sine-wave source as shown in Figure 18 and Figure 19. Here, the potential of V_{TT} should be set to the termination voltage required by the driver along with the proper termination resistors (R_T). The DAC5675 clock input can also be driven single ended; this is shown in Figure 20.

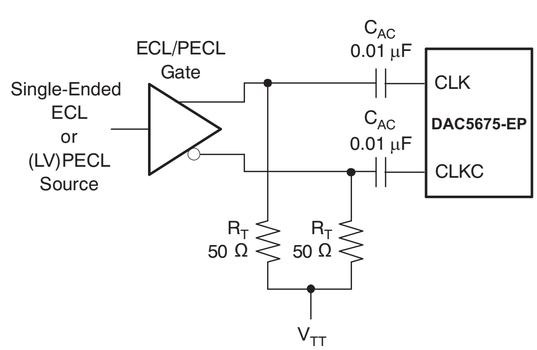


Figure 18. Driving the DAC5675 With a Single-Ended ECL/PECL Clock Source

APPLICATION INFORMATION (continued)

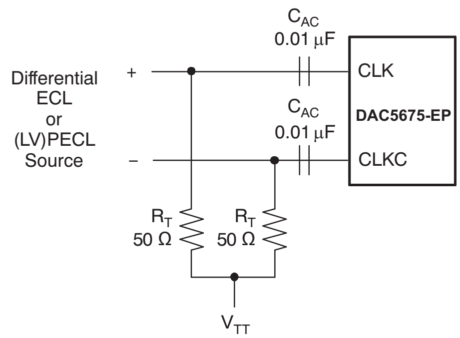


Figure 19. Driving the DAC5675 With a Differential ECL/PECL Clock Source

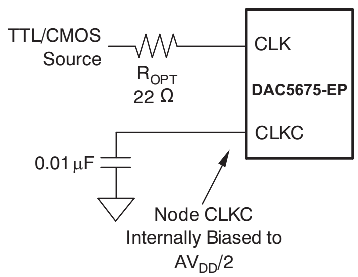


Figure 20. Driving the DAC5675 With a Single-Ended TTL/CMOS Clock Source

Supply Inputs

The DAC5675 comprises separate analog and digital supplies, that is AV_{DD} and DV_{DD}, respectively. These supply inputs can be set independently from 3.6 V down to 3.15 V.

DAC Transfer Function

The DAC5675 delivers complementary output currents IOUT1 and IOUT2. The DAC supports straight binary coding, with D13 being the MSB and D0 the LSB. (For ease of notation, we denote D13–D0 as the logical bit equivalent of the complementary LVDS inputs D[13:0]A and D[13:0]B). Output current IOUT1 equals the approximate full-scale output current when all input bits are set high, when the binary input word has the decimal representation 16383. Full-scale output current flows through terminal IOUT2 when all input bits are set low (mode 0, straight binary input). The relation between IOUT1 and IOUT2 can thus be expressed as:

$$IOUT1 = IO_{(FS)} - IOUT2 \quad (1)$$

where $IO_{(FS)}$ is the full-scale output current. The output currents can be expressed as:

$$IOUT1 = \frac{IO_{(FS)} \times CODE}{16384} \quad (2)$$

$$IOUT2 = \frac{IO_{(FS)} \times (16383 - CODE)}{16384} \quad (3)$$

where CODE is the decimal representation of the DAC data input word. Output currents IOUT1 and IOUT2 drive a load R_L. R_L is the combined impedance for the termination resistance and/or transformer load resistance, R_{LOAD} (see Figure 22 and Figure 23). This would translate into single-ended voltages VOUT1 and VOUT2 at terminal IOUT1 and IOUT2, respectively, of Equation 4 and Equation 5:

APPLICATION INFORMATION (continued)

$$VOUT1 = IOUT1 \times R_L = \frac{\left(CODE \times I_{O(FS)} \times R_L\right)}{16384} \quad (4)$$

$$VOUT2 = IOUT2 \times R_L = \frac{(16383 - CODE) \times I_{O(FS)} \times R_L}{16384} \quad (5)$$

Thus, the differential output voltage $VOUT_{(DIFF)}$ can be expressed as:

$$VOUT_{(DIFF)} = VOUT1 - VOUT2 = \frac{(2CODE - 16383) \times I_{O(FS)} \times R_L}{16384} \quad (6)$$

Equation 6 shows that applying the differential output results in doubling the signal power delivered to the load. Since the output currents IOUT1 and IOUT2 are complementary, they become additive when processed differentially. Care should be taken not to exceed the compliance voltages at nodes IOUT1 and IOUT2, which leads to increased signal distortion.

Reference Operation

The DAC5675 has a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS}. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The full-scale output current equals 16 times this bias current. The full-scale output current $IO_{(FS)}$ is thus expressed as Equation 7:

$$I_{O(FS)} = 16 \times I_{BIAS} = \frac{16 \times V_{EXTIO}}{R_{BIAS}} \quad (7)$$

where V_{EXTIO} is the voltage at terminal EXTIO. The bandgap reference voltage delivers a stable voltage of 1.2 V. This reference can be overridden by applying an external voltage to terminal EXTIO. The bandgap reference can additionally be used for external reference operation. In such a case, an external buffer amplifier with high impedance input should be selected in order to limit the bandgap load current to less than 100 nA. The capacitor C_{EXT} may be omitted. Terminal EXTIO serves as either an input or output node. The full-scale output current is adjustable from 20 mA down to 2 mA by varying resistor R_{BIAS}.

Analog Current Outputs

Figure 21 shows a simplified schematic of the current source array output with corresponding switches. Differential NPN switches direct the current of each individual NPN current source to either the positive output node IOUT1 or its complementary negative output node IOUT2. The output impedance is determined by the stack of the current sources and differential switches and is >300 kΩ in parallel with an output capacitance of 5 pF.

The external output resistors are referred to the positive supply AV_{DD}.

APPLICATION INFORMATION (continued)

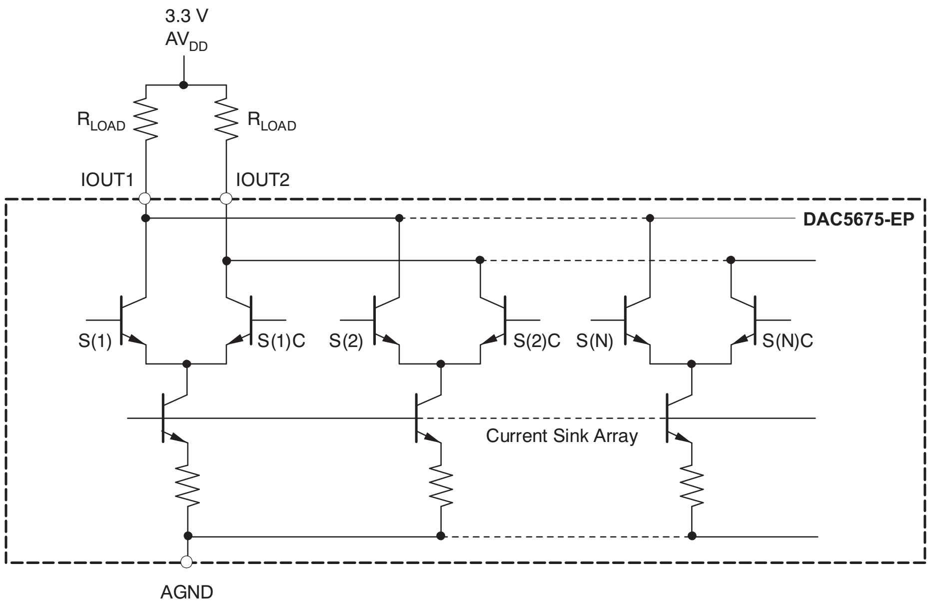


Figure 21. Equivalent Analog Current Output

The DAC5675 can easily be configured to drive a doubly-terminated 50-Ω cable using a properly selected transformer. Figure 22 and Figure 23 show the 1:1 and 4:1 impedance ratio configuration, respectively. These configurations provide maximum rejection of common-mode noise sources and even-order distortion components, thereby doubling the power of the DAC to the output. The center tap on the primary side of the transformer is terminated to AV_{DD}, enabling a dc-current flow for both IOUT1 and IOUT2. Note that the ac performance of the DAC5675 is optimum and specified using a 1:1 differential transformer-coupled output.

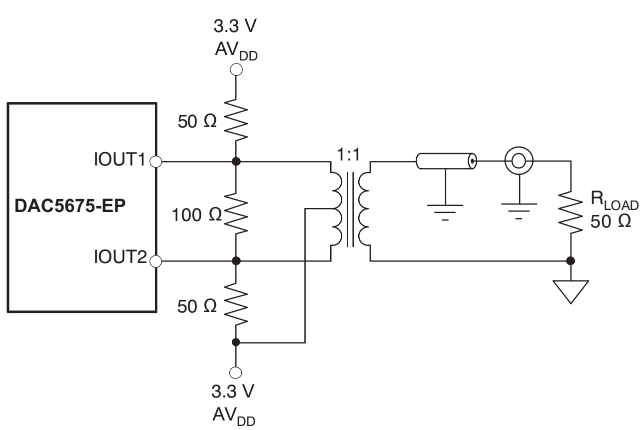


Figure 22. Driving a Doubly-Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

APPLICATION INFORMATION (continued)

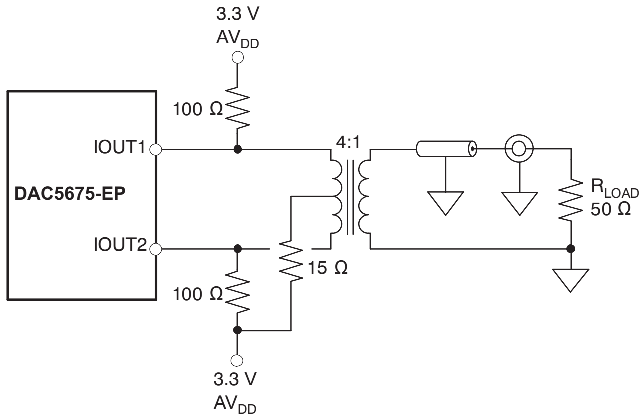


Figure 23. Driving a Doubly-Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

Figure 24(a) shows the typical differential output configuration with two external matched resistor loads. The nominal resistor load of 25 Ω gives a differential output swing of 1 V_{PP} (0.5 V_{PP} single ended) when applying a 20-mA full-scale output current. The output impedance of the DAC5675 slightly depends on the output voltage at nodes IOUT1 and IOUT2. Consequently, for optimum dc-integral nonlinearity, the configuration of Figure 24(b) should be chosen. In this current/voltage (I-V) configuration, terminal IOUT1 is kept at AV_{DD} by the inverting operational amplifier. The complementary output should be connected to AV_{DD} to provide a dc-current path for the current sources switched to IOUT1. The amplifier maximum output swing and the full-scale output current of the DAC determine the value of the feedback resistor R_{FB}. The capacitor C_{FB} filters the steep edges of the DAC5675 current output, thereby reducing the operational amplifier slew-rate requirements. In this configuration, the operational amplifier should operate at a supply voltage higher than the resistor output reference voltage AV_{DD} as a result of its positive and negative output swing around AV_{DD}. Node IOUT1 should be selected if a single-ended unipolar output is desired.

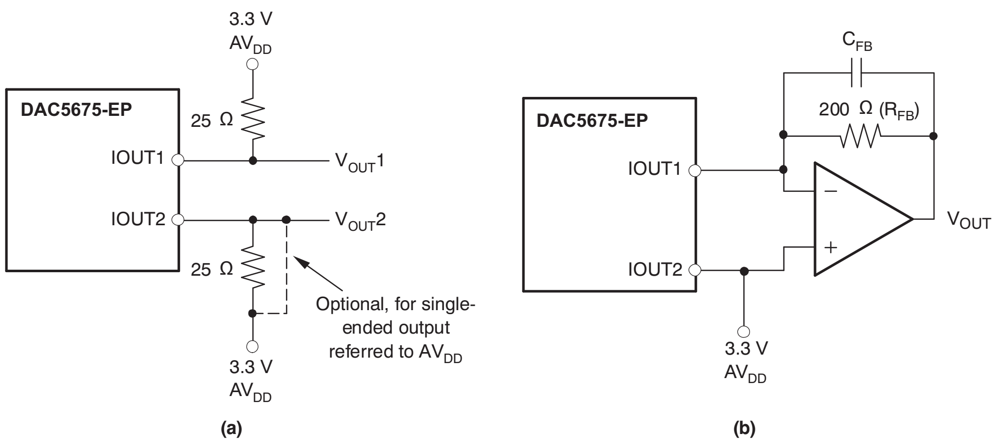


Figure 24. Output Configurations

Sleep Mode

The DAC5675 features a power-down mode that turns off the output current and reduces the supply current to approximately 6 mA. The power-down mode is activated by applying a logic level one to the SLEEP pin, pulled down internally.

DEFINITIONS

Definitions of Specifications and Terminology

Gain error is defined as the percentage error in the ratio between the measured full-scale output current and the value of 16 × $V_{(EXTIO)}/R_{BIAS}$. A $V_{(EXTIO)}$ of 1.25 V is used to measure the gain error with an external reference voltage applied. With an internal reference, this error includes the deviation of $V_{(EXTIO)}$ (internal bandgap reference voltage) from the typical value of 1.25 V.

Offset error is defined as the percentage error in the ratio of the differential output current (IOUT1-IOUT2) and the half of the full-scale output current for input code 8192.

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental output signal.

SNR is the ratio of the rms value of the fundamental output signal to the rms sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

SINAD is the ratio of the rms value of the fundamental output signal to the rms sum of all other spectral components below the Nyquist frequency, including noise and harmonics, but excluding dc.

ACPR or adjacent channel power ratio is defined for a 3.84-Mcps 3GPP W-CDMA input signal measured in a 3.84-MHz bandwidth at a 5-MHz offset from the carrier with a 12-dB peak-to-average ratio.

APSSR or analog power supply ratio is the percentage variation of full-scale output current versus a 5% variation of the analog power supply AV_{DD} from the nominal. This is a dc measurement.

DPSSR or digital power supply ratio is the percentage variation of full-scale output current versus a 5% variation of the digital power supply DV_{DD} from the nominal. This is a dc measurement.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC5675MPHPEP	ACTIVE	HTQFP	PHP	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC5675MPHPREP	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
V62/05619-01XE	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
V62/05619-02XE	ACTIVE	HTQFP	PHP	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF DAC5675-EP :

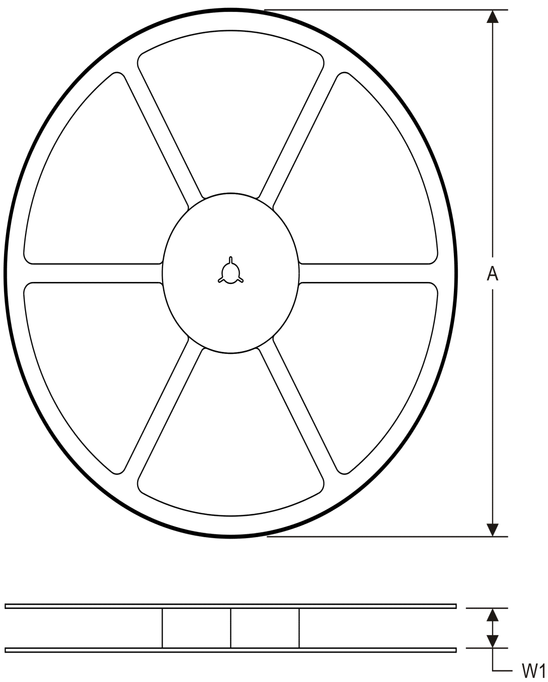
- Catalog: DAC5675

NOTE: Qualified Version Definitions:

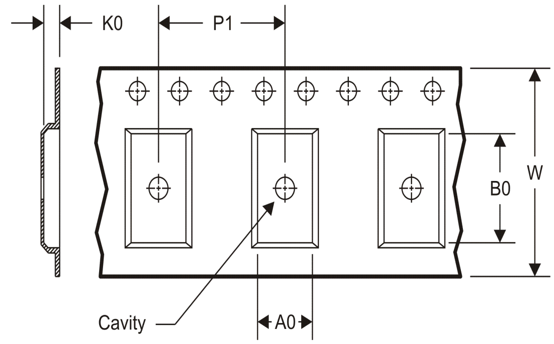
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



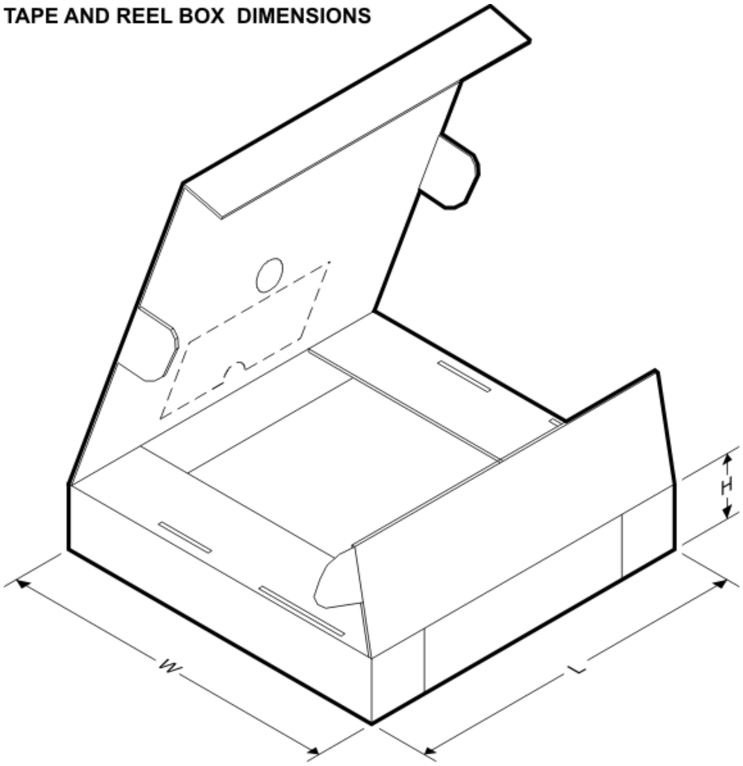
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC5675MPHPREP	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

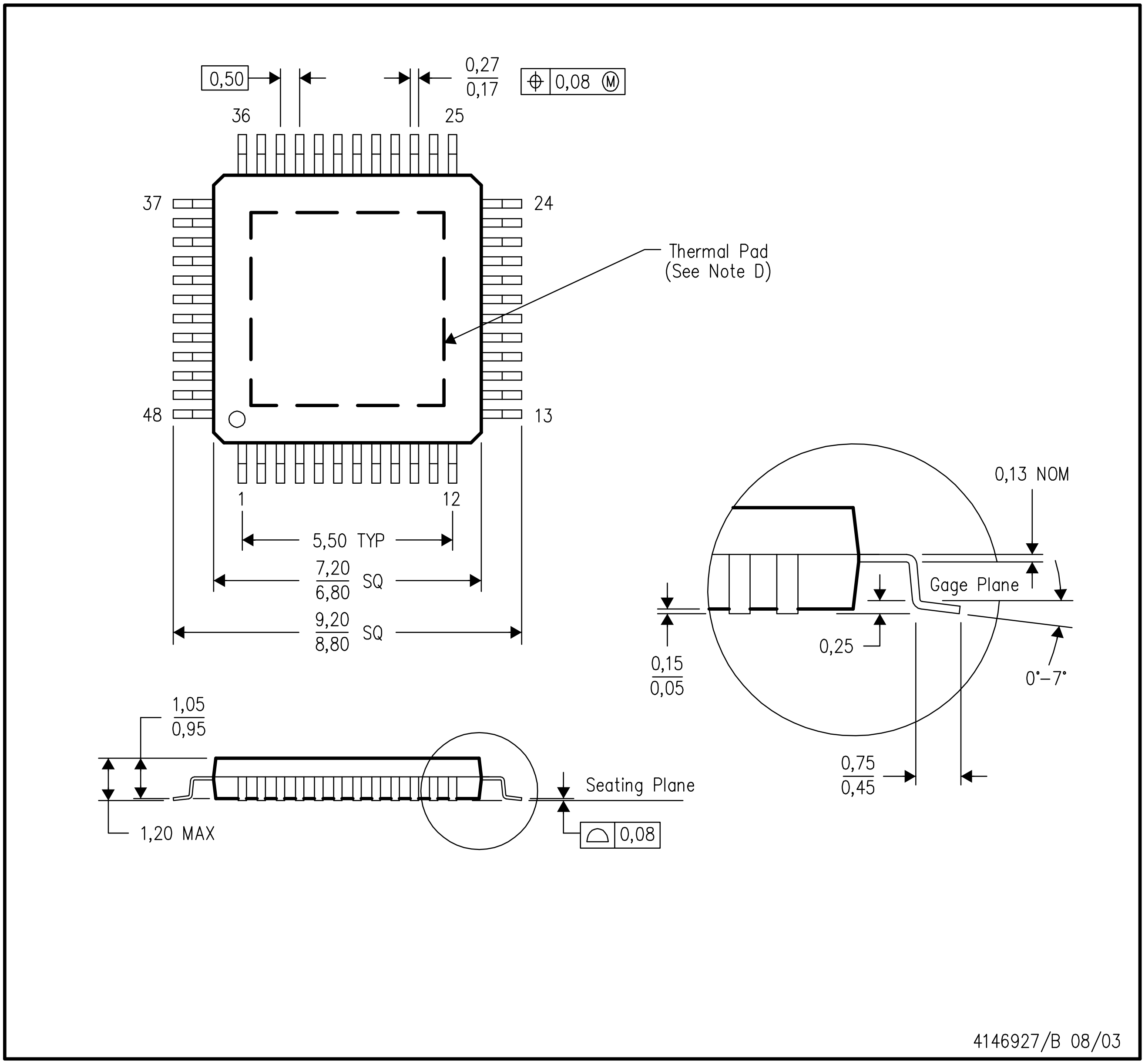
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC5675MPHPREP	HTQFP	PHP	48	1000	367.0	367.0	38.0

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

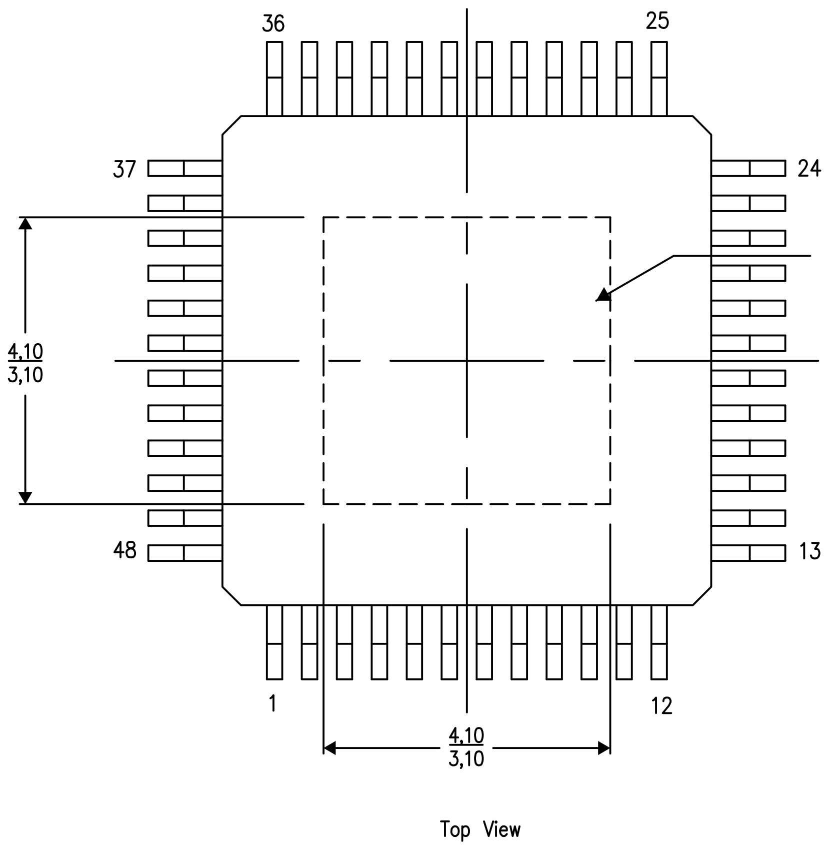
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206329–3/N 04/12

NOTE: A. All linear dimensions are in millimeters

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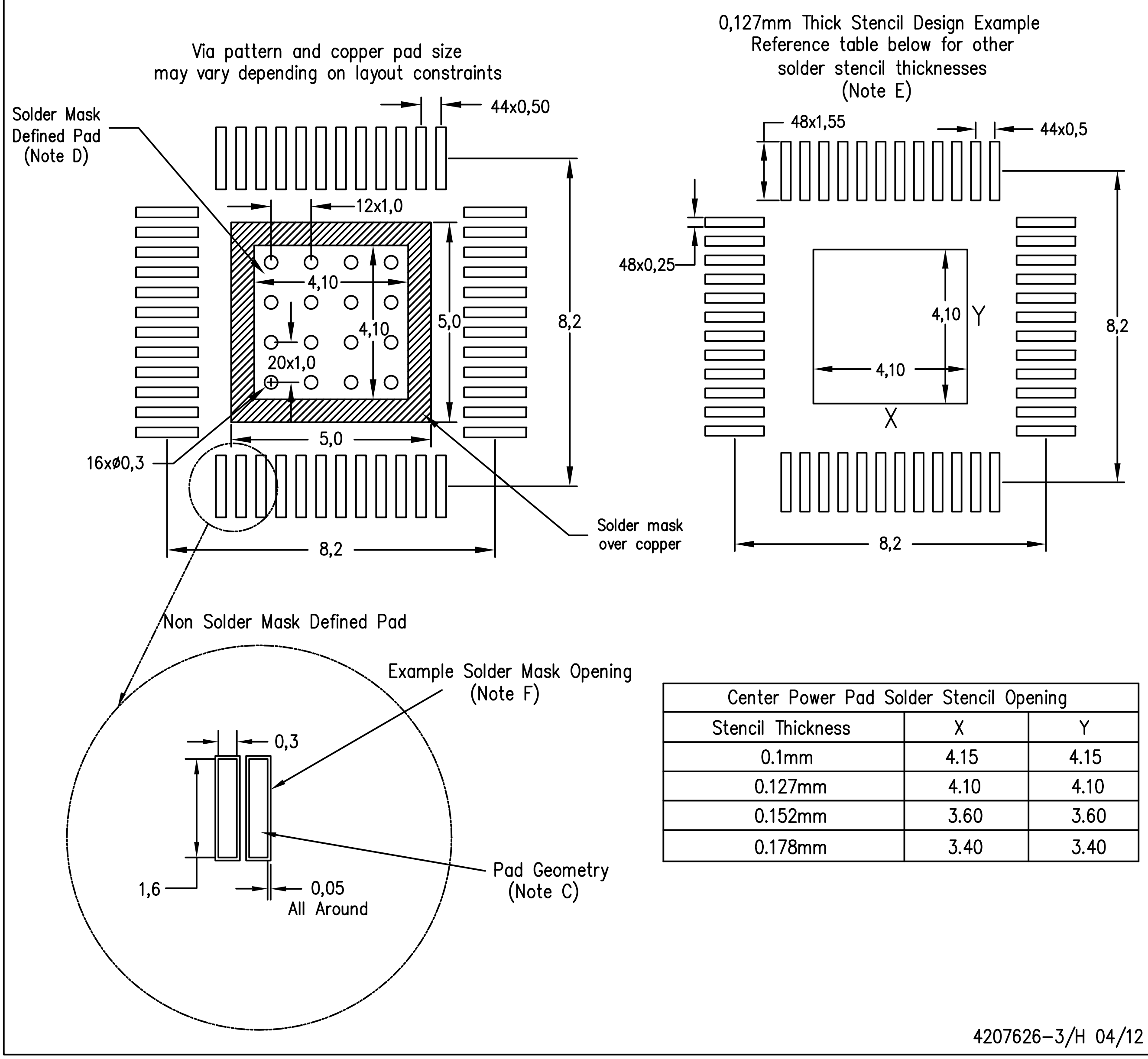
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.15	4.15
0.127mm	4.10	4.10
0.152mm	3.60	3.60
0.178mm	3.40	3.40

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

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