

DBL 2018-C

2 MOTOR DRIVER FOR A VTR

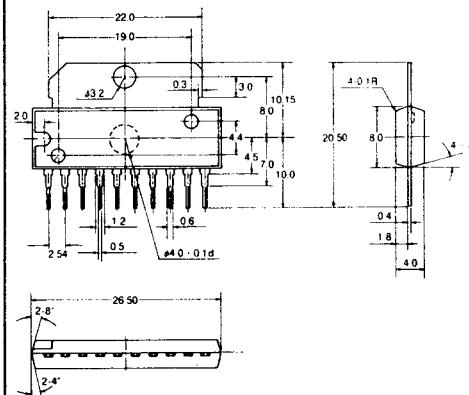
The DBL 2018-C is a monolithic integrated circuit designed to perform bi-directional DC Motor driving.

FEATURES

- Stable braking characteristics by built-in braking function.
 - Stable driving direction change.
 - Built-in element to absorb dash current derived from changing motor direction and braking motor driving.
 - C² MOS logic level compatible input level.

10SIP/HS

Unit: mm

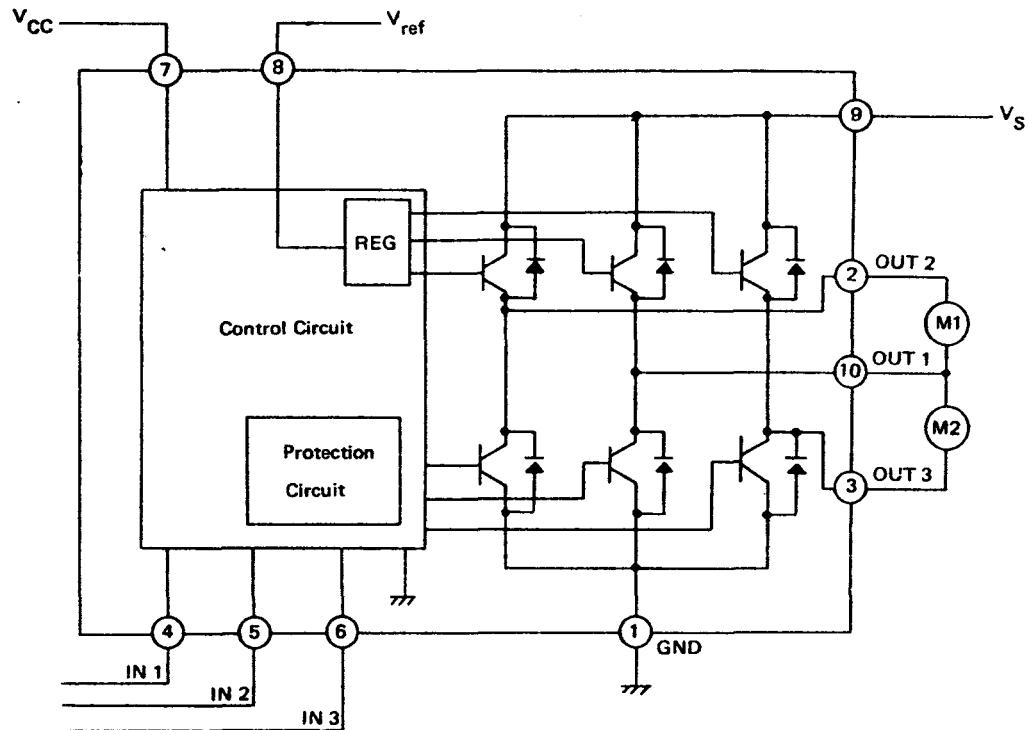


MAXIMUM RATINGS($T_a=25^\circ\text{C}$)

Characteristics		Symbol	Rating	Unit
Supply Voltage		V _{CC}	25	V
Input Voltage		V _{IN}	V _{CC}	V
Output Current	Peak	I _O (peak)	2	A
	Ave.	I _O (Ave)	1	A
Allowable Power Dissipation		P _D	12.5	W
Operating Temperature		T _{opr}	-30~+75	°C
Storage Temperature		T _{stg}	-55~+150	°C

DBL 2018-C

□ BLOCK DIAGRAM



□ LOGIC TRUTH TABLE

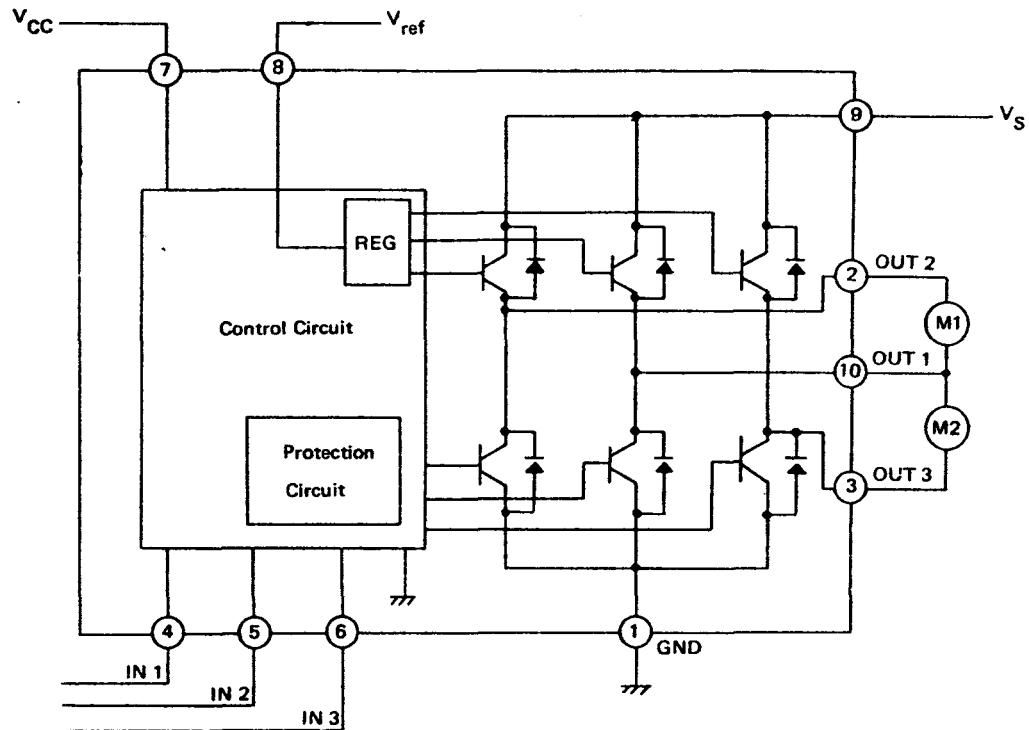
INPUT			OUTPUT			MODE	
IN 1	IN 2	IN 3	OUT 1	OUT 2	OUT 3	M 1	M 2
0	0	1/0	L	L	L	BRAKE	BRAKE
1	0	0	H	L	∞	CW/CCW	STOP
1	0	1	L	H	∞	CCW/CW	STOP
0	1	0	H	∞	L	STOP	CW/CCW
0	1	1	L	∞	H	STOP	CCW/CW
1	1	1/0	L	L	L	BRAKE	BRAKE

∞ : High Impedance

Input Level 'H' : Active

DBL 2018-C

BLOCK DIAGRAM



LOGIC TRUTH TABLE

INPUT			OUTPUT			MODE	
IN 1	IN 2	IN 3	OUT 1	OUT 2	OUT 3	M 1	M 2
0	0	1/0	L	L	L	BRAKE	BRAKE
1	0	0	H	L	∞	CW/CCW	STOP
1	0	1	L	H	∞	CCW/CW	STOP
0	1	0	H	∞	L	STOP	CW/CCW
0	1	1	L	∞	H	STOP	CCW/CW
1	1	1/0	L	L	L	BRAKE	BRAKE

∞ : High Impedance

Input Level 'H' : Active

DBL 2018-C

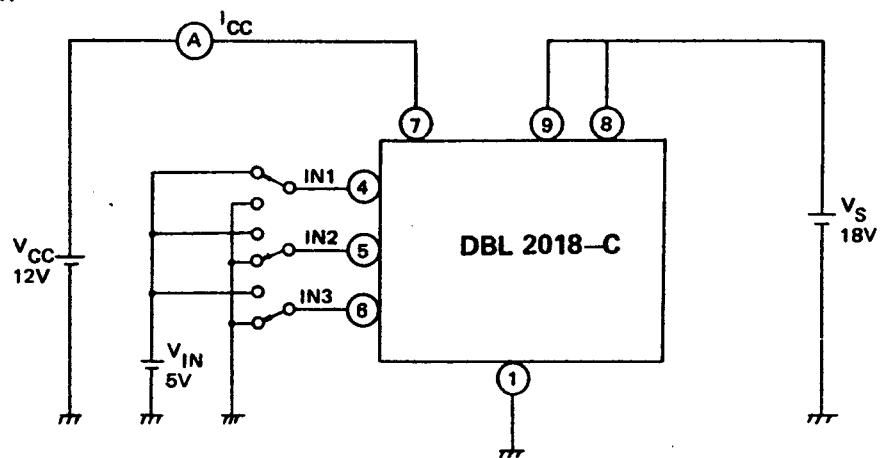
ELECTRICAL CHARACTERISTICS($V_{CC} = 12V$, $V_S = 18V$, $T_a = 25^\circ C$)

Characteristic		Symbol	Test Circuit	Test Conditions	Min.	Typ.	Max.	Unit
Supply Current		I_{CC1}	1	Output Off CW/CCW	—	17	30	mA
		I_{CC2}	1	Output off brake	—	13	25	mA
Input Voltage	1(High)	V_{IN1}	2	Pin 4,5,6	3.5	—	5.5	V
	2(Low)	V_{IN2}	2	Pin 4,5,6	GND	—	0.8	V
Input Current		I_{IN}	2	Sink $V_{IN} = 3.5V$	—	5	20	μA
Input Hysteresis Range		ΔV_T	2		—	0.7	—	V
Saturation Voltage	Upper	V_{SATU-1}	3	$V_{ref} : V_S \text{ Short; Output} - V_S$ $I_O = 0.2A$	—	0.9	1.3	V
	Lower	V_{SATL-1}	3	$V_{ref} : V_S \text{ Short; Output} - GND$ $I_O = 0.2A$	—	1.1	1.4	V
	Upper	V_{SATU-2}	3	$V_{ref} : V_S \text{ Short; Output} - V_S$ $I_O = 0.1A$	—	1.8	2.3	V
	Lower	V_{SATL-2}	3	$V_{ref} : V_S \text{ Short; Output} - GND$ $I_O = 0.1A$	—	2.4	2.9	V
Output Voltage		V_{O1}	3	$V_{ref} = 10V, I_O = 0.5A$	10.7	11	11.8	V
		V_{O2}	3	$V_{ref} = 10V, I_O = 1.0A$	10.4	10.7	11.5	V
Output Tr.	Upper	I_{LU}		$V_S = 25V$	—	—	50	μA
	Lower	I_{LL}		$V_S = 25V$	—	—	50	μA
Diode Forward Voltage	Upper	V_{FU}	4	$I_F = 1A$	0.7	2.2	2.7	V
	Lower	V_{FL}	4	$I_F = 1A$	0.1	1.4	2	V
Control Supply Current		I_{ref}	2	$V_{ref} = 10V$ Source type	—	5	30	μA

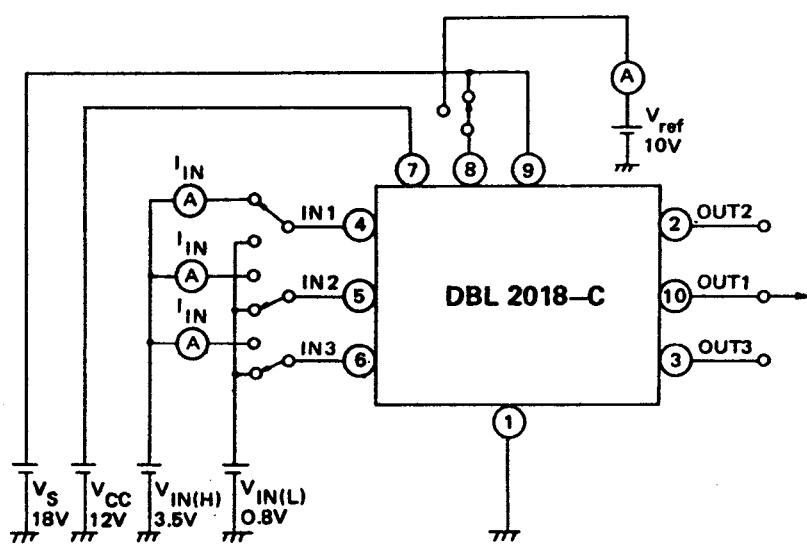
DBL 2018-C

TEST CIRCUITS

1.



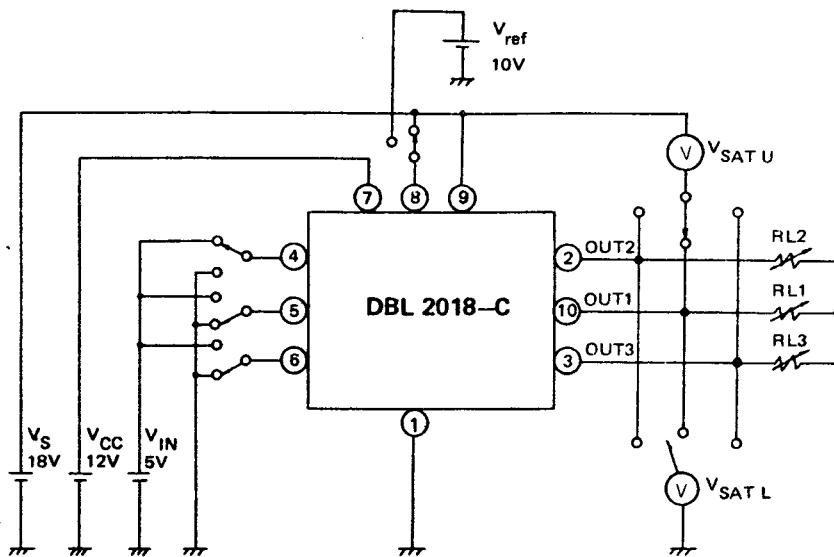
2.



DBL 2018-C

TEST CIRCUITS(Continued)

3.



Adjust R_{L1} , R_{L2} , R_{L3} , so that I_{out} may be 0.2A or 1.0A.

4.

