DG129

Dual DPST JFET Analog Switch

Features

- Standby Power: <1 mW
- Bipolar Drivers
- Constant $r_{DS(on)}$ Over Signal Range
- Off Isolation: > 60 dB @ 1 MHz
- Make-Before-Break

Benefits

- Minimizes Standby Power Requirements
- Better Radiation Tolerance
- Less Distortion
- Higher Frequency Switching
- Smooth Closed Loop Response

Applications

- Battery Powered Systems
- Aerospace Control Systems
- Low Distortion Circuits
- High Frequency Switching Circuits

Description

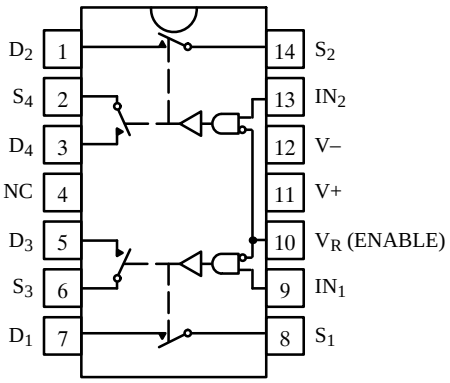
The DG129 is a dual double-pole single-throw analog switch for use in instrumentation, control, and audio communication systems. It is ideally suited for applications requiring a constant on-resistance over the entire analog range.

On-resistance for the DG129 is 20 Ω (typical), and on-leakage is < 2 nA. With all switches off, total power consumption is < 750 µW. These switches have make-before-break action and due to the processing are relatively radiation tolerant. An enable pin (V_R) simplifies interfacing with microprocessor, or other logic.

Each device contains four junction field-effect transistors (JFETs) to achieve constant on-resistance. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the on-off state of each switch. With logic “0” at the driver input the switches will be off. With a logic “1” at the input the switches will be on. In the on-state each switch will conduct current in either direction, and in the off-state each switch will block voltages up to 20 V peak-to-peak.

Functional Block Diagram and Pin Configuration

Dual-In-Line



Top View

Two DPST Switches per Package

Truth Table

Logic	Switch
0	OFF
1	ON

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.5 V

Switches Shown for Logic “0” Input

Ordering Information

Temp Range	Package	Part Number
–55 to 125°C	14-Pin Sidebraze	DG129AP/883
		781401CA

DG129

Absolute Maximum Ratings

V+ to V– . . . . . 36 V
V+ to V_D . . . . . 36 V
V_D or V_S to V– . . . . . 36 V
V_D to V_S . . . . . ±22 V
V+ to V_R . . . . . 25 V
V_R to V– . . . . . 25 V
V_{IN} to V– . . . . . 30 V
V+ to V_{IN} . . . . . 25 V
V_{IN} to V_R . . . . . ±6 V
Current (any terminal) . . . . . 30 mA
Storage Temperture . . . . . –65 to 150°C
Power Dissipationa
14-Pin DIP[b] . . . . . 825 mW

Notes:
a. All leads welded or soldered to PC Board.
b. Derate 11 mW/°C above 75°C

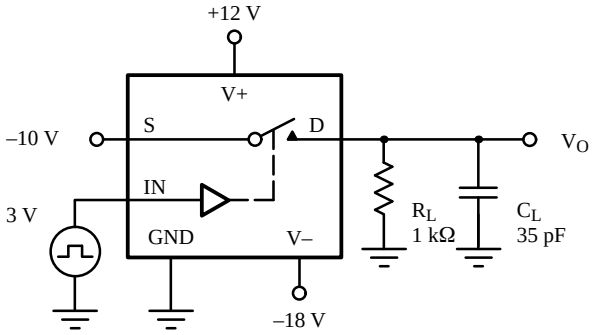
Specifications[a]

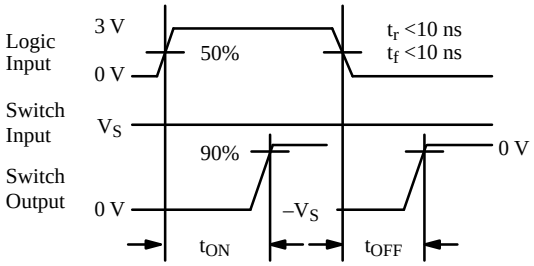
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V– = –18 V, V_R = 0 V, V_{IN} = 0.8 V or 2.5 V[f]	Temp[b]	A Suffix –55 to 125°C Min[d]	Typ[c]	Max[d]	Unit
Switch							
Analog Signal Range	V_{ANALOG}		Full	–10		10	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S= –10 mA, V_D = 10 V	Room Full		20	30 60	Ω
Source-Off Leakage Current	I_S(off)	V_S = ±10 V, V_D = ∓10 V	Room Full	–1 –100	0.03	1 100	nA
Drain-Off Leakage Current	I_D(off)	V_D = ±10 V, V_S = ∓10 V	Room Full	–1 –100	0.02	1 100	
Channel-On Leakage Current	$I_{D(on)}$	V_D = V_S = –10 V	Room Full	–2 –100	–0.03		
Input							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.5 V	Room Full		15	60 120	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8 V	Room Full		0.005	0.1 2	
Dynamic							
Turn-On Time	t_{ON}	See Figure 1	Room		0.5	0.6	µs
Turn-Off Time	t_{OFF}		Room		1.1	1.6	
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz V_D, V_S = 0	Room		2.4		pF
Drain-Off Capacitance	$C_{D(off)}$		Room		2.4		
Channel-On Capacitance	$C_{D(on)}$		Room		2.8		
Off-Isolation	OIRR	R_L = 75 Ω, f = 1 MHz	Room		> 60		dB
Supply							
Positive Supply Current	I+	One Channel On V_{IN} = 2.5 V	Room		2.5	3	mA
Negative Supply Current	I–		Room	–1.8	–1.6		
Reference Supply Current	I_R		Room	–1.4	–1.1		
Positive Supply Current	I+	All Channel Off Both V_{IN} = 0 V	Room		0.6	25	µA
Negative Supply Current	I–		Room	–25	–0.5		
Reference Supply Current	I_R		Room	–25	–0.5		

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = –55 to 125°C.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Test Circuits

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Logic “1” = Switch On

Figure 1. Switching Time

Application Hints

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_R Reference Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
12	–18	0	2.5/0.8	–10 to 10
15	–15	0	2.5/0.8	–7 to 13
7	–12	0	2.5/0.8	–5 to 5
5	–15	0	2.5/0.8	–7 to 3
5	–10	0	2.5/0.8	–2 to 3