![intersil™]

DG406/883, DG407/883

Single 16-Channel/Differential 8-Channel CMOS Analog Multiplexers

April 1997

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- ON-Resistance 100Ω (Max)
- Low Power Consumption (P_D <1.2mW)
- Fast Transition Time (300ns Max)
- Low Charge Injection
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- **Battery Operated Systems**
- **Data Acquisition**
- **Medical Instrumentation**
- **Hi-Rel Systems**
- **Communication Systems**
- **Automatic Test Equipment**

Ordering Information

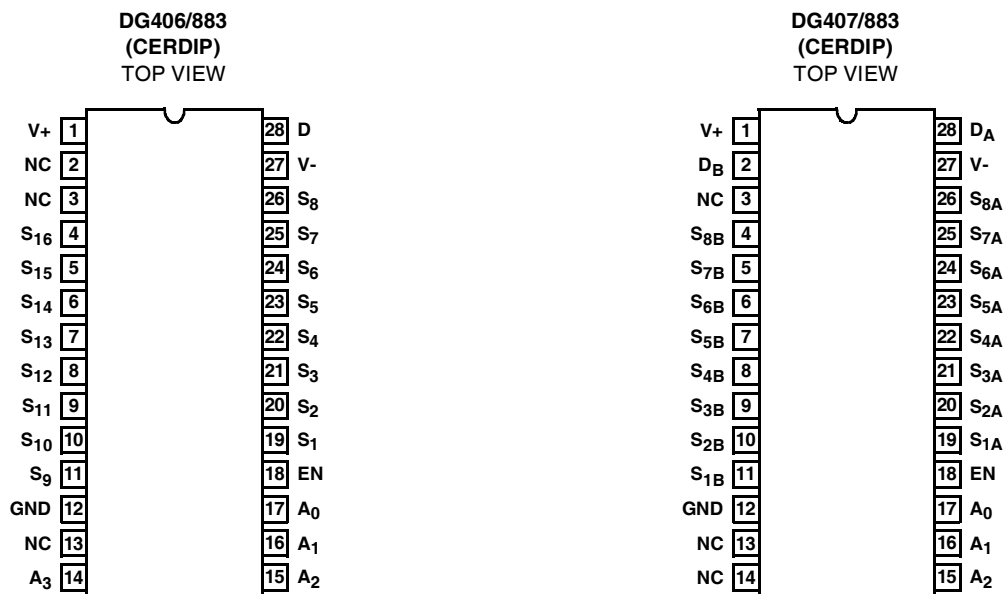| PART NUMBER	TEMP.RANGE (^oC)	PACKAGE	PKG. NO.
DG406AK/883	-55 to 125	28 Ld CERDIP	F28.6
DG407AK/883	-55 to 125	28 Ld CERDIP	F28.6

Description

The DG406/883 and DG407/883 monolithic CMOS analog multiplexers are drop-in replacements for the popular DG506A/883 and DG507A/883 series devices. They each include an array of sixteen analog switches, a TTL and CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

These multiplexers feature lower signal ON resistance (<100Ω) and faster transition time (t_{TRANS} <250ns) compared to the DG506A/883 and DG507A/883. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG406 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $30V_{P-P}$ signals when operating with ±15V power supplies.
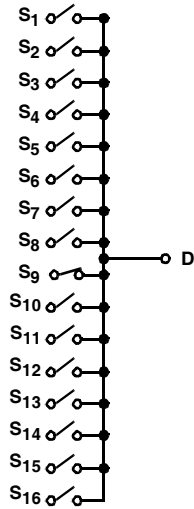
The sixteen switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.
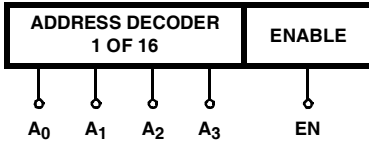
Pinouts

DG406/883 (CERDIP) TOP VIEW

V+	1	28	D
NC	2	27	V-
NC	3	26	S_8
S_{16}	4	25	S_7
S_{15}	5	24	S_6
S_{14}	6	23	S_5
S_{13}	7	22	S_4
S_{12}	8	21	S_3
S_{11}	9	20	S_2
S_{10}	10	19	S_1
S_9	11	18	EN
GND	12	17	A_0
NC	13	16	A_1
A_3	14	15	A_2

DG407/883 (CERDIP) TOP VIEW

V+	1	28	D_A
D_B	2	27	V-
NC	3	26	S_{8A}
S_{8B}	4	25	S_{7A}
S_{7B}	5	24	S_{6A}
S_{6B}	6	23	S_{5A}
S_{5B}	7	22	S_{4A}
S_{4B}	8	21	S_{3A}
S_{3B}	9	20	S_{2A}
S_{2B}	10	19	S_{1A}
S_{1B}	11	18	EN
GND	12	17	A_0
NC	13	16	A_1
NC	14	15	A_2

Spec Number **512041-883**

FN3720.1

Functional Block Diagrams

DG406

DG407

TO DECODER LOGIC
CONTROLLING BOTH
TIERS OF MUXING

ADDRESS DECODER 1 OF 16	ENABLE

A_0 A_1 A_2 A_3 EN

TO DECODER LOGIC
CONTROLLING BOTH
TIERS OF MUXING

ADDRESS DECODER 1 OF 8	ENABLE

A_0 A_1 A_2 EN

DG406 TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
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1	1	1	0	1	15
1	1	1	1	1	16
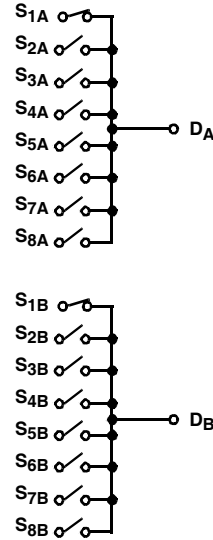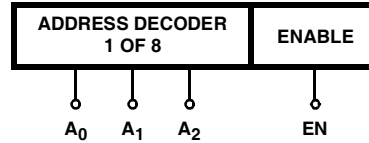
DG407 TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} < 0.8V$
Logic "1" = $V_{AH} > 2.4V$
X = Don't Care

Absolute Maximum Ratings

Voltages Referenced to V-

V+ . . . . +44.0V

GND 25V

Digital Inputs, V_S, V_D (Note 1) . . . . . . (V-) -2V to (V+) +2V or 20mA, Whichever Occurs First

Current (Any Terminal) 30mA

Peak Current, S or D 100mA

(Pulsed 1ms, 10% Duty Cycle Max)

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
CERDIP Package	55	12

Maximum Junction Temperature. . . . . 150°C

Maximum Storage Temperature Range . . . . -65°C to 150°C

Operating Conditions

Temperature Range . . . . -55°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Devices tested at +V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUP	DEVICE TYPE	(NOTE 3) MIN	(NOTE 3) MAX	UNITS
Drain-Source ON Resistance	$r_{DS(ON)}$	V_D = 10V, I_S = -10mA VD = -10V, IS = 10mA (Note 4)	1, 3	All	-	90	Ω
			2	All	-	120	Ω
Matching Between Channels	$\Delta r_{DS(ON)}$	$r_{DS(ON)}$ Max - $r_{DS(ON)}$ Min (Note 3)	1	All	-	15	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = +10V	1	All	-0.5	0.5	nA
			2, 3	All	-50	50	nA
Drain OFF Leakage Current DG406	$I_{D(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = +10V	1	DG406	-1	1	nA
			2, 3		-200	200	nA
DG407			1	DG407	-1	1	nA
			2, 3		-100	100	nA
Drain ON Leakage Current DG406	$I_{D(ON)}$	V_S = V_D = ±10V Sequence Each Switch ON (Note 4)	1	DG406	-1	1	nA
			2, 3		-200	200	nA
DG407			1	DG407	-1	1	nA
			2, 3		-100	100	nA
Logic High Input Current	I_{AH}	V_A = 2.4V, 15V	1, 2, 3	All	-1	1	μA
Logic Low Input Current	I_{AL}	V_{EN} = 0V, 2.4V, V_A = 0V	1, 2, 3	All	-1	1	μA
Positive Supply Current	I_{CC}	V_{EN} = 2.4V, V_A = 0V	1	All	-	100	μA
			2, 3	All	-	500	μA
Negative Supply Current	I_{EE}		1	All	-1	-	μA
			2, 3	All	-10	-	μA

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Devices tested at +V$_{SUPPLY}$ = +15V, -V$_{SUPPLY}$ = -15V, V$_{AL}$ = 0.8V, V$_{AH}$ = 2.4V, Unless Otherwise Specified   **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUP	DEVICE TYPE	(NOTE 3) MIN	(NOTE 3) MAX	UNITS
Positive Standby Current	I$_{CC}$ Standby	V$_{EN}$ = V$_A$ = 0V or 5V	1	All	-	30	μA
			2, 3	All	-	75	μA
Negative Standby Current	I$_{EE}$ Standby		1	All	-1	-	μA
			2, 3	All	-10	-	μA

NOTES:

3. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

4. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

TABLE 1A. ELECTRICAL PERFORMANCE SPECIFICATIONS (SINGLE SUPPLY)

Devices tested at +V$_{SUPPLY}$ = +12V, -V$_{SUPPLY}$ = 0V, V$_{AL}$ = 0.8V, V$_{AH}$ = 2.4V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUP	DEVICE TYPE	MIN	MAX	UNITS
Drain-Source ON Resistance	r$_{DS(ON)}$	V$_D$ = 3V, 10V I$_S$ = -1mA	1	All	-	120	Ω
Positive Current	I$_{CC}$	V$_{EN}$ = 0V or 5V, V$_A$ = 0V or 5V	1	All	-	30	μA
			2, 3	All	-	75	μA
Negative Current	I$_{EE}$		1	All	-1	-	μA
			2, 3	All	-5	-	μA
Switching Time of Multiplexer	t$_{TRANS}$	V$_{S1}$ = 8V, V$_{SS}$ - 0V, V$_{IN}$ = 2.4V	1	All	-	450	ns
Enable Turn-ON Time	t$_{ON(EN)}$	V$_{INH}$ = 2.4V, V$_{INL}$ = 0V, V$_{S1}$ = 5V	1	All	-	600	ns
Enable Turn-OFF Time	t$_{OFF(EN)}$		1	All	-	300	ns

TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Devices tested at +V$_{SUPPLY}$ = +15V, -V$_{SUPPLY}$ = -15V, V$_{AL}$ = 0.8V, V$_{AH}$ = 2.4V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUP	DEVICE TYPE	MIN	MAX	UNITS
Transition Time	t$_{TRANS}$	C$_L$ = 35pF, R$_L$ = 300Ω, See Figure 1	9	All	-	300	ns
			10, 11	All	-	400	ns
Enable Turn-ON Time	t$_{ON(EN)}$	C$_L$ = 35pF, R$_L$ = 300Ω, See Figure 2	9	All	-	200	ns
			10, 11	All	-	400	ns
Enable Turn-OFF Time	t$_{OFF(EN)}$		9	All	-	150	ns
			10, 11	All	-	300	ns
Break Before Leakage Current	t$_{OPEN}$	C$_L$ = 35pF, R$_L$ = 300Ω, See Figure 3	9	All	25	-	ns
			10, 11	All	10	-	ns

TABLE 3. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Devices tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP (^{o}C)	MIN	TYP	MAX	UNITS
Off Isolation Time	V_{ISO}	V_{EN} = 0V, R_L = 1K, f = 100kHz, GEN = 1V_{P-P} Sine Wave, See Figure 5	5	25	50	-	-	dB
Charge Transfer Error	V_{CTE}	C_L = 10nF, V_S = 0V, R_S = 0Ω, See Figure 4	5	25	-	-	10	mV
Crosstalk	V_{CT}	R_L = 1K, f = 100kHz, GEN = 1V_{P-P} Sine Wave, See Figure 5	5	25	50	-	-	dB
Source OFF Capacitance	$C_{S(OFF)}$	V_{EN} = 0V, V_S = 0V, f = 1MHz	65	25	-	-	10	pF
Drain OFF Capacitance DG406	$C_{D(OFF)}$	V_{EN} = 0V, V_D = 0V, f = 1MHz	5	25	-	-	200	pF
DG407			5	25	-	-	100	pF
Drain ON Capacitance DG406	$C_{D(ON)}$	V_{EN} = 0V, V_D = 0V, f = 1MHz	5	25	-	-	400	pF
DG407			5	25	-	-	200	pF

NOTE:

5. Parameters listed via process parameters and are not directly tested at final production. These parameters are lab characterized upon design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production rich reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn0In)	1
Final Electrical Test Parameters	1 (Note 6), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Group C and D Endpoints	1

NOTE:

6. PDA applied to Subgroup 1 only.

Test Circuits and Waveforms
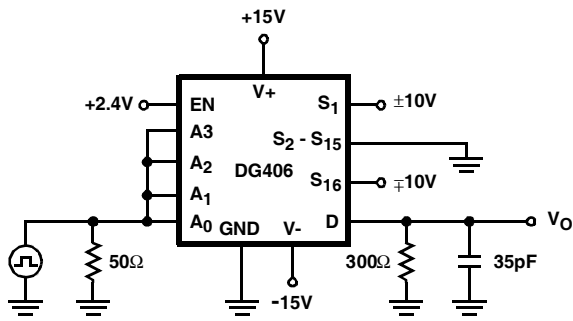
FIGURE 1A.
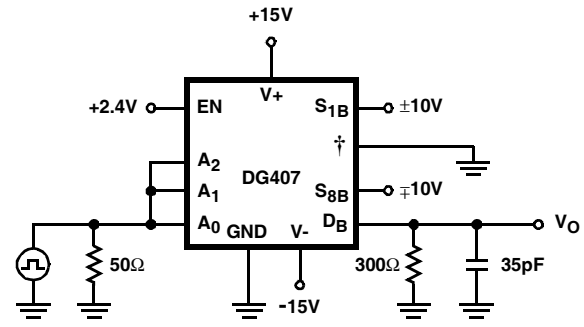
$\dagger$ = S_{1A} - S_{8A}, S_{2B} - S_{7B}, D_A
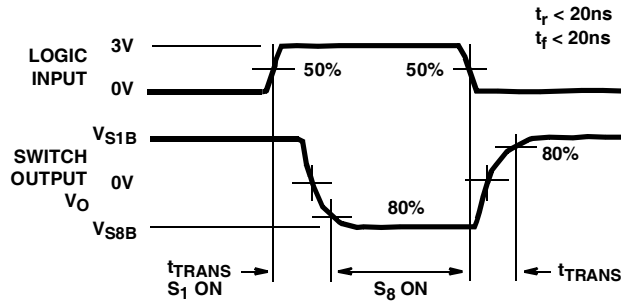
FIGURE 1B.

FIGURE 1C.

FIGURE 1. TRANSITION TIME
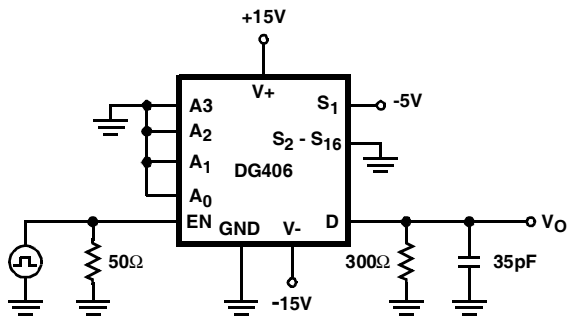
FIGURE 2A.
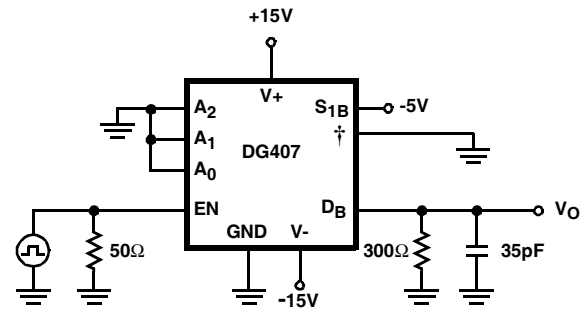
$\dagger$ = S_{1A} - S_{8A}, S_{2B} - S_{8B}, D_A
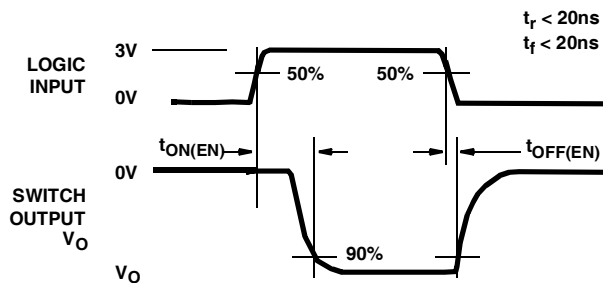
FIGURE 2B.

FIGURE 2C.

Test Circuits and Waveforms (Continued)

FIGURE 2. ENABLE SWITCHING TIME
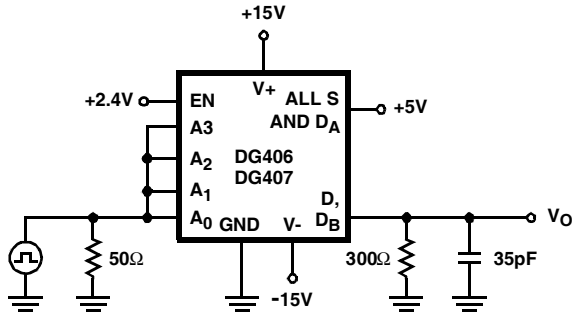
FIGURE 3A.
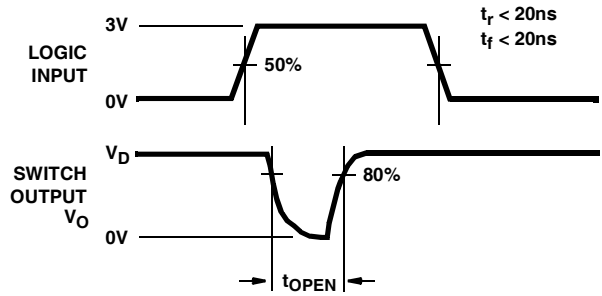
FIGURE 3B.

FIGURE 3. BREAK-BEFORE-MAKE INTERVAL
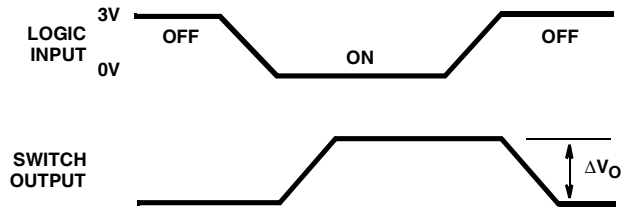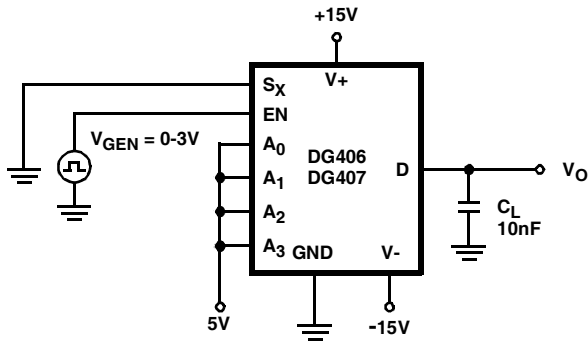
FIGURE 4. CHARGE INJECTION

OFF ISOLATION = $20 \text{LOG} \left| \dfrac{V_{OUT}}{V_{IN}} \right|$
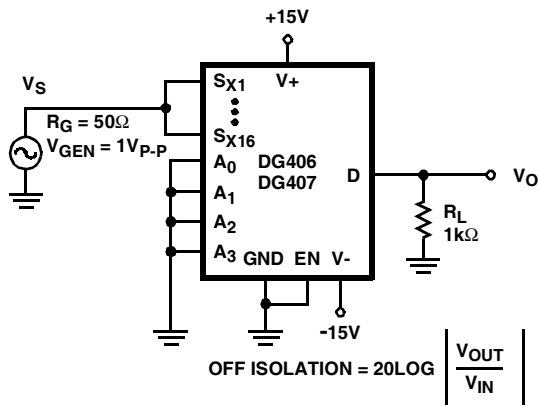
FIGURE 5. OFF ISOLATION

CROSSTALK = $20 \text{LOG} \left| \dfrac{V_{OUT}}{V_{IN}} \right|$
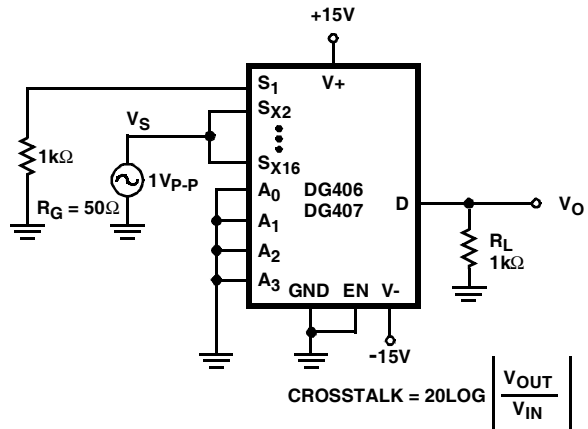
FIGURE 6. CROSSTALK

Burn-In Circuit

CERDIP BURN-IN SCHEMATIC
DG406/407AK/883
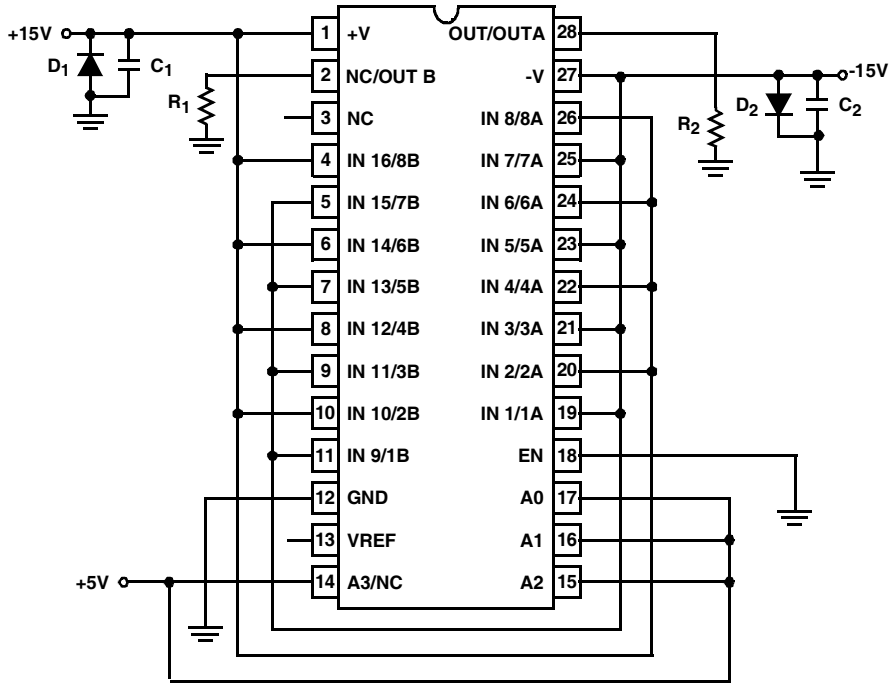
NOTE:

R_1, R_2 = 10kΩ ±5%, 1/2W or 1/4W (Per Socket)
C_1, C_2 = 0.01μF (Min, Per Socket) or 0.1μF (Min, Per Row)
D_1, D_2 = IN402 (or Equivalent, Per Board)

Schematic Diagram (Typical Channel)

Spec Number **512041-883**
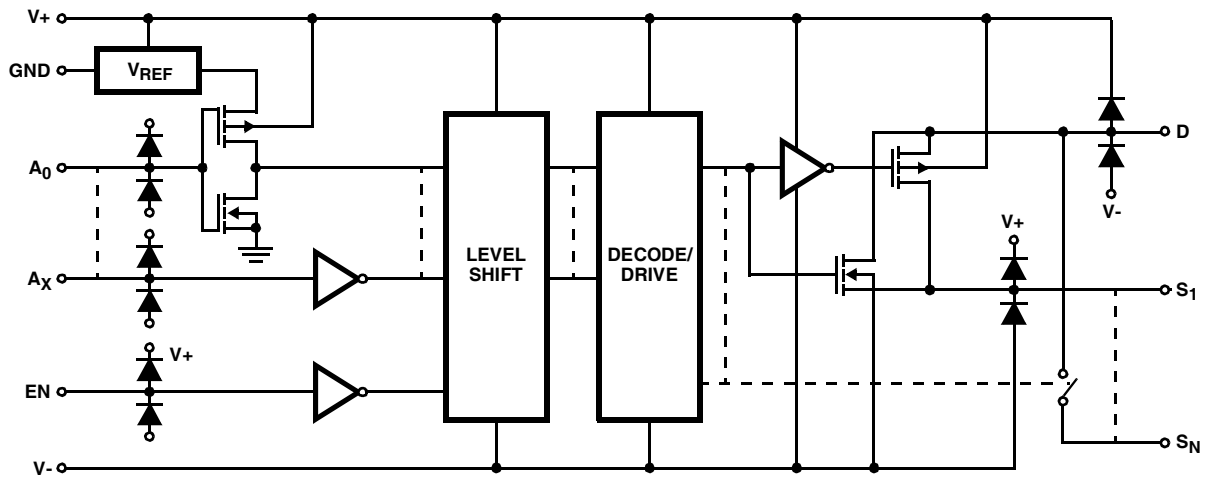
Typical Design Information

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves
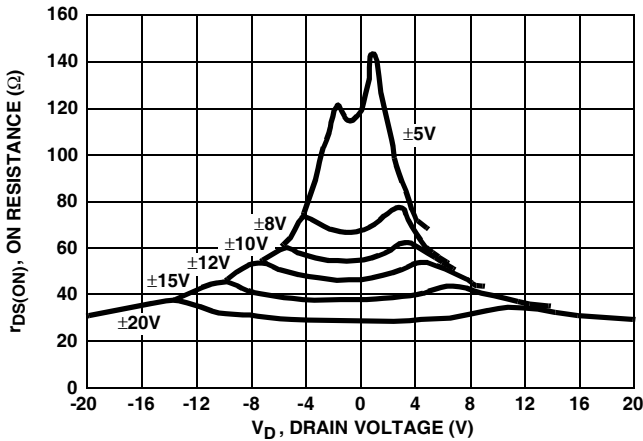
FIGURE 7. $r_{DS(ON)}$ vs V_D AND SUPPLY
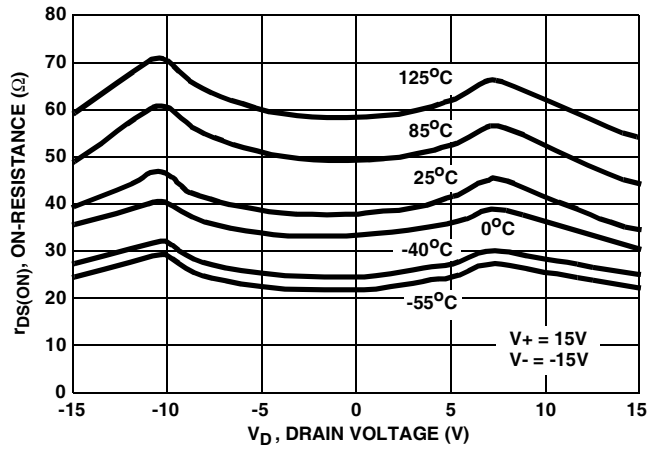
FIGURE 8. $r_{DS(ON)}$ vs V_D AND TEMPERATURE
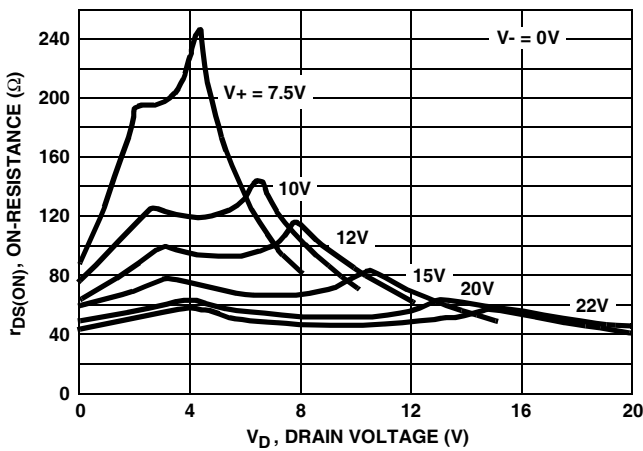
FIGURE 9. $r_{DS(ON)}$ vs V_D AND SUPPLY
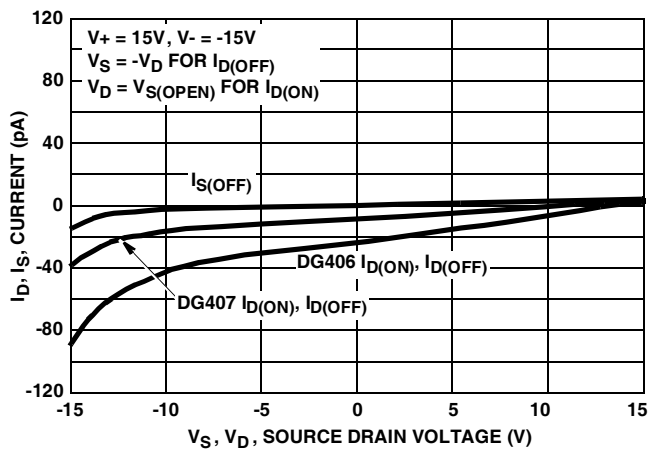
FIGURE 10. I_D, I_S LEAKAGE CURRENTS vs ANALOG VOLTAGE

Typical Performance Curves (Continued)
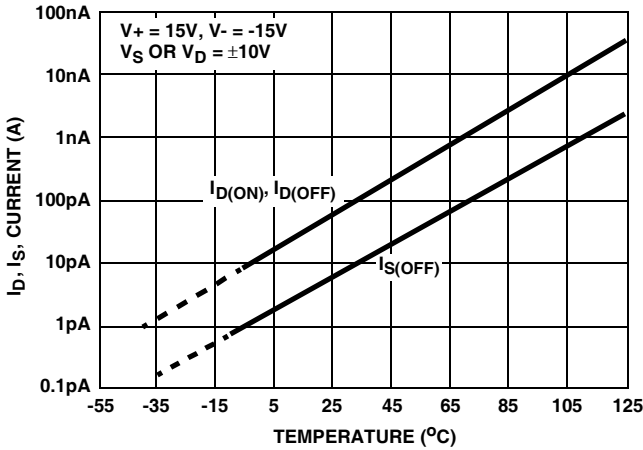
FIGURE 11. I_D, I_S LEAKAGE vs TEMPERATURE
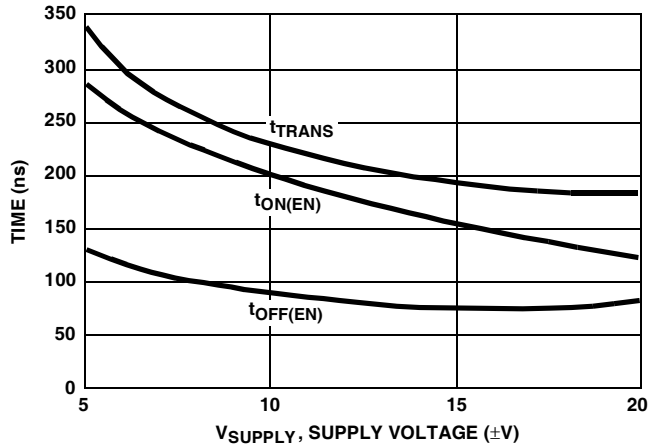
FIGURE 12. SWITCHING TIMES vs BIPOLAR SUPPLIES
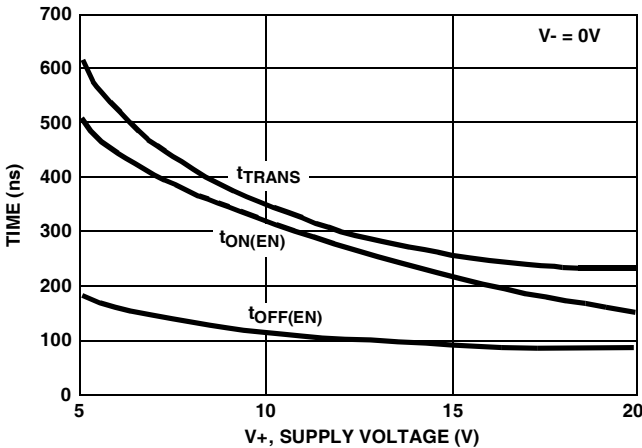
FIGURE 13. SWITCHING TIMES vs SINGLE SUPPLY
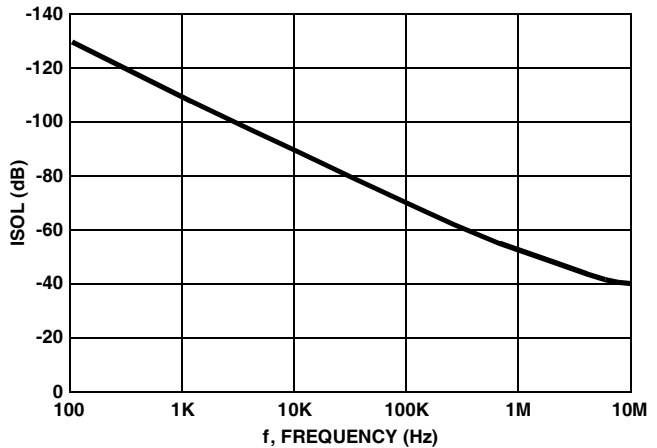
FIGURE 14. OFF-ISOLATION vs FREQUENCY
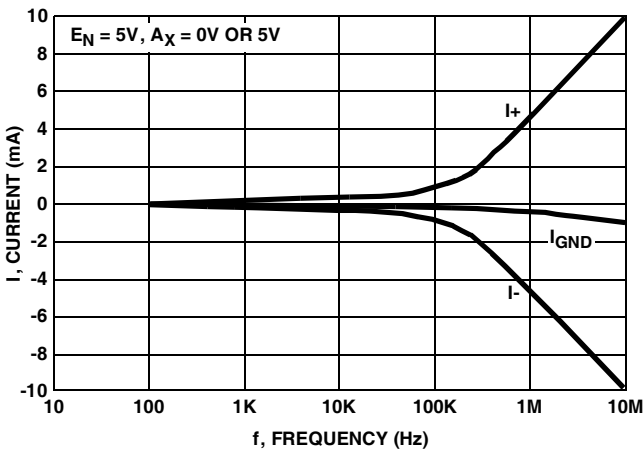
FIGURE 15. SUPPLY CURRENTS vs SWITCHING FREQUENCY
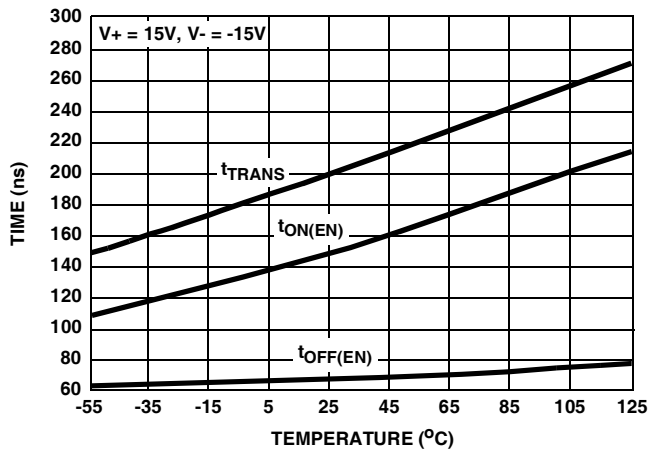
FIGURE 16. t_{ON}/t_{OFF} vs TEMPERATURE

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Typical Performance Curves (Continued)
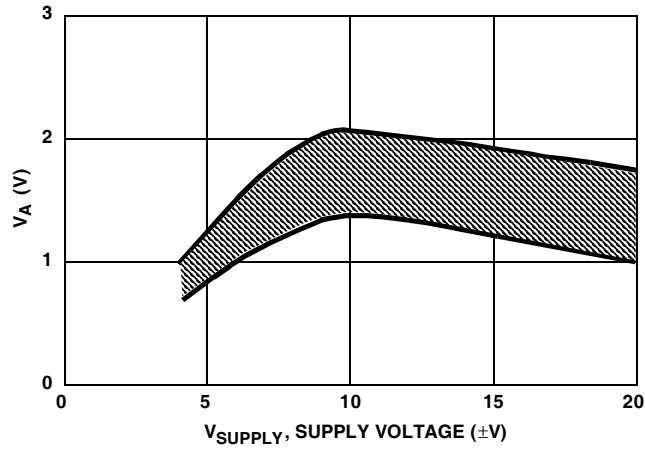
FIGURE 17. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

DG406/883, DG407/883

Die Characteristics

DIE DIMENSIONS:

2490μm x 4560μm x 485μm ±25μm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

9.1×10^4 A/cm^2

Metallization Mask Layout

DG406/883

Die Characteristics

DIE DIMENSIONS:

2490μm x 4560μm x 485μm ±25μm
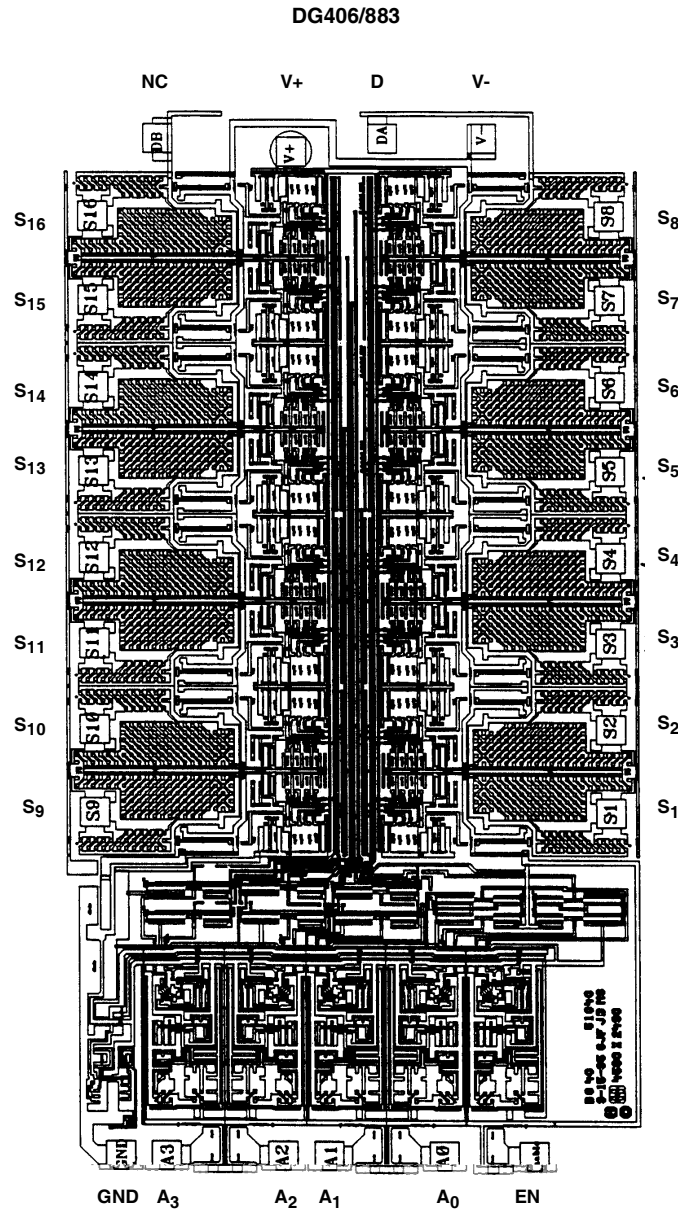
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)

F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE
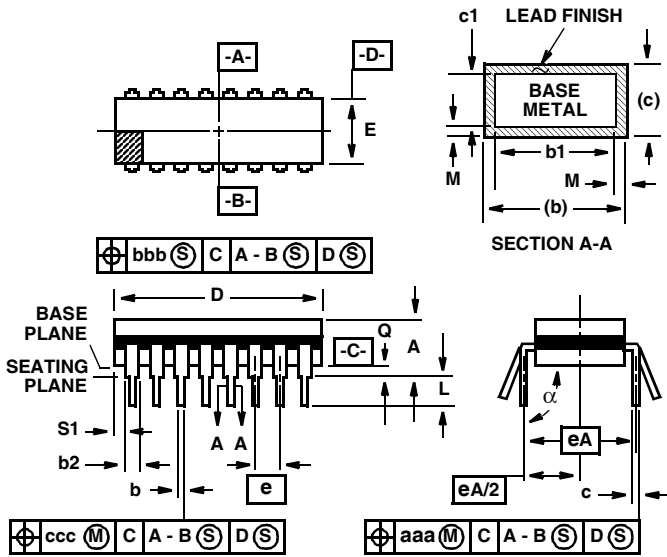
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	28		28		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.

2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.

3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.

4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.

5. This dimension allows for off-center lid, meniscus, and glass overrun.

6. Dimension Q shall be measured from the seating plane to the base plane.

7. Measure dimension S1 at all four corners.

8. N is the maximum number of terminal positions.

9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

10. Controlling dimension: INCH.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
7585 Irvine Center Drive
Suite 100
Irvine, CA 92618
TEL: (949) 341-7000
FAX: (949) 341-7123

Intersil Corporation
2401 Palm Bay Rd.
Palm Bay, FL 32905
TEL: (321) 724-7000
FAX: (321) 724-7946

EUROPE
Intersil Europe Sarl
Ave. William Graisse, 3
1006 Lausanne
Switzerland
TEL: +41 21 6140560
FAX: +41 21 6140579

ASIA
Intersil Corporation
Unit 1804 18/F Guangdong Water Building
83 Austin Road
TST, Kowloon Hong Kong
TEL: +852 2723 6339
FAX: +852 2730 1433

Spec Number **512041-883**