DLPC3478 Display and Light Controller

1 Features

- Display and Light Controller for DLP3010 (.3 720p) TRP DMD
- Display Features:
  - Supports Input Image Sizes Up to 720p
  - Input Frame Rates to 120 Hz (2D and 3D)
  - 24-Bit, Input Pixel Interface Support
    - Parallel or BT656, Interface Protocols
    - Pixel Clock Up to 150 MHz
  - Image Processing - IntelliBright™ Algorithms, Image Resizing, 1D Keystone, CCA, Programmable Degamma
- Light Control Features:
  - Pattern Display Optimized for Machine Vision and Digital Exposure
  - Flexible Internal (1D) and External (2D) Pattern Streaming Modes
    - Programmable Exposure Times
    - High Speed Pattern Rates Up to 2500 Hz (1-bit) and 360 Hz (8-bit)
  - Programmable 2D Static Patterns via Splash
  - Internal Pattern Streaming Mode Enables Simplified System Design
    - Eliminates Video Interface Requirement
    - Store >1000 Patterns in Flash Memory
  - Flexible Trigger Signals for Camera/Sensor Synchronization
    - One Configurable Input Trigger
    - Two Configurable Output Triggers
- System Features:
  - I^2C Control of Device Configuration
  - Programmable Splash Screens
  - Programmable LED Current Control
  - Auto DMD Parking at Power Down

2 Applications

- Battery Powered Mobile Accessory HD Projectors
- Embedded Projection (Notebooks, Laptops, Tablets, Hot Spots)
- 3D Scanners: 3D Camera, 3D Reconstruction, AR/VR, Dental Scanner
- 3D Machine Vision: Robotics, Metrology, In-line Inspection (AOI)
- 3D Biometrics: Facial and Finger Print Recognition
- Light Exposure: 3D Printers, Laser Marking

3 Description

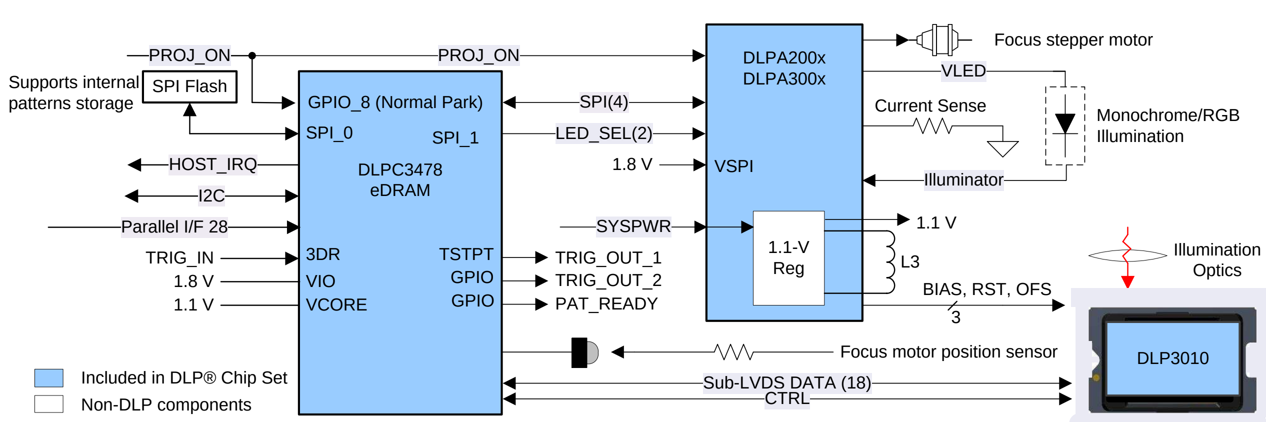
The DLPC3478 display and light controller supports reliable operation of the DLP3010 digital micromirror device (DMD) for video display and light control applications. The DLPC3478 controller provides a convenient interface between user electronics and the DMD to display video and steer light patterns with high speed, precision, and efficiency.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPC3478	NFBGA (201)	13.00 × 13.00 mm^2

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Standalone System



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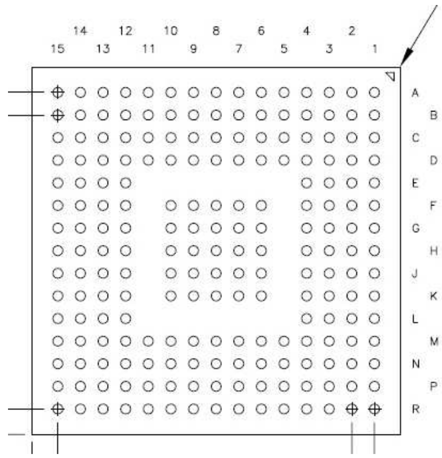
• First public release of full data sheet	1

5 Pin Configuration and Functions

ZEZ Package
201-Pin NFBGA
Bottom View



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DMD_LS_CLK	DMD_LS_WDATA	DMD_HS_WDATAH_P	DMD_HS_WDATAG_P	DMD_HS_WDATAF_P	DMD_HS_WDATAE_P	DMD_HS_CLK_P	DMD_HS_WDATAD_P	DMD_HS_WDATAC_P	DMD_HS_WDATAB_P	DMD_HS_WDATAA_P	CMP_OUT	SPI0_CLK	SPI0_CSZ0	CMP_PWM
B	DMD_DEN_ARSTZ	DMD_LS_RDATA	DMD_HS_WDATAH_N	DMD_HS_WDATAG_N	DMD_HS_WDATAF_N	DMD_HS_WDATAE_N	DMD_HS_CLK_N	DMD_HS_WDATAD_N	DMD_HS_WDATAC_N	DMD_HS_WDATAB_N	DMD_HS_WDATAA_N	SPI0_DIN	SPI0_DOUT	LED_SEL_1	LED_SEL_0
C	DD3P	DD3N	VDDLP12	VSS	VDD	VSS	VCC	VSS	VCC	HWTEST_EN	RESETZ	SPI0_CSZ1	PARKZ	GPIO_00	GPIO_01
D	DD2P	DD2N	VDD	VCC	VDD	VSS	VDD	VSS	VDD	VSS	VCC_FLSH	VDD	VDD	GPIO_02	GPIO_03
E	DCLKP	DCLKN	VDD	VSS								VCC	VSS	GPIO_04	GPIO_05
F	DD1P	DD1N	RREF	VSS		VSS	VSS	VSS	VSS	VSS		VCC	VDD	GPIO_06	GPIO_07
G	DD0P	DD0N	VSS_PLLM	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VSS	GPIO_08	GPIO_09
H	PLL_REFCLK_I	VDD_PLLM	VSS_PLLD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VDD	GPIO_10	GPIO_11
J	PLL_REFCLK_O	VDD_PLLD	VSS	VDD		VSS	VSS	VSS	VSS	VSS		VDD	VSS	GPIO_12	GPIO_13
K	PDATA_1	PDATA_0	VDD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VCC	GPIO_14	GPIO_15
L	PDATA_3	PDATA_2	VSS	VDD								VDD	VDD	GPIO_16	GPIO_17
M	PDATA_5	PDATA_4	VCC_INTF	VSS	VSS	VDD	VCC_INTF	VSS	VDD	VDD	VCC	VSS	JTAGTMS1	GPIO_18	GPIO_19
N	PDATA_7	PDATA_6	VCC_INTF	PDM_CVS_TE	HSYNC_CS	3DR	VCC_INTF	HOST_IRQ	IIC0_SDA	IIC0_SCL	JTAGTMS2	JTAGTDO2	JTAGTDO1	TSTPT_6	TSTPT_7
P	VSYNC_WE	DATEN_CMD	PCLK	PDATA_11	PDATA_13	PDATA_15	PDATA_17	PDATA_19	PDATA_21	PDATA_23	JTAGTRSTZ	JTAGTCK	JTAGTDI	TSTPT_4	TSTPT_5
R	PDATA_8	PDATA_9	PDATA_10	PDATA_12	PDATA_14	PDATA_16	PDATA_18	PDATA_20	PDATA_22	IIC1_SDA	IIC1_SCL	TSTPT_0	TSTPT_1	TSTPT_2	TSTPT_3

Pin Functions – Board Level Test, Debug, and Initialization

PIN		I/O	DESCRIPTION
NAME	NUMBER		
HWTEST_EN	C10	I_6	Manufacturing test enable signal. Connect this signal directly to ground on the PCB for normal operation.
PARKZ	C13	I_6	DMD fast PARK control (active low Input) (hysteresis buffer). PARKZ must be set high to enable normal operation. Set PARKZ high prior to releasing RESETZ (that is, prior to the low-to-high transition on the RESETZ input). Set PARKZ low for a minimum of 32 µs before any power is removed from the DLPC3478 such that the fast DMD PARK operation can be completed. Note for PARKZ, use fast PARK control only when loss of power is eminent and beyond the control of the host processor (for example, when the external power source has been disconnected or the battery has dropped below a minimum level). The longest lifetime of the DMD may not be achieved with the fast PARK operation. The longest lifetime is achieved with a normal PARK operation. Because of this, PARKZ is typically used in conjunction with a normal PARK request control input through GPIO_08. The difference being that when the host sets PROJ_ON low, which connects to both GPIO_08 and the DLPA200x or DLPA300x PMIC chip, the takes much longer than 32 µs to park the mirrors. The DLPA200x or DLPA300x holds on all power supplies, and keep RESETZ high, until the longer mirror parking has completed. This longer mirror parking time, of up to 500 µs, ensures the longest DMD lifetime and reliability. The DLPA200x or DLPA300x monitors power to the and detects an eminent power loss condition and drives the PARKZ signal accordingly.
Reserved	P12	I_6	TI internal use. Leave unconnected.
Reserved	P13	I_6	TI internal use. Leave unconnected.
Reserved	N13(1)	O_1	TI internal use. Leave unconnected.
Reserved	N12(1)	O_1	TI internal use. Leave unconnected.
Reserved	M13	I_6	TI internal use. Leave unconnected.
Reserved	N11	I_6	TI internal use. Leave unconnected.
Reserved	P11	I_6	TI internal use This pin must be tied to ground, through an external 8-kΩ, or less, resistor for normal operation. Failure to tie this pin low during normal operation causes startup and initialization problems.
RESETZ	C11	I_6	power-on reset (active low input) (hysteresis buffer). Self-configuration starts when a low-to-high transition is detected on RESETZ. All ASIC power and clocks must be stable before this reset is de-asserted. Note that the following signals become tri-stated while RESETZ is asserted: SPI0_CLK, SPI0_DOUT, SPI0_CSZ0, SPI0_CSZ1, and GPIO(19:00) External pullups or downs (as appropriate) are typically added to all tri-stated output signals listed (including bidirectional signals to be configured as outputs) to avoid floating ASIC outputs during reset if connected to devices on the PCB that can malfunction. For SPI, at a minimum, any chip selects connected to the devices typically have a pullup. Unused bidirectional signals can be functionally configured as outputs to avoid floating ASIC inputs after RESETZ is set high. The following signals are forced to a logic low state while RESETZ is asserted and corresponding I/O power is applied: LED_SEL_0, LED_SEL_1 and DMD_DEN_ARSTZ No signals operate in active state while RESETZ is asserted. Note that no I^2C activity is permitted for a minimum of 500 ms after RESETZ (and PARKZ) are set high.
TSTPT_0	R12	B_1	Test pin 0 (includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ, and then driven as an output. Normal use: reserved for test output. Leave open for normal use. Note: Do not apply an external pullup component to this pin to avoid putting the in a test mode. Without external pullup (2): Feeds TMSEL(0) With external pullup(3): Feeds TMSEL(0)

(1) If operation does not call for an external pullup and there is no external logic that might overcome the weak internal pulldown resistor, then this I/O can be left open or unconnected for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.
(2) External pullup resistor must be 8 kΩ, or less, for pins with internal pullup or down resistors.
(3) If operation does not call for an external pullup and there is no external logic that might overcome the weak internal pulldown resistor, then the TSTPT I/O can be left open/ unconnected for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.

Pin Functions – Board Level Test, Debug, and Initialization (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
TSTPT_1	R13	B_1	Test pin 1 (includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for test output. Leave open for normal use. Note: Do not apply an external pullup component to this pin to avoid putting the in a test mode. Without external pullup(2) Feeds TMSEL(1) — With external pullup(3) Feeds TMSEL(1)
TSTPT_2	R14	B_1	Test pin 2 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for test output. Leave open for normal use. Note: Do not apply an external pullup component to this pin to avoid putting the in a test mode. Without external pullup(2) Feeds TMSEL(2) — With external pullup(3) Feeds TMSEL(2)
TSTPT_3	R15	B_1	Test pin 3 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for for test output. Leave open for normal use.
TSTPT_4	P14	B_1	Test pin 4 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for test output. Leave open for normal use. Reserved for TRIG_OUT_1 signal (Output).
TSTPT_5	P15	B_1	Test pin 5 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for test output. Leave open or unconnected for normal use.
TSTPT_6	N14	B_1	Test pin 6 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for test output. Leave open for normal use. Alternative use: none. External logic shall not unintentionally pull this pin high to avoid putting the in a test mode.
TSTPT_7	N15	B_1	Test pin 7 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for test output. Leave open for normal use.

Pin Functions – Parallel Port Input Data and Control(1)(2)

PIN		I/O	DESCRIPTION	
NAME	NUMBER		PARALLEL RGB MODE	BT656 INTERFACE MODE
PCLK	P3	I_{11}	Pixel clock(3)	Pixel clock(3)
PDM_CVS_TE	N4	B_5	Parallel data mask(4)	Unused(5)
VSYNC_WE	P1	I_{11}	Vsync(6)	Unused(5)
HSYNC_CS	N5	I_{11}	Hsync(6)	Unused(5)
DATAEN_CMD	P2	I_{11}	Data Valid(6)	Unused(5)
			(TYPICAL RGB 888)	
PDATA_0 PDATA_1 PDATA_2 PDATA_3 PDATA_4 PDATA_5 PDATA_6 PDATA_7	K2 K1 L2 L1 M2 M1 N2 N1	I_{11}	Blue (bit weight 1) Blue (bit weight 2) Blue (bit weight 4) Blue (bit weight 8) Blue (bit weight 16) Blue (bit weight 32) Blue (bit weight 64) Blue (bit weight 128)	BT656_Data (0) BT656_Data (1) BT656_Data (2) BT656_Data (3) BT656_Data (4) BT656_Data (5) BT656_Data (6) BT656_Data (7)
			(TYPICAL RGB 888)	
PDATA_8 PDATA_9 PDATA_10 PDATA_11 PDATA_12 PDATA_13 PDATA_14 PDATA_15	R1 R2 R3 P4 R4 P5 R5 P6	I_{11}	Green (bit weight 1) Green (bit weight 2) Green (bit weight 4) Green (bit weight 8) Green (bit weight 16) Green (bit weight 32) Green (bit weight 64) Green (bit weight 128)	Unused
			(TYPICAL RGB 888)	
PDATA_16 PDATA_17 PDATA_18 PDATA_19 PDATA_20 PDATA_21 PDATA_22 PDATA_23	R6 P7 R7 P8 R8 P9 R9 P10	I_{11}	Red (bit weight 1) Red (bit weight 2) Red (bit weight 4) Red (bit weight 8) Red (bit weight 16) Red (bit weight 32) Red (bit weight 64) Red (bit weight 128)	Unused
3DR	N6		3D reference • For 3D applications: left or right 3D reference (left = 1, right = 0). To be provided by the host when a 3D command is not provided. Must transition in the middle of each frame (no closer than 1 ms to the active edge of VSYNC) • For light control applications: Reserved for TRIG_IN (Input). Applicable in Internal Pattern Streaming Mode only. • If a 3D or light control application are not being used (i.e. 3DR input is not being used), then this input is typically pulled low through an external resister (8 kΩ or less).	

(1) PDATA(23:0) bus mapping is pixel format and source mode dependent. See later sections for details.
(2) PDM_CVS_TE is optional for parallel interface operation. Ground unused inputs or pull down to ground through an external resistor (8 kΩ or less).
(3) Pixel clock capture edge is software programmable.
(4) The parallel data mask signal input is optional for parallel interface operations. Ground unused inputs or pull down to ground through an external resistor (8 kΩ or less).
(5) Ground unused inputs or pull down to ground through an external resistor (8 kΩ or less).
(6) VSYNC, HSYNC, and DATAEN polarity is software programmable.

Pin Functions - DSI Input Data and Clock[(1)]

Added PIN		I/O	DESCRIPTION
NAME	NUMBER		MIPI DSI MODE
DCLKN DCLKP	E2 E1	B_{10}	Not supported in this device. This pin must remain unconnected and left floating.
DD0N DD0P DD1N DD1P DD2N DD2P DD3N DD3P	G2 G1 F2 F1 D2 D1 C2 C1	B_{10}	Not supported in this device. This pin must remain unconnected and left floating.
RREF	F3		Not supported in this device. This pin must remain unconnected and left floating.

(1) This device supports none of these pins. These pins must remain unconnected and left floating.

Pin Functions – DMD Reset and Bias Control

PIN		I/O	DESCRIPTION
NAME	NUMBER		
DMD_DEN_ARSTZ	B1	O_2	DMD driver enable (active high)/ DMD reset (active low). Assuming the corresponding I/O power is supplied, this signal is driven low after the DMD is parked and before power is removed from the DMD. If the 1.8-V power to the is independent of the 1.8-V power to the DMD, then TI recommends a weak, external pulldown resistor to hold the signal low in the event power is inactive while DMD power is applied.
DMD_LS_CLK	A1	O_3	DMD, low speed interface clock
DMD_LS_WDATA	A2	O_3	DMD, low speed serial write data
DMD_LS_RDATA	B2	I_6	DMD, low speed serial read data

Pin Functions – DMD Sub-LVDS Interface

PIN		I/O	DESCRIPTION
NAME	NUMBER		
DMD_HS_CLK_P DMD_HS_CLK_N	A7 B7	O_4	DMD high speed interface
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	A3 B3 A4 B4 A5 B5 A6 B6 A8 B8 A9 B9 A10 B10 A11 B11	O_4	DMD high speed interface lanes, write data bits: (The true numbering and application of the DMD_HS_DATA pins are software configuration dependent)

Pin Functions – Peripheral Interface(1)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
CMP_OUT	A12	I_6	Successive approximation ADC comparator output (Input). Assumes a successive approximation ADC is implemented with a WPC light sensor and/or a thermistor feeding one input of an external comparator and the other side of the comparator is driven from the ASIC's CMP_PWM pin. Typically pulled-down to ground if this function is not used. (hysteresis buffer)
CMP_PWM	A15	O_1	Successive approximation comparator pulse-duration modulation (output). Supplies a PWM signal to drive the successive approximation ADC comparator used in WPC light-to-voltage sensor applications. Leave unconnected if this function is not used.
HOST_IRQ(2)	N8	O_9	Host interrupt (output) HOST_IRQ indicates when the auto-initialization is in progress and most importantly when it completes. The tri-states this output during reset and assumes that an external pullup is in place to drive this signal to its inactive state.
IIC0_SCL	N10	B_7	I^2C slave (port 0) SCL (bidirectional, open-drain signal with input hysteresis): An external pullup is required. The slave I^2C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^2C pullups must be connected to an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the VIH specification of the slave I^2C input buffers).
Reserved	R11	B_8	TI internal use. TI recommends an external pullup resistor.
IIC0_SDA	N9	B_7	I^2C slave (port 0) SDA. (bidirectional, open-drain signal with input hysteresis): An external pullup is required. The slave I^2C port is the control port of ASIC. The slave I^2C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^2C pullups must be connected to an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the VIH specification of the slave I^2C input buffers).
Reserved	R10	B_8	TI internal use. TI recommends an external pullup resistor.
LED_SEL_0	B15	O_1	LED enable select. Controlled by programmable DMD sequence Timing / LED_SEL(1:0) — Enabled LED / DLPA200x / DLPA300x application 00 — None 01 — Red 10 — Green 11 — Blue
LED_SEL_1	B14	O_1	These signals are driven low when RESETZ is asserted and the corresponding I/O power is supplied and continues throughout the auto-initialization process. A weak, external pulldown resistor is still recommended to ensure that the LEDs are disabled when I/O power is not applied.
SPI0_CLK	A13	O_{13}	Synchronous serial port 0, clock
SPI0_CSZ0	A14	O_{13}	SPI port 1, chip select 0 (active low output) TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during ASIC reset assertion.
SPI0_CSZ1	C12	O_{13}	SPI port 1, chip select 1 (active low output) TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during ASIC reset assertion.
SPI0_DIN	B12	I_{12}	Synchronous serial port 0, receive data in
SPI0_DOUT	B13	O_{13}	Synchronous serial port 0, transmit data out

(1) External pullup resistor must be 8 kΩ or less.
(2) For more information about usage, see *HOST_IRQ Usage Model*.

Pin Functions – GPIO Peripheral Interface(1)

PIN		I/O	DESCRIPTION(2)
NAME	NUMBER		
GPIO_19	M15	B_1	General purpose I/O 19 (hysteresis buffer). Options: 1. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input). 2. MTR_SENSE, Motor Sense (Input): For Focus Motor control applications, this GPIO must be configured as an input to the fed from the focus motor position sensor. 3. KEYPAD_4 (input): keypad applications
GPIO_18	M14	B_1	General purpose I/O 18 (hysteresis buffer). Options: 1. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input) 2. KEYPAD_3 (input): keypad applications
GPIO_17	L15	B_1	General purpose I/O 17 (hysteresis buffer). Options: 1. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input). 2. KEYPAD_2 (input): keypad applications
GPIO_16	L14	B_1	General purpose I/O 16 (hysteresis buffer). Options: 1. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input). 2. KEYPAD_1 (input): keypad applications
GPIO_15	K15	B_1	General purpose I/O 15 (hysteresis buffer). Options: 1. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input). 2. KEYPAD_0 (input): keypad applications
GPIO_14	K14	B_1	General purpose I/O 14 (hysteresis buffer). Options: 1. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_13	J15	B_1	General purpose I/O 13 (hysteresis buffer). Options: 1. CAL_PWR (output): Intended to feed the calibration control of the successive approximation ADC light sensor. 2. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_12	J14	B_1	General purpose I/O 12 (hysteresis buffer). Options: 1. (Output) power enable control for LABB light sensor. 2. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_11	H15	B_1	General purpose I/O 11 (hysteresis buffer). Options: 1. (Output): thermistor power enable. 2. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_10	H14	B_1	General Purpose I/O 10 (hysteresis buffer). Options: 1. RC_CHARGE (output): Intended to feed the RC charge circuit of the successive approximation ADC used to control the light sensor comparator. 2. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_09	G15	B_1	General purpose I/O 09 (hysteresis buffer). Options: 1. LS_PWR (active high output): Intended to feed the power control signal of the successive approximation ADC light sensor. 2. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).

(1) GPIO signals must be configured through software for input, output, bidirectional, or open-drain. Some GPIO have one or more alternative use modes, which are also software configurable. The reset default for all GPIO is as an input signal. An external pullup is required for each signal configured as open-drain.
(2) general purpose I/O. These GPIO are software configurable.

Pin Functions – GPIO Peripheral Interface[(1)] (continued)

PIN		I/O	DESCRIPTION[(2)]
NAME	NUMBER		
GPIO_08	G14	B_1	General purpose I/O 08 (hysteresis buffer). Options: 1. (All) Normal mirror parking request (active low): To be driven by the PROJ_ON output of the host. A logic low on this signal causes the to ASIC to PARK the DMD, but it does not power down the DMD (the DLPA200x or DLPA300x performs that function). The minimum high time is 200 ms. The minimum low time is also 200 ms.
GPIO_07	F15	B_1	General purpose I/O 07 (hysteresis buffer). Options: 1. (Output): LABB output sample and hold sensor control signal. 2. Light Control: Reserved for TRIG_OUT_2 signal (Output). 3. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_06	F14	B_1	General purpose I/O 06 (hysteresis buffer). Option: 1. Light Control: Reserved for pattern ready signal (Output). Applicable in Internal Pattern Streaming Mode only. 2. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_05	E15	B_1	General purpose I/O 05 (hysteresis buffer). Options: 1. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_04	E14	B_1	General purpose I/O 04 (hysteresis buffer). Options: 1. 3D glasses control (output): intended to be used to control the shutters on 3D glasses (Left = 1, Right = 0). 2. SPI1_CSZ1 (active-low output): optional SPI1 chip select 1 signal. An external pullup resistor is required to deactivate this signal during reset and auto-initialization processes. 3. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_03	D15	B_1	General purpose I/O 03 (hysteresis buffer). Options: 1. SPI1_CSZ0 (active low output): Optional SPI1 chip select 0 signal. An external pullup resistor is required to deactivate this signal during reset and auto-initialization processes. 2. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_02	D14	B_1	General purpose I/O 02 (hysteresis buffer). Options: 1. SPI1_DOUT (output): Optional SPI1 data output signal. 2. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_01	C15	B_1	General purpose I/O 01 (hysteresis buffer). Options: 1. SPI1_CLK (output): Optional SPI1 clock signal. 2. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).
GPIO_00	C14	B_1	General purpose I/O 00 (hysteresis buffer). Options: 1. SPI1_DIN (input): Optional SPI1 data input signal. 2. Optional GPIO. Configure as a logic zero GPIO output and leave unconnected if not used (otherwise this pin requires an external pullup or pulldown component to avoid a floating GPIO input).

Pin Functions – Clock and PLL Support

PIN		I/O	DESCRIPTION
NAME	NUMBER		
PLL_REFCLK_I	H1	I_{11}	Reference clock crystal input. If the application uses an external oscillator instead of a crystal, use this pin as the oscillator input.
PLL_REFCLK_O	J1	O_5	Reference clock crystal return. If the application uses an external oscillator instead of a crystal, leave this pin unconnected (floating with no added capacitive load).

Pin Functions – Power and Ground(1)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
VDD	C5, D5, D7, D12, J4, J12, K3, L4, L12, M6, M9, D9, D13, F13, H13, L13, M10, D3, E3	PWR	Core power 1.1 V (main 1.1 V)
VDDLP12	C3	PWR	Reserved
VSS	Common to all package types C4, D6, D8, D10, E4, E13, F4, G4, G12, H4, H12, J3, J13, K4, K12, L3, M4, M5, M8, M12, G13, C6, C8 Only available on F6, F7, F8, F9, F10, G6, G7, G8, G9, G10, H6, H7, H8, H9, H10, J6, J7, J8, J9, J10, K6, K7, K8, K9, K10	GND	Core ground (eDRAM, I/O ground, thermal ground)
VCC18	C7, C9, D4, E12, F12, K13, M11	PWR	All 1.8-V I/O power: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT, and JTAG pins)
VCC_INTF	M3, M7, N3, N7	PWR	Host or parallel interface I/O power: 1.8 to 3.3 V (Includes IIC0, PDATA, video syncs, and HOST_IRQ pins)
VCC_FLSH	D11	PWR	Flash interface I/O power:1.8 to 3.3 V (Dedicated SPI0 power pin)
VDD_PLLM	H2	PWR	MCG PLL 1.1-V power
VSS_PLLM	G3	RTN	MCG PLL return
VDD_PLLD	J2	PWR	DCG PLL 1.1-V power
VSS_PLLD	H3	RTN	DCG PLL return

(1) The only power sequencing restrictions are:
  (a) The VDD supply typically ramps up with a 1-ms minimum rise time.
  (b) The reverse is needed at power down.

Table 1. I/O Type Subscript Definition

I/O		SUPPLY REFERENCE	ESD STRUCTURE
SUBSCRIPT	DESCRIPTION		
1	1.8 LVCMOS I/O buffer with 8-mA drive	V_{cc18}	ESD diode to GND and supply rail
2	1.8 LVCMOS I/O buffer with 4-mA drive	V_{cc18}	ESD diode to GND and supply rail
3	1.8 LVCMOS I/O buffer with 24-mA drive	V_{cc18}	ESD diode to GND and supply rail
4	1.8 sub-LVDS output with 4-mA drive	V_{cc18}	ESD diode to GND and supply rail
5	1.8, 2.5, 3.3 LVCMOS with 4-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
6	1.8 LVCMOS input	V_{cc18}	ESD diode to GND and supply rail
7	1.8-, 2.5-, 3.3-V I^2C with 3-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
8	1.8-V I^2C with 3-mA drive	V_{cc18}	ESD diode to GND and supply rail
9	1.8-, 2.5-, 3.3-V LVCMOS with 8-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
11	1.8, 2.5, 3.3 LVCMOS input	V_{cc_INTF}	ESD diode to GND and supply rail
12	1.8-, 2.5-, 3.3-V LVCMOS input	V_{cc_FLSH}	ESD diode to GND and supply rail
13	1.8-, 2.5-, 3.3-V LVCMOS with 8-mA drive	V_{cc_FLSH}	ESD diode to GND and supply rail

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
SUPPLY VOLTAGE(2)(3)				
$V_{(VDD)}$ (core)		–0.3	1.21	V
$V_{(VDDLP12)}$ (core)		–0.3	1.32	V
Power + sub-LVDS		–0.3	1.96	V
$V_{(VCC\_INTF)}$	Host I/O power	–0.3	3.60	V
	If 1.8-V power used	–0.3	1.99	
	If 2.5-V power used	–0.3	2.75	
	If 3.3-V power used	–0.3	3.60	
$V_{(VCC\_FLSH)}$	Flash I/O power	–0.3	3.60	V
	If 1.8-V power used	–0.3	1.96	
	If 2.5-V power used	–0.3	2.72	
	If 3.3-V power used	–0.3	3.58	
$V_{(VDD\_PLLM)}$ (MCG PLL)		–0.3	1.21	V
$V_{(VDD\_PLLD)}$ (1DCG PLL)		–0.3	1.21	V
GENERAL				
T_J	Operating junction temperature	–30	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Overlap currents, if allowed to continue flowing unchecked, not only increase total power dissipation in a circuit, but degrade the circuit reliability, thus shortening its usual operating life.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$(1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(3)	±500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(VDD)}$	Core power 1.1 V (main 1.1 V)	±5% tolerance	1.045	1.1	1.155	V
$V_{(VDDLP12)}$	Reserved	±5% tolerance See (1) (2)	1.045	1.10	1.155	V
$V_{(VCC18)}$	All 1.8-V I/O power: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT, and JTAG pins.)	±8.5% tolerance	1.64	1.8	1.96	V
$V_{(VCC\_INTF)}$	Host or parallel interface I/O power: 1.8 to 3.3 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)	±8.5% tolerance See (3)	1.64	1.8	1.96	V
			2.28	2.5	2.72	
			3.02	3.3	3.58	
$V_{(VCC\_FLSH)}$	Flash interface I/O power:1.8 to 3.3 V	±8.5% tolerance See (3)	1.64	1.8	1.96	V
			2.28	2.5	2.72	
			3.02	3.3	3.58	
$V_{(VDD\_PLLM)}$	MCG PLL 1.1-V power	±9.1% tolerance See (4)	1.025	1.1	1.155	V
$V_{(VDD\_PLLD)}$	DCG PLL 1.1-V power	±9.1% tolerance See (4)	1.025	1.1	1.155	V
T_A	Operating ambient temperature range (5)		–30		85	°C
T_J	Operating junction temperature		–30		105	°C

(1) It is recommended that VDDLP12 rail is tied to the VDD rail.
(2) If the VDDLP12 is fed from a separate (from VDD) supply, the VDDLP12 power must sequence ON after the 1.1V core supply and must sequence OFF before the 1.1V core supply.
(3) These supplies have multiple valid ranges.
(4) These I/O supply ranges are wider to facilitate additional filtering.
(5) The operating ambient temperature range assumes 0 forced air flow, a JEDEC JESD51 junction-to-ambient thermal resistance value at 0 forced air flow ($R_{\theta JA}$ at 0 m/s), a JEDEC JESD51 standard test card and environment, along with min and max estimated power dissipation across process, voltage, and temperature. Thermal conditions vary by application, which affects the value of $R_{\theta JA}$. Thus, maximum operating ambient temperature varies by application.
(a) $T_{a\_min} = T_{j\_min} – (P_{d\_min} \times R_{\theta JA})$ = –30°C – (0.0W × 30.3°C/W) = –30°C
(b) $T_{a\_max} = T_{j\_max} – (P_{d\_max} \times R_{\theta JA})$ = +105°C – (0.348W × 30.3°C/W) = +94.4°C

6.4 Thermal Information

THERMAL METRIC (1)			DLPC3478 ZEZ (NFBGA) 201 PINS	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance		10.1	°C/W
$R_{\theta JA}$	Junction-to-air thermal resistance	at 0 m/s of forced airflow (2)	28.8	°C/W
		at 1 m/s of forced airflow (2)	25.3	°C/W
		at 2 m/s of forced airflow (2)	24.4	°C/W
ψ_{JT} (3)	Temperature variance from junction to package top center temperature, per unit power dissipation		.23	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal coefficients abide by JEDEC Standard 51. $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC3478 PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different , it is the best information available during the design phase to estimate thermal performance.
(3) Example: (0.5 W) × (0.2 C/W) ≈ 1.00°C temperature rise.

6.5 Electrical Characteristics over Recommended Operating Conditions (1)(2)(3)(4)

PARAMETER		TEST CONDITIONS(5)(6)	MIN	TYP(7)	MAX(8)	UNIT
$V_{(VDD)}$ + $V_{(VDDLP12)}$	Core current 1.1 V (main 1.1 V)	IDLE disabled, 720p, 60 Hz		161	334	mA
		IDLE disabled, 720p, 120 Hz		185	368	
$V_{(VDD\_PLLM)}$	MCG PLL 1.1 V current	IDLE disabled, 720p, 60 Hz		4	7	mA
		IDLE disabled, 720p, 120 Hz		4	7	
$V_{(VDD\_PLLD)}$	DCG PLL 1.1 V current	IDLE disabled, 720p, 60 Hz		4	7	mA
		IDLE disabled, 720p, 120 Hz		4	7	
V(VDD) + V(VDD_PLLM) + V(VDD_PLLD)	Core Current 1.1 V + MCG PLL 1.1 V current + DCG PLL 1.1 V current	IDLE disabled, 720p, 60 Hz		169	348	mA
		IDLE disabled, 720p, 120 Hz		193	382	
$V_{(VCC18)}$	Main 1.8 V I/O current: 1.8 V power supply for all I/O other than the host or parallel interface and the SPI flash interface.	IDLE disabled, 720p, 60 Hz		13	18	mA
	This includes sub-LVDS DMD I/O , RESETZ, PARKZ, LED_SEL, CMP, GPIO, IIC1, TSTPT and JTAG pins	IDLE disabled, 720p, 120 Hz		13	18	
$V_{(VCC\_INTF)}$	Host or parallel interface I/O current: 1.8 to 3.3 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)	IDLE disabled, 720p, 60 Hz		2	3	mA
		IDLE disabled, 720p, 120 Hz		4	6	
$V_{(VCC\_FLSH)}$	Flash interface I/O current: 1.8 to 3.3 V	IDLE disabled, 720p, 60 Hz		1	1.5	mA
		IDLE disabled, 720p, 120 Hz		1	1.5	
$V_{(VCC18)}$ + $V_{(VCC\_INTF)}$ + $V_{(VCC\_FLSH)}$	Main 1.8 V I/O current + VCC_INTF current + VCC_FLSH current	IDLE disabled, 720p, 60 Hz		16	22.5	mA
		IDLE disabled, 720p, 120 Hz		18	25.5	

(1) Assumes 12.5% activity factor, 30% clock gating on appropriate domains, and mixed SVT or HVT cells
(2) Programmable host and flash I/O are at minimum voltage (that is 1.8 V) for this typical scenario.
(3) Max currents column use typical motion video as the input. The typical currents column uses SMPTE color bars as the input.
(4) Some applications (that is, high-resolution 3D) may be forced to use 1-oz copper to manage ASIC package heat.
(5) Input image is 1280 × 720 (720p) 24-bits on the parallel interface at the frame rate shown with a 0.3-inch 720p DMD.
(6) In normal operation while displaying an image with CAIC enabled.
(7) Assumes typical case power PVT condition = nominal process, typical voltage, typical temperature (55°C junction). 720p resolution.
(8) Assumes worse case power PVT condition = corner process, high voltage, high temperature (105°C junction), 720p resolution.

6.6 Electrical Characteristics(1)(2)

over operating free-air temperature range (unless otherwise noted)

PARAMETER(3)			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	I2C buffer (I/O type 7)		0.7 × VCC_INTF		(1)	V
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		1.17		3.6	
		1.8-V LVTTL (I/O type 1, 6) identified below: (2) CMP_OUT; PARKZ; RESETZ; GPIO 0 →19		1.3		3.6	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		1.7		3.6	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		2		3.6	
V_{IL}	Low-level input threshold voltage	I2C buffer (I/O type 7)		–0.5		0.3 × VCC_INTF	V
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		–0.3		0.63	
		1.8-V LVTTL (I/O type 1, 6) identified below: (2) CMP_OUT; PARKZ; RESETZ; GPIO_00 through GPIO_19		–0.3		0.5	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		–0.3		0.7	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		–0.3		0.8	
V_{CM}	Steady-state common mode voltage	1.8 sub-LVDS (DMD high speed) (I/O type 4)		0.8	0.9	1	mV
$\|V_{OD}\|$	Differential output magnitude	1.8 sub-LVDS (DMD high speed) (I/O type 4)			200		mV
V_{OH}	High-level output voltage	1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		1.35			V
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		1.7			
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		2.4			
		1.8 sub-LVDS – DMD high speed (I/O type 4)			1		
V_{OL}	Low-level output voltage	I2C buffer (I/O type 7)	VCC_INTF > 2 V			0.4	V
		I2C buffer (I/O type 7)	VCC_INTF < 2 V			0.2 × VCC_INTF	
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)				0.45	
		2.5 V LVTTL (I/O type 5, 9, 11, 12, 13)				0.7	
		3.3 V LVTTL (I/O type 5, 9, 11, 12, 13)				0.4	
		1.8 sub-LVDS – DMD high speed (I/O type 4)			0.8		

(1) I/O is high voltage tolerant; that is, if VCC = 1.8 V, the input is 3.3-V tolerant, and if VCC = 3.3 V, the input is 5-V tolerant.
(2) ASIC pins: CMP_OUT; PARKZ; RESETZ; GPIO_00 through GPIO_19 have slightly varied V_{IH} and V_{IL} range from other 1.8-V I/O.
(3) The number inside each parenthesis for the I/O refers to the type defined in Table 1.

Electrical Characteristics[1][2] (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER[3]			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	High-level output current	1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	4 mA	2			mA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	8 mA	3.5			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	24 mA	10.6			
		2.5-V LVTTL (I/O type 5)	4 mA	5.4			
		2.5-V LVTTL (I/O type 9, 13)	8 mA	10.8			
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)	24 mA	28.7			
		3.3-V LVTTL (I/O type 5)	4 mA	7.8			
		3.3-V LVTTL (I/O type 9, 13)	8 mA	15			
I_{OL}	Low-level output current	I^2C buffer (I/O type 7)		3			mA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	4 mA	2.3			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	8 mA	4.6			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	24 mA	13.9			
		2.5-V LVTTL (I/O type 5)	4 mA	5.2			
		2.5-V LVTTL (I/O type 9, 13)	8 mA	10.4			
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)	24 mA	31.1			
		3.3-V LVTTL (I/O type 5)	4 mA	4.4			
		3.3-V LVTTL (I/O type 9, 13)	8 mA	8.9			
I_{OZ}	High-impedance leakage current	I^2C buffer (I/O type 7)	0.1 × VCC_INTF < VI < 0.9 × VCC_INTF	–10		10	µA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		–10		10	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		–10		10	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		–10		10	
C_I	Input capacitance (including package)	I^2C buffer (I/O type 7)				5	pF
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		2.6		3.5	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		2.6		3.5	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		2.6		3.5	
		1.8 sub-LVDS – DMD high speed (I/O type 4)				3	

Table 2. Internal Pullup and Pulldown Characteristics(1)(2)

INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS	VCCIO	MIN	MAX	UNIT
Weak pullup resistance	3.3 V	29	63	kΩ
	2.5 V	38	90	kΩ
	1.8 V	56	148	kΩ
Weak pulldown resistance	3.3 V	30	72	kΩ
	2.5 V	36	101	kΩ
	1.8 V	52	167	kΩ

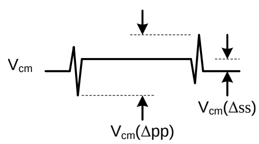
(1) The resistance is dependent on the supply voltage level applied to the I/O.
(2) An external 8-kΩ pullup or pulldown (if needed) would work for any voltage condition to correctly pull enough to override any associated internal pullups or pulldowns.

6.7 High-Speed Sub-LVDS Electrical Characteristics

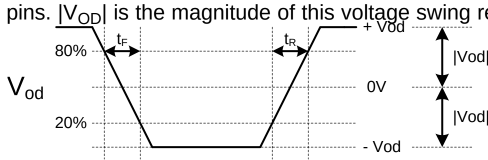
over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{CM}	Steady-state common mode voltage	0.8	0.9	1.0	V
V_{CM} (Δpp)(1)	V_{CM} change peak-to-peak (during switching)			75	mV
V_{CM} (Δss)(1)	V_{CM} change steady state	–10		10	mV
$\|V_{OD}\|$(2)	Differential output voltage magnitude		200		mV
V_{OD} (Δ)	V_{OD} change (between logic states)	–10		10	mV
V_{OH}	Single-ended output voltage high		1.00		V
V_{OL}	Single-ended output voltage low		0.80		V
t_R(2)	Differential output rise time			250	ps
t_F(2)	Differential output fall time			250	ps
t_{MAX}	Max switching rate			1200	Mbps
DCout	Output duty cycle	45%	50%	55%	
Tx_{term}(1)	Internal differential termination	80	100	120	Ω
Tx_{load}	100-Ω differential PCB trace (50-Ω transmission lines)	0.5		6	inches

(1) Definition of V_{CM} changes:



(2) Note that V_{OD} is the differential voltage swing measured across a 100-Ω termination resistance connected directly between the transmitter differential pins. $|V_{OD}|$ is the magnitude of this voltage swing relative to 0. Rise and fall times are defined for the differential V_{OD} signal as follows:



Differential Output Signal
(Note Vcm is removed when the signals are viewed differentially)

6.8 Low-Speed SDR Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	ID	TEST CONDITIONS	MIN	MAX	UNIT
Operating voltage	VCC18 (all signal groups)		1.64	1.96	V
DC input high voltage	VIHD(DC) Signal group 1	All	0.7 × VCC18	VCC18 + 0.5	V
DC input low voltage(1)	VILD(DC) Signal group 1	All	–0.50	0.3 × VCC18	V
AC input high voltage(2)	VIHD(AC) Signal group 1	All	0.8 × VCC18	VCC18 + 0.5	V
AC input low voltage	VILD(AC) Signal group 1	All	–0.5	0.2 × VCC18	V
Slew rate (3)(4)(5)(6)	Signal group 1		1	3.0	V/ns
	Signal group 2		0.25		
	Signal group 3		0.5		

(1) VILD(AC) min applies to undershoot.
(2) VIHD(AC) max applies to overshoot.
(3) Signal group 1 output slew rate for rising edge is measured between VILD(DC) to VIHD(AC).
(4) Signal group 1 output slew rate for falling edge is measured between VIHD(DC) to VILD(AC).
(5) Signal group 1: See Figure 1.
(6) Signal groups 2 and 3 output slew rate for rising edge is measured between VILD(AC) to VIHD(AC).

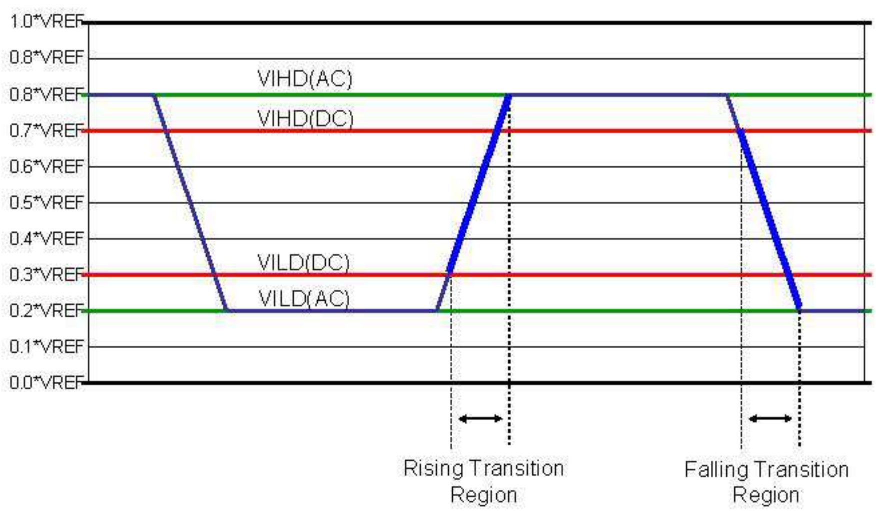


Figure 1. Low Speed (LS) I/O Input Thresholds

6.9 System Oscillators Timing Requirements(1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, MOSC(2)	24-MHz oscillator	23.998	24.002	MHz
t_c	Cycle time, MOSC(2)	24-MHz oscillator	41.670	41.663	ns
$t_{w(H)}$	Pulse duration(3), MOSC, high	50% to 50% reference points (signal)		40 t_c%	
$t_{w(L)}$	Pulse duration(3), MOSC, low	50% to 50% reference points (signal)		40 t_c%	
t_t	Transition time(3), MOSC, $t_t = t_f / t_r$	20% to 80% reference points (signal)		10	ns
t_{jp}	Long-term, peak-to-peak, period jitter(3), MOSC (that is the deviation in period from ideal period due solely to high frequency jitter)			2%	

(1) The I/O pin TSTPT_6 must be left open for 24 MHz timing to work properly inside the DLPC3478.
(2) The frequency accuracy for MOSC is ±200 PPM. (This includes impact to accuracy due to aging, temperature, and trim sensitivity.) The MOSC input cannot support spread spectrum clock spreading.
(3) Applies only when driven through an external digital oscillator.

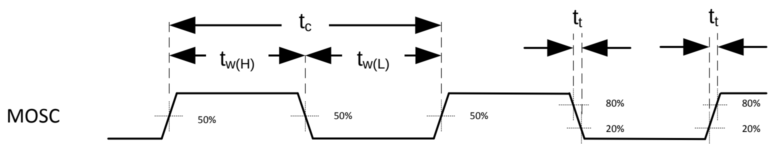


Figure 2. System Oscillators

6.10 Power-Up and Reset Timing Requirements

NUMBER				MIN	MAX	UNIT
1	$t_{w(L)}$	Pulse duration, inactive low, RESETZ	50% to 50% reference points (signal)	1.25		µs
2	t_t	Transition time, RESETZ(1), $t_t = t_f / t_r$	20% to 80% reference points (signal)		0.5	µs

(1) For more information on RESETZ, see *Pin Configuration and Functions*.

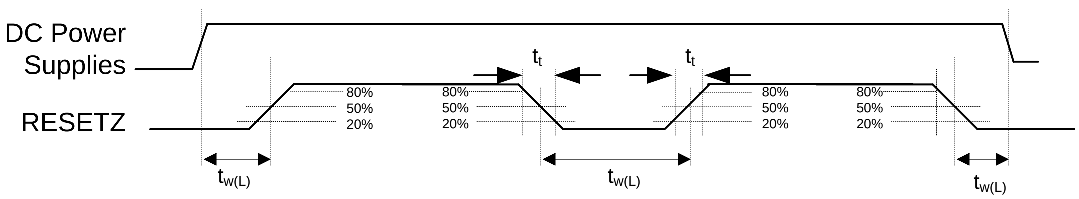


Figure 3. Power-Up and Power-Down RESETZ Timing

6.11 Parallel Interface Frame Timing Requirements

			MIN	MAX	UNIT
t_{p_vsw}	Pulse duration – VSYNC_WE high	50% reference points	1		lines
t_{p_vbp}	Vertical back porch (VBP) – time from the leading edge of VSYNC_WE to the leading edge HSYNC_CS for the first active line (see (1))	50% reference points	2		lines
t_{p_vfp}	Vertical front porch (VFP) – time from the leading edge of the HSYNC_CS following the last active line in a frame to the leading edge of VSYNC_WE (see (1))	50% reference points	1		lines
t_{p_tvb}	Total vertical blanking – time from the leading edge of HSYNC_CS following the last active line of one frame to the leading edge of HSYNC_CS for the first active line in the next frame. (This is equal to the sum of VBP (t_{p_vbp}) + VFP (t_{p_vfp}).)	50% reference points	See (1)		lines
t_{p_hsw}	Pulse duration – HSYNC_CS high	50% reference points	4	128	PCLKs
t_{p_hbp}	Horizontal back porch – time from rising edge of HSYNC_CS to rising edge of DATAEN_CMD	50% reference points	4		PCLKs
t_{p_hfp}	Horizontal front porch – time from falling edge of DATAEN_CMD to rising edge of HSYNC_CS	50% reference points	8		PCLKs
t_{p_thb}	Total horizontal blanking – sum of horizontal front and back porches	50% reference points	See (2)		PCLKs

(1) The minimum total vertical blanking is defined by the following equation: $t_{p\_tvb}(min) = 6 + [8 \times Max(1, Source\_ALPF/ DMD\_ALPF)]$ lines where:
(a) SOURCE_ALPF = Input source active lines per frame
(b) DMD_ALPF = Actual DMD used lines per frame supported

(2) The maximum line rate for a given source (which is a function of resolution and orientation) drives total horizontal blanking. Use this equation: $t_{p\_thb} = Roundup[(1000 \times f_{clock})/ LR] – APPL$
where:
(a) f_{clock} = Pixel clock rate in MHz
(b) LR = Line rate in kHz
(c) APPL is the number of active pixels per (horizontal) line.
(d) If t_{p_thb} is calculated to be less than $t_{p\_hbp} + t_{p\_hfp}$ then the pixel clock rate is too low or the line rate is too high, and one or both must be adjusted.

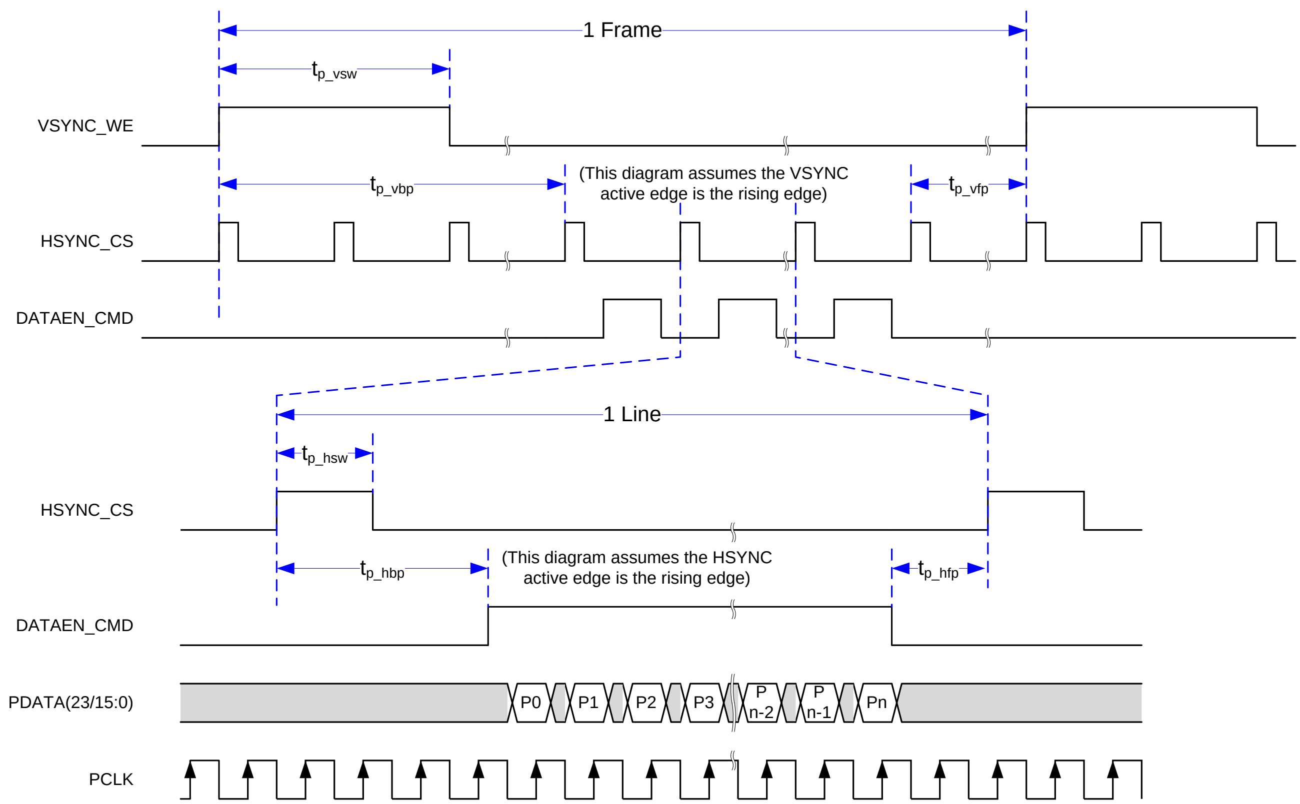


Figure 4. Parallel Interface Frame Timing

6.12 Parallel Interface General Timing Requirements(1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1.0	150.0	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	6.66	1000	ns
t_{p_clkjit}	Clock jitter, PCLK	Max f_{clock}	see (2)	see (2)	
t_{p_wh}	Pulse duration low, PCLK	50% reference points	2.43		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	2.43		ns
t_{p_su}	Setup time – HSYNC_CS, DATEN_CMD, PDATA(23:0) valid before the active edge of PCLK	50% reference points	0.9		ns
t_{p_h}	Hold time – HSYNC_CS, DATEN_CMD, PDATA(23:0) valid after the active edge of PCLK	50% reference points	0.9		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	2.0	ns

(1) The active (capture) edge of PCLK for HSYNC_CS, DATEN_CMD and PDATA(23:0) is software programmable, but defaults to the rising edge.
(2) Clock jitter (in ns) calculation: Jitter = [1 / f_{clock} – 5.76 ns]. Setup and hold times must be met during clock jitter.

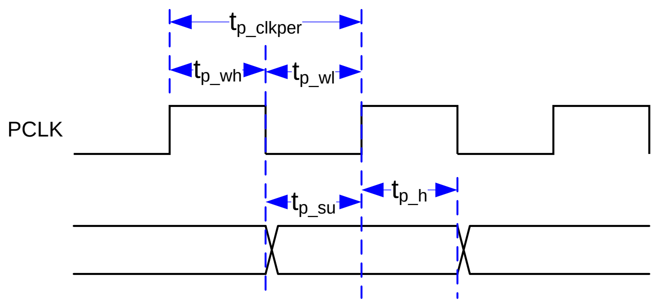


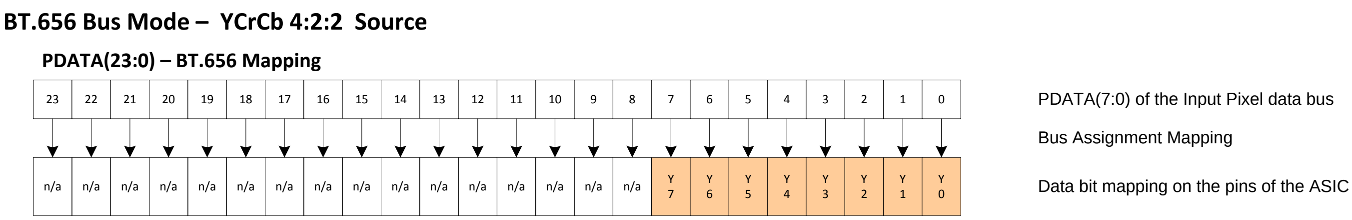
Figure 5. Parallel Interface General Timing

6.13 BT656 Interface General Timing Requirements(1)

The DLPC3478 ASIC input interface supports the industry standard BT.656 parallel video interface. See the appropriate ITU-R BT.656 specification for detailed interface timing requirements.

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1.0	33.5	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	29.85	1,000	ns
t_{p_clkjit}	Clock jitter, PCLK	Max f_{clock}	See (2)	See (2)	
t_{p_wh}	Pulse duration low, PCLK	50% reference points	10.0		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	10.0		ns
t_{p_su}	Setup time – PDATA(7:0) before the active edge of PCLK	50% reference points	3.0		ns
t_{p_h}	Hold time – PDATA(7:0) after the active edge of PCLK	50% reference points	0.9		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	3.0	ns

(1) The BT.656 interface accepts 8-bits per color, 4:2:2 YCb/Cr data encoded per the industry standard through PDATA(7:0) on the active edge of PCLK (that is programmable). See Figure 6.
(2) Clock jitter calculation: Jitter = [1 / f_{clock} – 5.76 ns]. Setup and hold times must be met during clock jitter.



A. BT.656 data bits map to the DLPC3478 PDATA bus as shown.

Figure 6. DLPC3478 PDATA Bus – BT.656 Interface Mode Bit Mapping

6.14 Flash Interface Timing Requirements(1)(2)

The DLPC3478 ASIC flash memory interface consists of a SPI flash serial interface with a programmable clock rate. The DLPC3478 can support 1- to 16-Mb flash memories.

			MIN	MAX	UNIT
f_{clock}	Clock frequency, SPI_CLK	See (3)	1.42	36.0	MHz
t_{p_clkper}	Clock period, SPI_CLK	50% reference points	704	27.7	ns
t_{p_wh}	Pulse duration low, SPI_CLK	50% reference points	352		ns
t_{p_wl}	Pulse duration high, SPI_CLK	50% reference points	352		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	3.0	ns
t_{p_su}	Setup time – SPI_DIN valid before SPI_CLK falling edge	50% reference points	10.0		ns
t_{p_h}	Hold time – SPI_DIN valid after SPI_CLK falling edge	50% reference points	0.0		ns
t_{p_clqv}	SPI_CLK clock falling edge to output valid time – SPI_DOUT and SPI_CSZ	50% reference points		1.0	ns
t_{p_clqx}	SPI_CLK clock falling edge output hold time – SPI_DOUT and SPI_CSZ	50% reference points	–3.0	3.0	ns

(1) Standard SPI protocol is to transmit data on the falling edge of SPI_CLK and capture data on the rising edge. The DLPC3478 does transmit data on the falling edge, but it also captures data on the falling edge rather than the rising edge. This provides support for SPI devices with long clock-to-Q timing. DLPC3478 hold capture timing has been set to facilitate reliable operation with standard external SPI protocol devices.
(2) With the above output timing, DLPC3478 provides the external SPI device 8.2-ns input set-up and 8.2-ns input hold, relative to the rising edge of SPI_CLK.
(3) This range includes the 200 ppm of the external oscillator (but no jitter).

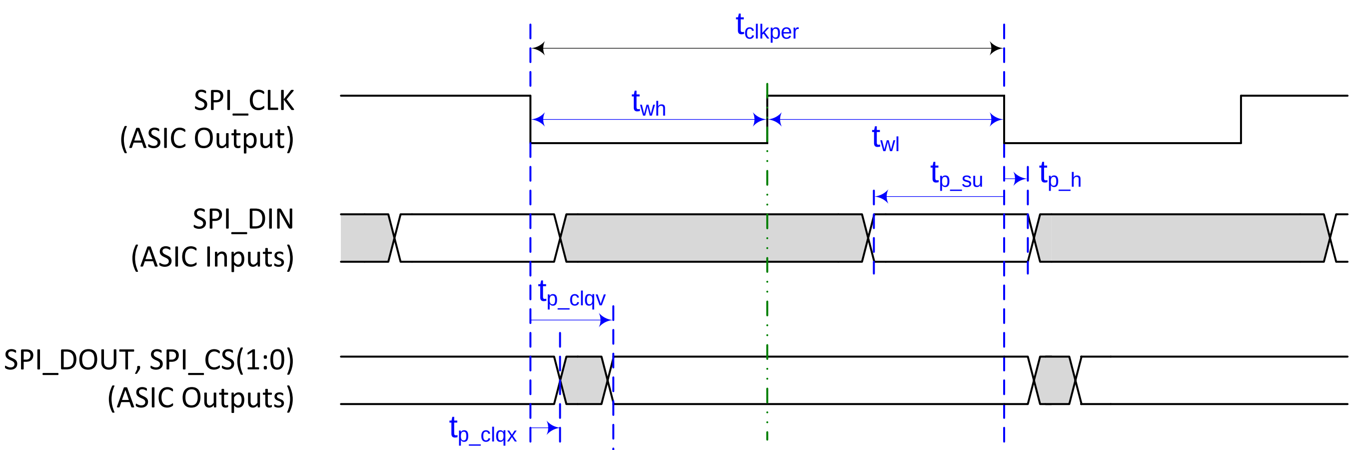
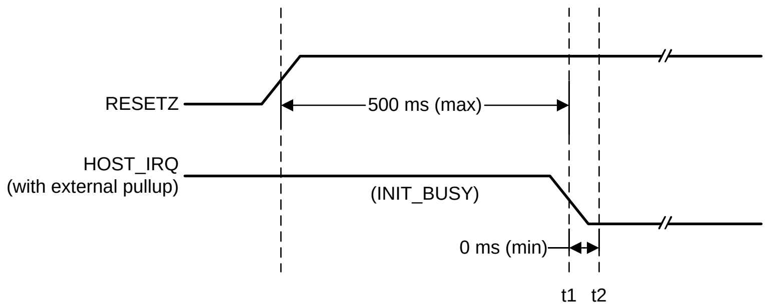


Figure 7. Flash Interface Timing

7 Parameter Measurement Information

7.1 HOST_IRQ Usage Model

- While reset is applied, HOST_IRQ resets to tri-state (an external pullup pulls the line high).
- HOST_IRQ remains in tri-state (pulled high externally) until the microprocessor boot completes. While the signal is pulled high, this indicates that the ASIC is performing boot-up and auto-initialization.
- As soon as possible after boot-up, the microprocessor drives HOST_IRQ to a logic-high state to indicate that the ASIC is continuing to perform auto-initialization (no real state change occurs on the external signal)
- Upon completion of auto-initialization, software sets HOST_IRQ to a logic low state to indicate the completion of auto-initialization. (At the falling edge, the system enters the INIT_DONE state.)
- The 500-ms maximum period from the rising edge of RESETZ to the falling edge of HOST_IRQ may become longer than 500 ms if many commands are added to the autoinit batch file in flash which automatically runs at power up.



t1 is the first falling edge of HOST_IRQ, At this point the auto-initiation sequence is complete.

t2 is where HOST_IRQ goes low. Ensure that I²C interface to the device does not begin until this point (within 500 ms of the release of RESETZ)

Figure 8. Host IRQ Timing

7.2 Input Source

Table 3. Supported Input Source Ranges[(1)(2)(3)(4)]

INTERFACE	BITS / PIXEL [(5)]	IMAGE TYPE	SOURCE RESOLUTION RANGE [(6)]				FRAME RATE RANGE
			HORIZONTAL		VERTICAL		
			Landscape	Portrait	Landscape	Portrait	
Parallel	24 max	2D only	320 to 1280	200 to 800	200 to 800	320 to 1280	10 to 122 Hz
Parallel	24 max	3D only	320 to 1280	200 to 720	200 to 720	320 to 1280	98 to 102 Hz 118 to 122 Hz
BT.656-NTSC [(7)]	See [(8)]	2D only	720	n/a	240	n/a	60 ±2 Hz
BT.656-PAL [(7)]	See [(8)]	2D only	720	n/a	288	n/a	50 ±2 Hz

(1) The user must stay within specifications for all source interface parameters such as max clock rate and max line rate.
(2) The max DMD size for all rows in the table is 1280 × 720.
(3) To achieve the ranges stated, the composer-created firmware used must be defined to support the source parameters used.
(4) These interfaces are supported with the DMD sequencer sync mode command (3Bh) set to auto.
(5) Bits / Pixel does not necessarily equal the number of data pins used on the DLPC3478. Fewer pins are used if multiple clocks are used per pixel transfer.
(6) By using an I^2C command, portrait image inputs can be rotated on the DMD by minus 90 degrees so that the image is displayed in landscape format.
(7) All parameters in this row follow the BT.656 standard. The image format is always landscape.
(8) BT.656 uses 16-bit 4:2:2 YCr/Cb.

7.2.1 Input Source - Frame Rates and 3-D Display Orientation

For 3D sources on the parallel interface, images must be frame sequential (L, R, L, ...) when input to the DLPC3478. Any processing required to unpack 3D images and to convert them to frame sequential must be done by external electronics prior to inputting the images to the DLPC3478. Each 3D source frame input must contain a single eye frame of data separated by a VSYNC where an eye frame contains image data for a single left or right eye. The signal 3DR input to the DLPC3478 tells whether the input frame is for the left eye or right eye.

Each DMD frame displays at the same rate as the input interface frame rate. Typical timing for a 50-Hz or 60-Hz 3D HDMI source frame, the input interface of the DLPC3478, and the DMD is shown in Figure 9. GPIO_04 is optionally sent to a transmitter on the system PCB for wirelessly transmitting a sync signal to 3D glasses. The glasses are then in phase with the DMD images being displayed. Alternately, *3-D Glasses Operation* shows how DLP Link pulses can be used instead.

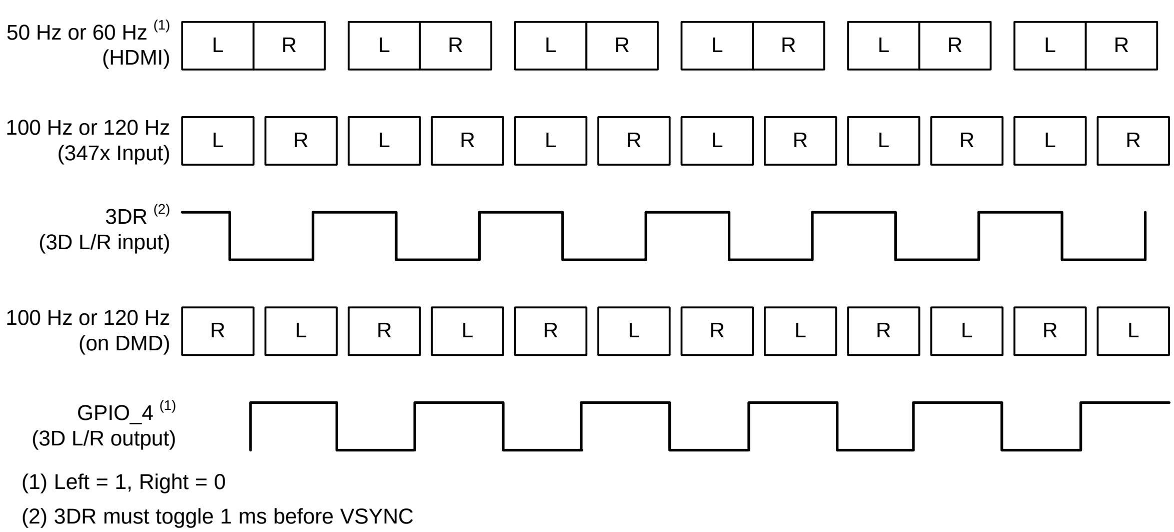


Figure 9. DLPC3478 L/R Frame and Signal Timing

7.2.2 Parallel Interface Supports Six Data Transfer Formats

- 24-bit RGB888 or 24-bit YCrCb888 on a 24 data wire interface

- 18-bit RGB666 or 18-bit YCrCb666 on a 18 data wire interface
- 16-bit RGB565 or 16-bit YCrCb565 on a 16 data wire interface
- 16-bit YCrCb 4:2:2 (standard sampling assumed to be Y0Cb0, Y1Cr0, Y2Cb2, Y3Cr2, Y4Cb4, Y5Cr4, …)
- 8-bit RGB888 or 8-bit YCrCb888 serial (1 color per clock input; 3 clocks per displayed pixel)
  – On an 8 wire interface
- 8-bit YCrCb 4:2:2 serial (1 color per clock input; 2 clocks per displayed pixel)
  – On an 8 wire interface

PDATA Bus – Parallel Interface Bit Mapping Modes shows the required PDATA(23:0) bus mapping for these six data transfer formats.

7.2.2.1 PDATA Bus – Parallel Interface Bit Mapping Modes

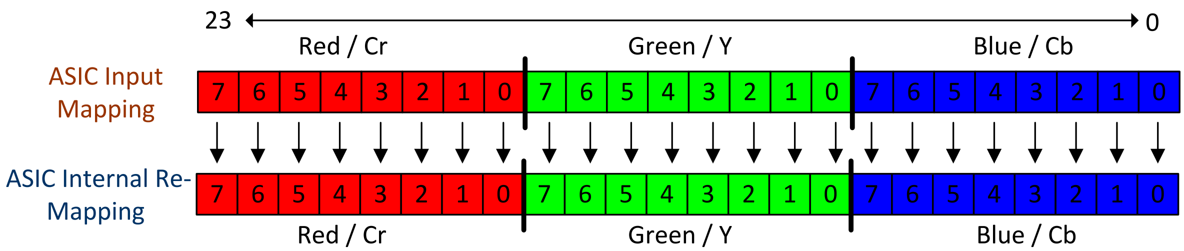


Figure 10. RGB-888 / YCrCb-888 I/O Mapping

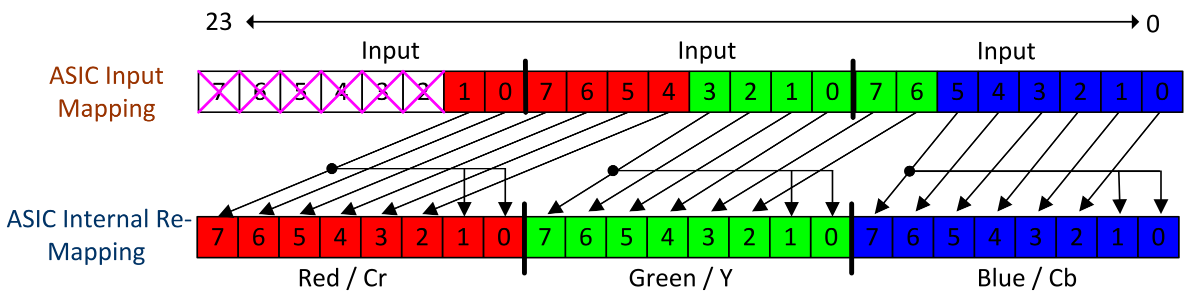


Figure 11. RGB-666 / YCrCb-666 I/O Mapping

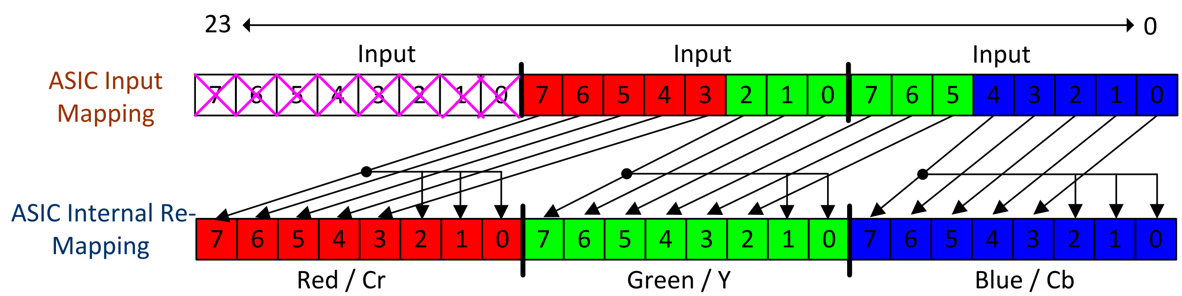


Figure 12. RGB-565 / YCrCb-565 I/O Mapping

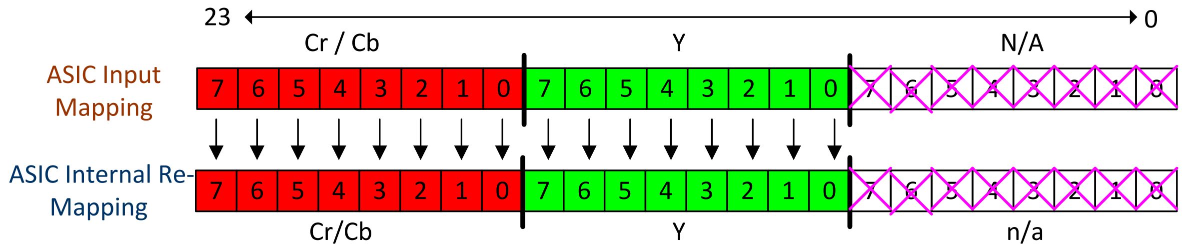


Figure 13. 16-Bit YCrCb-880 I/O Mapping

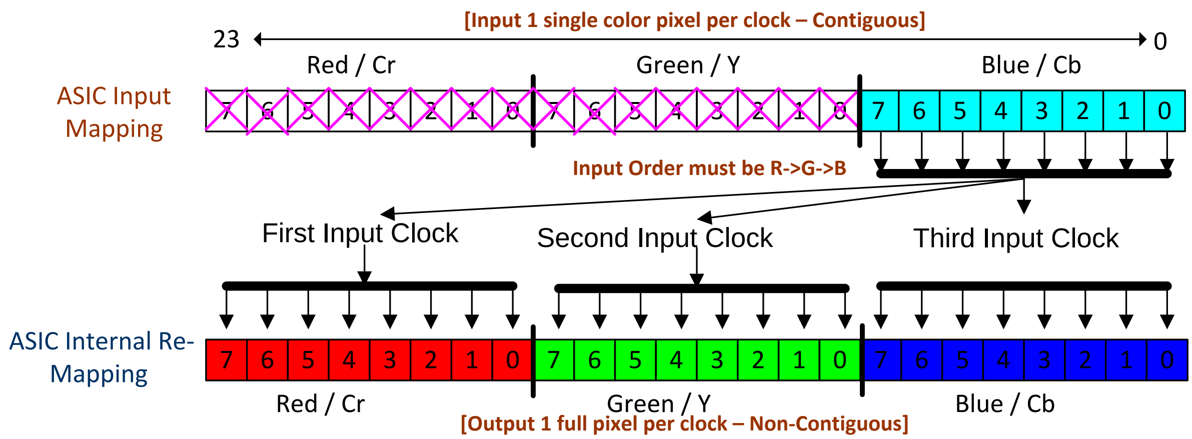


Figure 14. 8-Bit RGB-888 or YCrCb-888 I/O Mapping

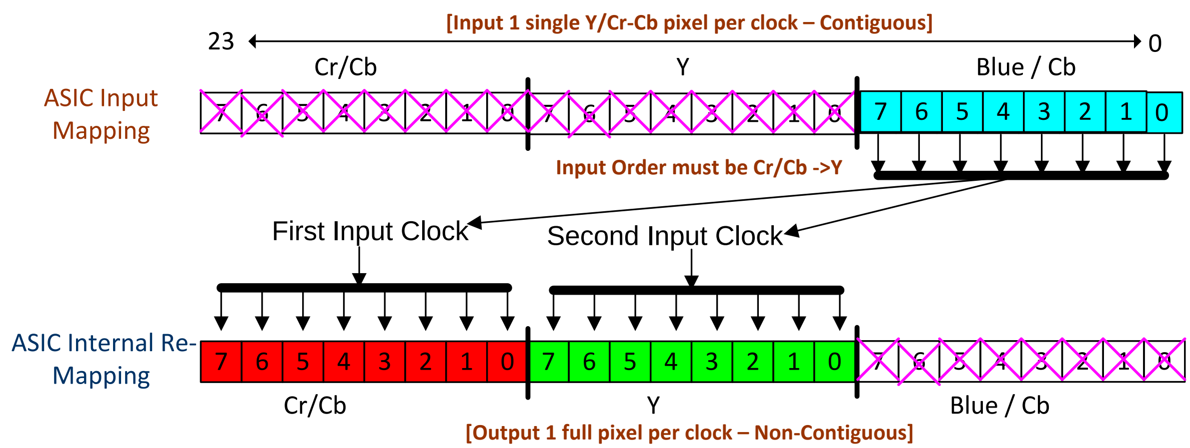


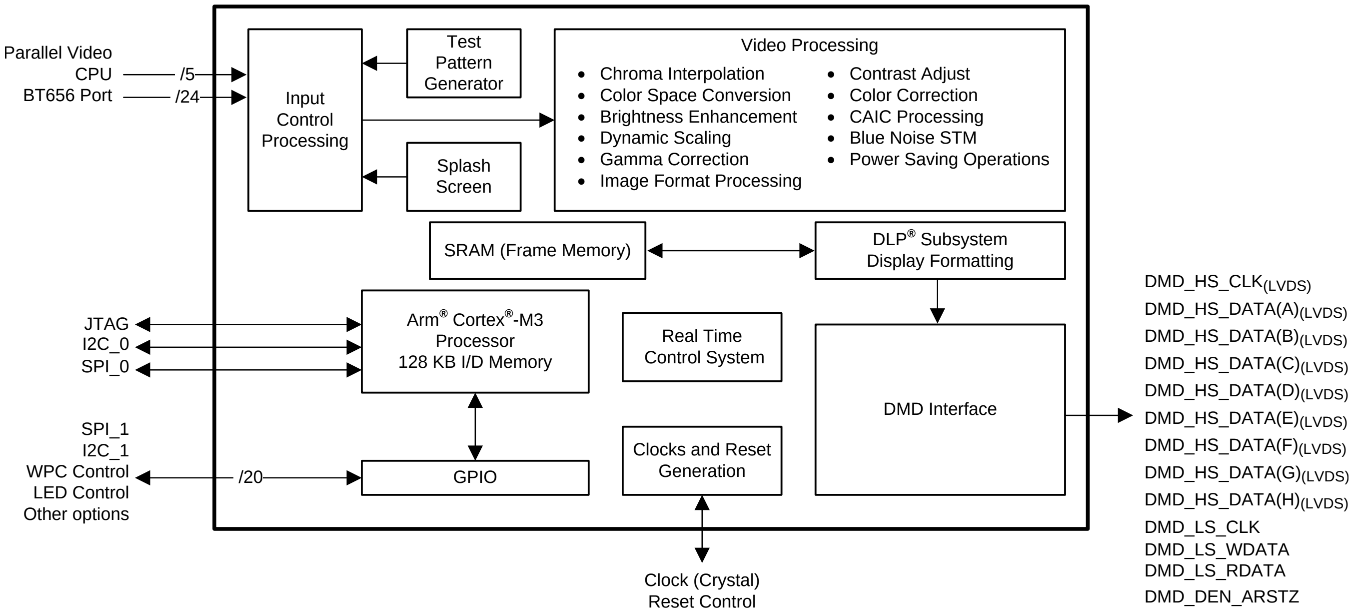
Figure 15. 8-Bit Serial YCrCb-422 I/O Mapping

8 Detailed Description

8.1 Overview

The DLPC3478 controller is one component of a device set that comprises of the DLPC3478 controller, the DLP3010 (.3 720p) DMD, and the DLPA200x or DLPA300x PMIC/LED driver. All three components of the device set must be used together for reliable operation of the DLP3010 (.3 720p) DMD. The DLPC3478 controller provides a convenient interface between user electronics and the DMD to display data and steer light patterns with high speed, precision, and efficiency.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Pattern Display

Pattern display is one of the key capabilities of the DLPC3478 display and light controller. When the DLPC3478 controller is configured for pattern display, video processing functions can be bypassed to allow for accurate pattern display. For user flexibility and simple system design the DLPC3478 controller supports both external pattern and internal pattern streaming modes. In external pattern streaming mode, patterns are sent to the DLPC3478 controller over parallel interface. In internal pattern streaming mode, 1D patterns are pre-loaded in flash memory and a host command is sent to DLPC3478 controller to display the patterns. Internal pattern mode allows for a simple system design by eliminating the need for any external processor to generate and sent 1D patterns to the DLPC3478 controller.

The DLPC3478 controller outputs two configurable Trigger Out and one Trigger In signal to synchronize patterns with a camera, sensor, or other peripherals.

Table 4. Pattern Display Signals

SIGNAL NAME	DESCRIPTION
TRIG_OUT_1	External Pattern Mode: Active during each input frame.
	Internal Pattern Mode: Active during a predefined group of patterns.
TRIG_OUT_2	Active during display of each pattern. When operating in external pattern mode, one input frame can have multiple patterns.
TRIG_IN	Active in Internal Pattern Display mode only. Trigger In signal is used to advance to next patterns in internal pattern mode.

8.3.1.1 External Pattern Mode

External pattern mode supports 8-bit and 1-bit monochrome or RGB patterns.

8.3.1.1.1 8-bit Monochrome Patterns

In 8-bit external pattern mode, the DLPC3478 controller supports up to 120-Hz input frame rate (VSYNC). In this mode, the 24-bit input data sent over the parallel interface can be configured as a combination of 1 (8-bits), 2 (16-bits), or 3 (24-bits) 8-bit patterns. Equation 1 calculates the maximum pattern rate for 8-bit pattern.

$$120 \text{ Hz} \times 3 = 360 \text{ Hz}$$

where

- the maximum allowed input frame rate is 120 Hz (1)

The DLPC3478 controller firmware allows for the following user programmability.

- Exposure time ($t_{Exposure}$): Time during which a pattern displayed and the illumination is ON.
- DarkPre time ($t_{DarkPre}$): Dark time (before the pattern exposure) during which no pattern displays and the illumination is OFF.
- DarkPost time ($t_{DarkPost}$): Dark time (after the pattern exposure) during which no pattern displays and the illumination is OFF.
- Number of 8-bit patterns within a frame: 1, 2, or 3 within each Frame period
- Selection of Illuminator that is ON for each 8-bit pattern.
- TRIG_OUT_1 and TRIG_OUT_2 signal configuration and delay

Figure 16 shows a configuration with 3 × 8-bit patterns.

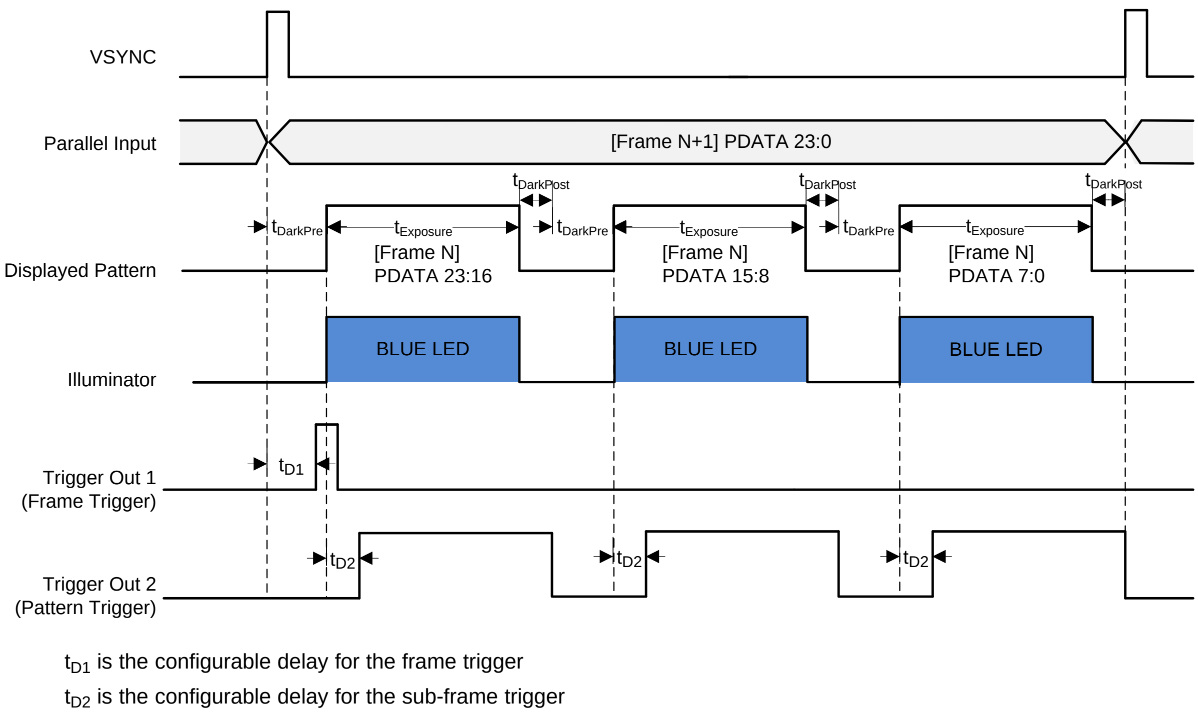


Figure 16. 3 × 8-bit (Blue) Pattern Configurations

- 3 × 8-bit patterns are displayed within each input VSYNC frame period.
- $t_{DarkPre}$, $t_{Exposure}$ and $t_{DarkPost}$are the same for each pattern within a frame period.
- The sum of dark time and exposure time ($t_{DarkPre}$ + $t_{Exposure}$ + $t_{DarkPost}$) for the three patterns must be equal to or less than the full frame period. If the sum is less than the full frame period, additional dark time will be appended to the end of the last pattern.
- Blue LED is configured to be ON for each pattern.
- TRIG_OUT_1 (Frame Trigger) is configured active high polarity and will have a minimum pulse width of 20 microseconds. TRIG_OUT_1 delay (t_{D1}) is configured with respect to input V_{SYNC}.
- TRIG_OUT_2 (Pattern Trigger) is configured active high polarity and stays active during the pattern exposure . TRIG_OUT_2 delay (t_{D2}) is configured with reference to the start of the pattern and is set once per pattern within a frame.

Figure 17 shows a configuration with 2 × 8-bit patterns.

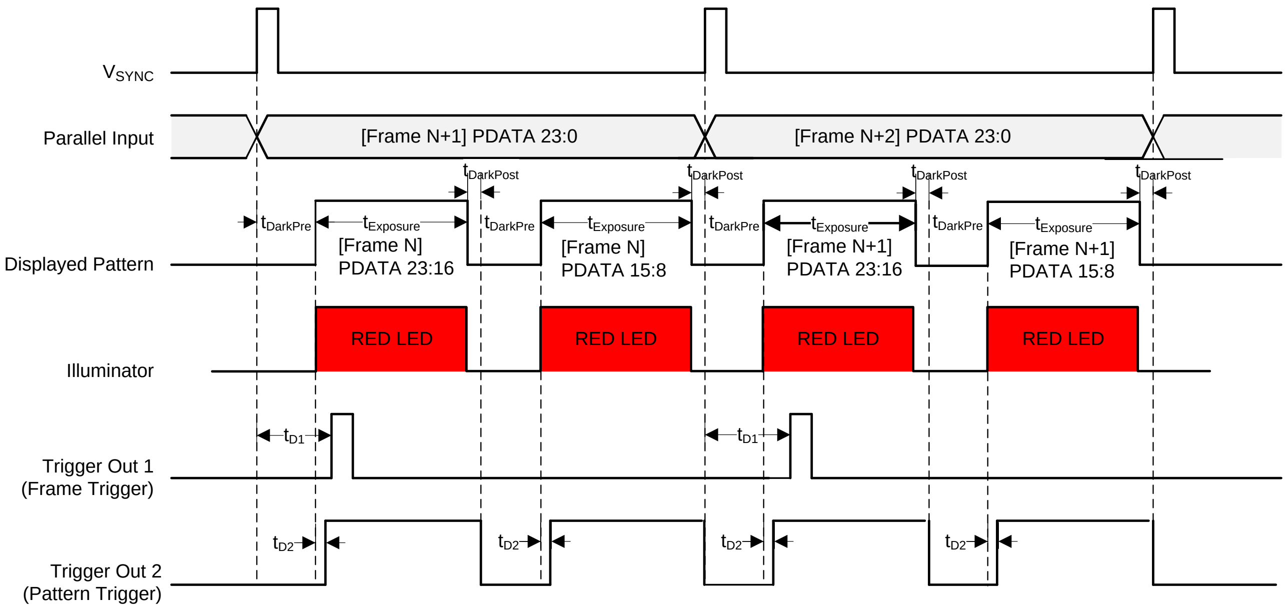


Figure 17. 2 × 8-bit (Red) Pattern Configurations

- 2 × 8-bit patterns are displayed within each input VSYNC frame period.
- $t_{DarkPre}$, $t_{Exposure}$ and $t_{DarkPost}$are the same for each pattern within a frame period.
- The sum of dark time and exposure time ($t_{DarkPre}$ + $t_{Exposure}$ + $t_{DarkPost}$) for the three patterns must be equal to or less than the full frame period. If the sum is less than the full frame period, additional dark time will be appended to the end of the last pattern.
- Red LED is configured to be ON for each pattern.
- TRIG_OUT_1 (Frame Trigger) is configured active high polarity and will have a minimum pulse width of 20 microseconds. TRIG_OUT_1 delay (t_{D1}) is configured with respect to input V_{SYNC}.
- TRIG_OUT_2 (Pattern Trigger) is configured active high polarity and stays active during the pattern exposure. TRIG_OUT_2 delay (t_{D2}) is configured with reference to the start of the pattern and is set once per pattern within a frame.

Figure 18 shows a configuration with 1 × 8-bit patterns.

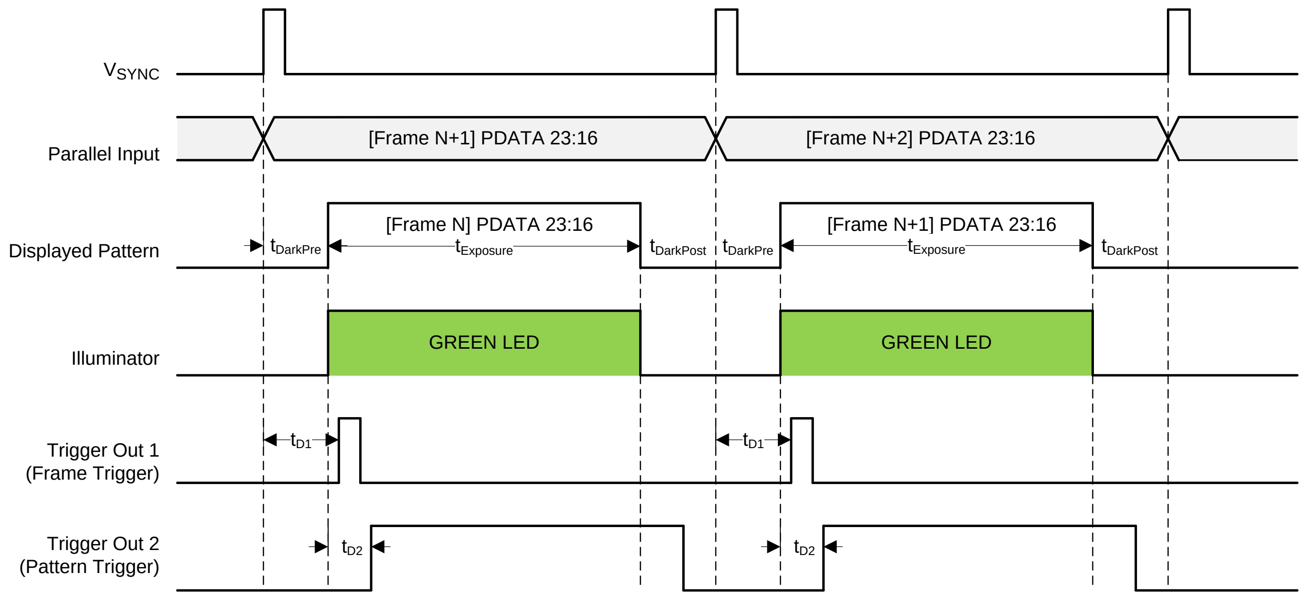


Figure 18. 1 × 8-bit (Green) Pattern Configurations

- 1 × 8-bit pattern is displayed within each input VSYNC frame period.
- $t_{DarkPre}$, $t_{Exposure}$ and $t_{DarkPost}$ are the same for each pattern within a frame period.
- The sum of dark time and exposure time ($t_{DarkPre}$ + $t_{Exposure}$ + $t_{DarkPost}$) for the three patterns must be equal to or less than the full frame period. If the sum is less than the full frame period, additional dark time will be appended to the end of the last pattern.
- Green LED is configured to be ON for each pattern.
- TRIG_OUT_1 (Frame Trigger) is configured active high polarity and will have a minimum pulse width of 20 microseconds. TRIG_OUT_1 delay (t_{D1}) is configured with respect to input V_{SYNC}.
- TRIG_OUT_2 (Pattern Trigger) is configured active high polarity and stays active during the pattern exposure . TRIG_OUT_2 delay (t_{D2}) is configured with reference to the start of the pattern and is set once per pattern within a frame.

8.3.1.1.2 1-Bit Monochrome Patterns

Similar to the 8-bit external pattern mode, the maximum supported input frame for 1-bit external pattern mode is 104.2 Hz. In 1-bit pattern mode each of the 24-bit inputs are treated as a separate binary patterns resulting in a maximum of 24 patterns. The maximum pattern rate for each 1-bit pattern is 2500 Hz.

The DLPC3478 controller firmware allows for the following user programmability:

- Exposure time: Time during which a pattern is displayed.
- Dark time: Time during which no pattern is displayed and the illumination in OFF.
- Number of 1-bit patterns within a frame- Up to maximum of 24.
- Illuminator: Illuminator that is ON for each 1-bit pattern. User defined illuminator is auto selected for all the patterns within a frame. User cannot select different illuminator for different 1-bit patterns within a frame.
- TRIG_OUT_1 and TRIG_OUT_2 signal configuration and delay.

Figure 19 shows a configuration with 24 × 1-bit patterns.

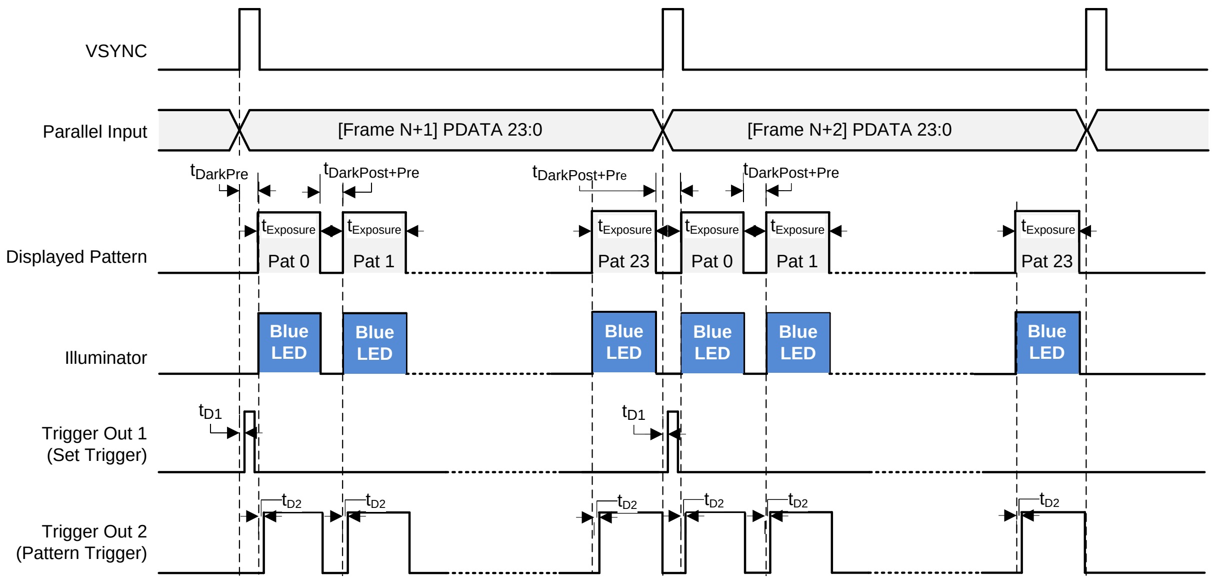


Figure 19. 24 × 1-bit (Blue) Pattern Configurations

- 24 × 1-bit patterns are displayed within each input VSYNC frame period.
- $t_{DarkPre}$, $t_{Exposure}$ and $t_{DarkPost}$are the same for each pattern within a frame period.
- The sum of dark time and exposure time ($t_{DarkPre}$ + $t_{Exposure}$ + $t_{DarkPost}$) for the three patterns must be equal to or less than the full frame period. If the sum is less than the full frame period, additional dark time will be appended to the end of the last pattern.
- Blue LED is configured to be ON for each pattern.
- TRIG_OUT_1 (Frame Trigger) is configured active high polarity and will have a minimum pulse width of 20 microseconds. TRIG_OUT_1 delay (t_{D1}) is configured with respect to input V_{SYNC}.
- TRIG_OUT_2 (Pattern Trigger) is configured active high polarity and stays active during the pattern exposure. TRIG_OUT_2 delay (t_{D2}) is configured with reference to the start of the pattern and is set once per pattern within a frame.

8.3.1.2 Internal Pattern Mode

There are two key differences between internal and external pattern mode:

- Internal pattern mode only supports 1D patterns i.e the pattern data is same across the entire row or column of the DMD (Figure 20, Figure 21).
- Internal pattern mode enables user to design a simple system by eliminating need of an external processor to generate and send patterns every frame. In internal pattern mode one row or one column patterns are pre-loaded in the flash memory and a command is send to DLPC3478 controller to display the patterns. Implementation details on how to create patterns, save patterns in Flash memory and load patterns from flash memory into the DLPC3478 controller's internal memory are described in SW Programmers Guide.

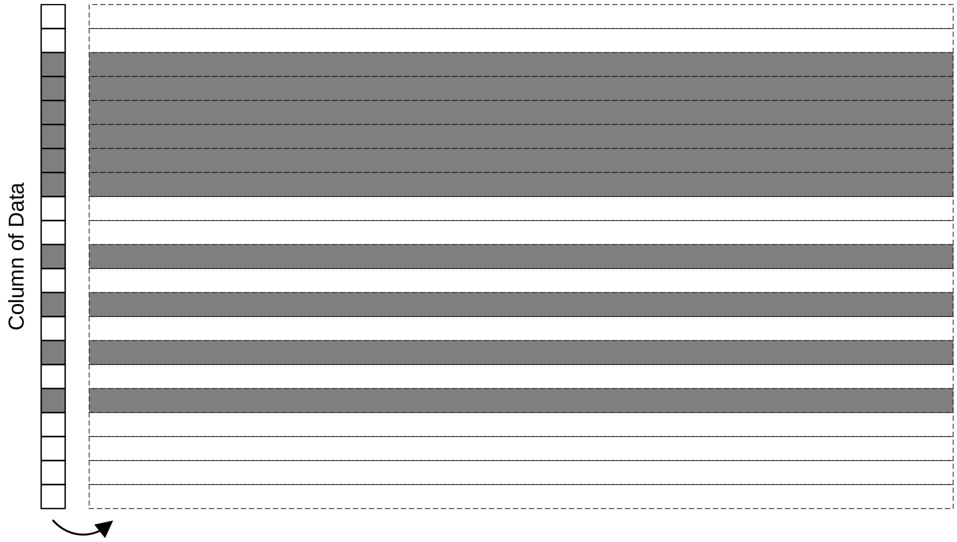


Figure 20. Column Replication

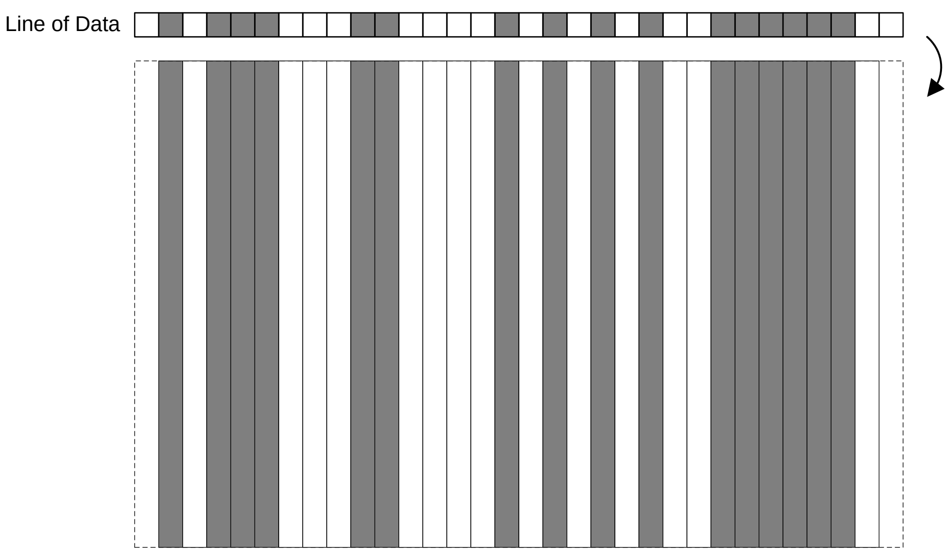


Figure 21. Row Replication

Internal pattern mode further provides two configurations to trigger the display of patterns, free running mode, (shown in Figure 22) and trigger in mode (shown in Figure 23).

8.3.1.2.1 Free Running Mode

In free running mode the DLPC3478 controller generates an internal synchronization signal to display pre-stored patterns. User sends an I^2C command to instruct DLPC3478 controller to start download of the 1D patterns from flash memory into DLPC3478 controller's internal memory and displaying of the 1D patterns.

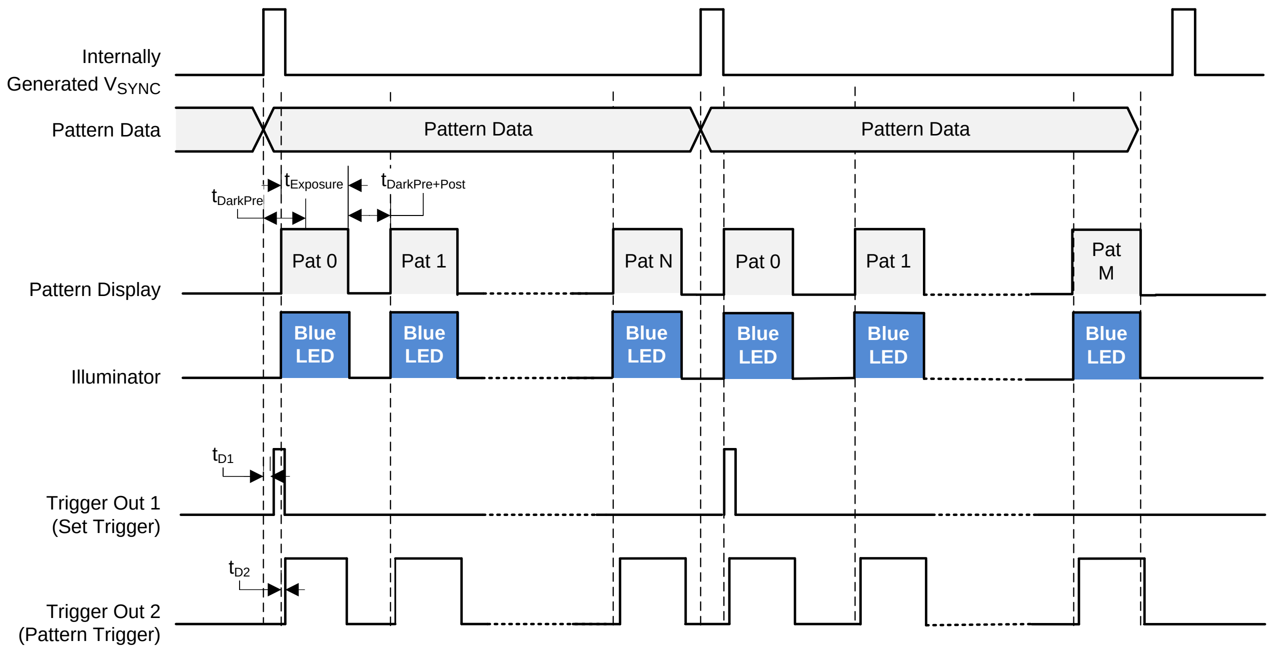


Figure 22. Free Running Mode

- The device displays multiple 1D patterns within an internally-generated V_{SYNC} signal. $t_{Exposure}$ (exposure time), $t_{DarkPre}$ and $t_{DarkPost}$ (dark time) are equal for all the 1D patterns within one internally generated V_{SYNC} frame.
- Blue LED is configured to be ON for each pattern.
- TRIG_OUT_1 (Frame Trigger) is configured active high polarity and will have a minimum pulse width of 20 microseconds. TRIG_OUT_1 delay (t_{D1}) is configured with respect to internally generated V_{SYNC}.
- TRIG_OUT_2 (Pattern Trigger) is configured active high polarity and stays active during the pattern exposure. TRIG_OUT_2 delay (t_{D2}) is configured with reference to the start of each pattern.
- V_{SYNC} is generated internally according to different sets of patterns stored in the SPI flash memory.

8.3.1.2.2 Trigger In Mode

Trigger In mode provides higher level of control to the user for displaying patterns. In this mode, user controls when to display the pattern by sending an external trigger signal to the DLPC3478 controller. The DLPC3478 controller outputs a Pattern Ready signal to let the user know when DLPC3478 controller is ready to accept the external trigger signal.

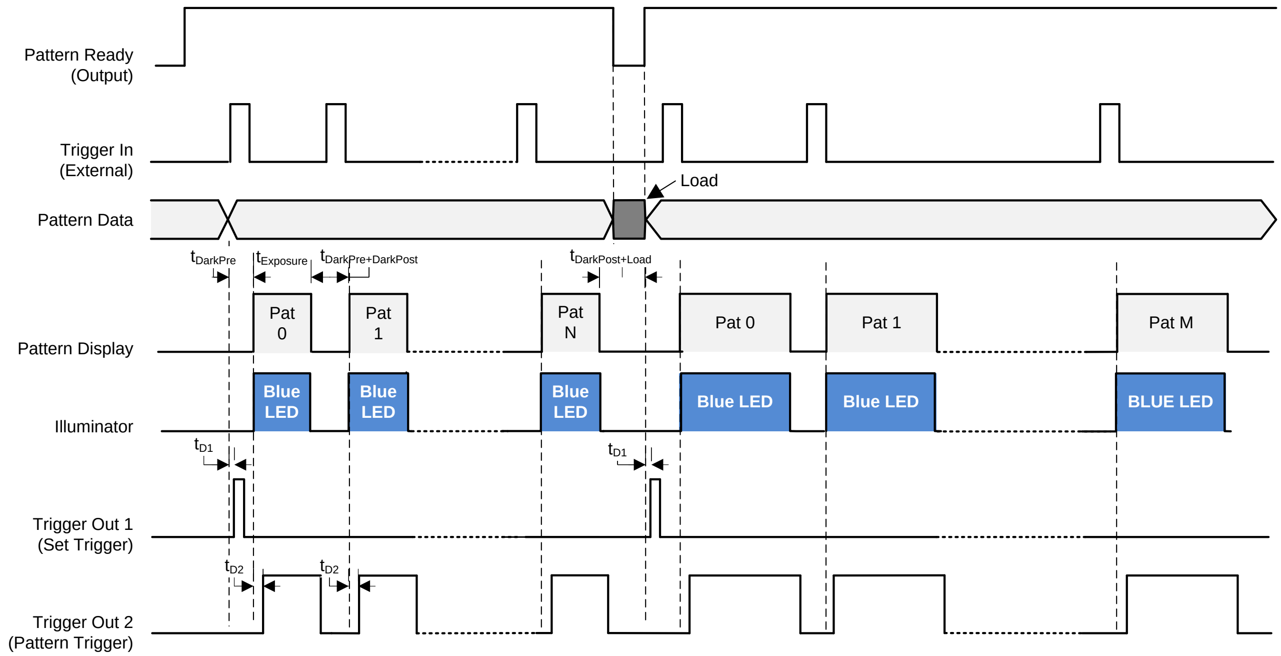


Figure 23. Trigger In Mode

- DLPC3478 controller sets the Pattern Ready signal high to denote that the DLPC3478 controller is ready to accept Trigger In signal.
- The user sends the external trigger input signal to the DLPC3478 controller to begin the display of the next pattern with $t_{Exposure}$ (exposure time), $t_{DarkPre}$ and $t_{DarkPost}$ (dark time).
- Blue LED is configured to be ON for each pattern.
- TRIG_OUT_1 (Pattern Set Trigger) is configured active high polarity and will have a minimum pulse width of 20 microseconds. TRIG_OUT_1 delay (t_{D1}) is configured with respect to external trigger input (TRIG_IN).
- TRIG_OUT_2 (Pattern Trigger) is configured active high polarity and stays active during the pattern exposure. TRIG_OUT_2 delay (t_{D2}) is configured with reference to the start of each pattern exposure.

8.3.2 Interface Timing Requirements

This section defines the timing requirements for the external interfaces for the DLPC3478 ASIC.

8.3.2.1 Parallel Interface

The parallel interface complies with standard graphics interface protocol, which includes a vertical sync signal (VSYNC_WE), horizontal sync signal (HSYNC_CS), optional data valid signal (DATAEN_CMD), a 24-bit data bus (PDATA), and a pixel clock (PCLK). The polarity of both syncs and the active edge of the clock are programmable. Figure 4 shows the relationship of these signals. The data valid signal (DATAEN_CMD) is optional in that the DLPC3478 provides auto-framing parameters that can be programmed to define the data valid window based on pixel and line counting relative to the horizontal and vertical syncs.

In addition to these standard signals, an optional side-band signal (PDM_CVS_TE) is available, which allows periodic frame updates to be stopped without losing the displayed image. When PDM_CVS_TE is active, it acts as a data mask and does not allow the source image to be propagated to the display. A programmable PDM polarity parameter determines if it is active high or active low. This parameter defaults to make PDM_CVS_TE active high. If this function is not desired, tie PDM_CVS_TE to a logic low signal on the PCB. The device allows PDM_CVS_TE to change only during vertical blanking.

NOTE

VSYNC_WE must remain active at all times (in lock-to-VSYNC mode) or the display sequencer stops and causes the LEDs to be turned off.

8.4 Serial Flash Interface

DLPC3478 device uses an external SPI serial flash memory device for configuration support. The minimum required size is dependent on the desired minimum number of sequences, CMT tables, and splash options while the maximum supported is 16 Mb.

For access to flash, the DLPC3478 device uses a single SPI interface operating at a programmable frequency complying to industry standard SPI flash protocol. The programmable SPI frequency is defined to be equal to 180 MHz/N, where N is a programmable value between 5 to 127 providing a range from 36.0 to 1.41732 MHz. Note that this results in a relatively large frequency step size in the upper range (for example, 36 MHz, 30 MHz, 25.7 MHz, 22.5 MHz, and so forth) and thus this must be taken into account when choosing a flash device.

The device supports two independent SPI chip selects; however, the flash must be connected to SPI chip select zero (SPI0_CSZ0) because the boot routine is only executed from the device connected to chip select zero (SPI0_CSZ0). The boot routine uploads program code from flash to program memory, then transfers control to an auto-initialization routine within program memory. The device asserts the HOST_IRQ output signal high while auto-initialization is in progress, then drives it low to signal its completion to the host processor. Only after auto-initialization is complete is the device ready to receive commands through I^2C.

The device supports any flash device that is compatible with the modes of operation, features, and performance as defined in Table 5 and Table 6.

Table 5. SPI Flash Required Features or Modes of Operation

FEATURE	DLPC3478 REQUIREMENT
SPI interface width	Single
SPI protocol	SPI mode 0
Fast READ addressing	Auto-incrementing
Programming mode	Page mode
Page size	256 B
Sector size	4 KB sector
Block size	any
Block protection bits	0 = Disabled
Status register bit(0)	Write in progress (WIP) {also called flash busy}
Status register bit(1)	Write enable latch (WEN)
Status register bits(6:2)	A value of 0 disables programming protection
Status register bit(7)	Status register write protect (SRWP)
Status register bits(15:8) (that is expansion status byte)	The device supports only single-byte status register R/W command execution, and thus may not be compatible with flash devices that contain an expansion status byte. However, as long as expansion status byte is considered optional in the byte 3 position and any write protection control in this expansion status byte defaults to unprotected, then the device shares compatibility with the DLPC3478 device.

To support flash devices with program protection defaults of either enabled or disabled, the DLPC3478 device always assumes the device default is enabled and goes through the process of disabling protection as part of the boot-up process. This process consists of:

- A write enable (WREN) instruction executed to request write enable, followed by
- A read status register (RDSR) instruction is then executed (repeatedly as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, a write status register (WRSR) instruction is executed that writes 0 to all 8-bits (this disables all programming protection)

Prior to each program or erase instruction, the DLPC3478 issues:

- A write enable (WREN) instruction to request write enable, followed by
- A read status register (RDSR) instruction (repeated as needed) to poll the write enable latch (WEL) bit

- After the write enable latch (WEL) bit is set, the program or erase instruction is executed
- Note the flash automatically clears the write enable status after each program and erase instruction

The specific instruction OpCode and timing compatibility requirements are listed in Table 8 and Table 7. Note however that the device does not read the flash electronic signature ID and thus cannot automatically adapt protocol and clock rate based on the ID.

Table 6. SPI Flash Instruction OpCode and Access Profile Compatibility Requirements

SPI FLASH COMMAND	FIRST BYTE (OPCODE)	SECOND BYTE	THIRD BYTE	FOURTH BYTE	FIFTH BYTE	SIXTH BYTE
Fast READ (1 Output)	0x0B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0) (1)
Read status	0x05	n/a	n/a	STATUS(0)		
Write status	0x01	STATUS(0)	(2)			
Write enable	0x06					
Page program	0x02	ADDRS(0)	ADDRS(1)	ADDRS(2)	DATA(0) (1)	
Sector erase (4KB)	0x20	ADDRS(0)	ADDRS(1)	ADDRS(2)		
Chip erase	0xC7					

(1) Only the first data byte is show, data continues
(2) DLPC3478 device does not support access to a second/ expansion Write Status byte

The specific and timing compatibility requirements for a DLPC3478 device compatible flash are listed in Table 7 and Table 8.

Table 7. SPI Flash Key Timing Parameter Compatibility Requirements (1) (2)

SPI FLASH TIMING PARAMETER	SYMBOL	ALTERNATE SYMBOL	MIN	MAX	UNIT
Access frequency (all commands)	FR	f_C	≤1.42		MHz
Chip select high time (also called chip select deselect time)	t_{SHSL}	t_{CSH}	≤200		ns
Output hold time	t_{CLQX}	t_{HO}	≥0		ns
Clock low to output valid time	t_{CLQV}	t_V		≤ 11	ns
Data in set-up time	t_{DVCH}	t_{DSU}	≤5		ns
Data in hold time	t_{CHDX}	t_{DH}	≤5		ns

(1) The timing values are related to the specification of the flash device itself, not the DLPC3478 device .
(2) The DLPC3478 device does not drive the HOLD or WP (active low write protect) pins on the flash device, and thus these pins are typically tied to a logic high on the PCB through an external pullup.

The DLPC3478 device supports 1.8-, 2.5-, or 3.3-V serial flash devices. To do so, VCC_FLSH must be supplied with the corresponding voltage. Table 8 contains a list of 1.8-, 2.5-, and 3.3-V compatible SPI serial flash devices supported by DLPC3478 device .

Table 8. Compatible SPI Flash Device Options (1) (2)

DVT (3)	DENSITY (Mb)	VENDOR	PART NUMBER	PACKAGE SIZE
1.8-V COMPATIBLE DEVICES				
Yes	4 Mb	Winbond	W25Q40BWUXIG	2 × 3 mm USON
Yes	4 Mb	Macronix	MX25U4033EBAI-12G	1.43 × 1.94 mm WLCSP
Yes	8 Mb	Macronix	MX25U8033EBAI-12G	1.68 × 1.99 mm WLCSP
2.5- OR 3.3-V COMPATIBLE DEVICES				
Yes	16 Mb	Winbond	W25Q16CLZPIG	5 × 6 mm WSON
Yes	32 Mb	Winbond	W25Q32FVSSIG	5.2 x 7.9 mm SOIC

8.4.1 Serial Flash Programming

Note that the flash can be programmed through the DLPC3478 device over I^2C or by driving the SPI pins of the flash directly while the DLPC3478 device I/O are tri-stated. SPI0_CLK, SPI0_DOUT, and SPI0_CSZ0 I/O can be tri-stated by holding RESETZ in a logic low state while power is applied to the DLPC3478 device . The SPI0_CSZ1 signal is not tri-stated by this same action.

(1) The flash supply voltage must match VCC_FLSH on the DLPC3478 device. Special attention needs to be paid when ordering devices to be sure the desired supply voltage is attained as multiple voltage options are often available under the same base part number.
(2) Beware when considering Numonyx (Micron) serial flash devices as they typically do not have the 4KB sector size needed to be DLPC3478 device compatible.
(3) All of these flash devices appear compatible with the DLPC3478 device , but only those marked with yes in the DVT column have been validated on the EVM reference design. Those marked with no can be used at the ODM's own risk.

8.4.2 SPI Signal Routing

The DLPC3478 device supports two SPI slave devices on the SPI0 interface, specifically, a serial flash and the DLPA200x or DLPA300x. This requires routing associated SPI signals to two locations while attempting to operate up to 36 MHz. Take special care to ensure that reflections do not compromise signal integrity. Follow these recommendations.

- Split the SPI0_CLK PCB signal trace from the DLPC3478 source to each slave device into separate routes as close to the DLPC3478 device as possible. Ensure that the SPI0_CLK trace length to each device are equal in total length.
- Split the SPI0_DOUT PCB signal trace from the DLPC3478 device source to each slave device into separate routes as close to the DLPC3478 device as possible. Ensure that the SPI0_DOUT trace length to each device are equal in total length (use the same strategy as listed for SPI0_CLK).
- Ensure the SPI0_DIN PCB signal trace from each slave device to the point where they intersect on the return to the DLPC3478 device are equal in length and as short as possible. Ensure that each slave device shares a common trace back to the DLPC3478 device.
- SPI0_CSZ0 and SPI0_CSZ1 need no special treatment because they are dedicated signals and drive only one device.

8.4.3 I^{2}C Interface Performance

Both DLPC3478 I^{2}C interface ports support 100-kHz baud rate. By definition, I^{2}C transactions operate at the speed of the slowest device on the bus, thus there is no requirement to match the speed grade of all devices in the system.

8.4.4 Content-Adaptive Illumination Control

Content-adaptive illumination control (CAIC) is an image processing algorithm that takes advantage of the fact that in common real-world image content most pixels in the images are well below full scale for the for the R, G, and B digital channels being input to the DLPC3478 device . As a result of this the average picture level (APL) for the overall image is also well below full scale, and the system's dynamic range for the collective set of pixel values is not fully utilized. CAIC takes advantage of this headroom between the source image APL and the top of the available dynamic range of the display system.

CAIC evaluates images frame by frame and derives three unique digital gains, one for each of the R, G, and B color channels. During CAIC image processing, each gain is applied to all pixels in the associated color channel. CAIC derives each color channel's gain that is applied to all pixels in that channel so that the pixels as a group collectively shift upward and as close to full scale as possible. To prevent any image quality degradation, the gains are set at the point where just a few pixels in each color channel are clipped. Figure 24 and Figure 25 show an example of the application of CAIC for one color channel.

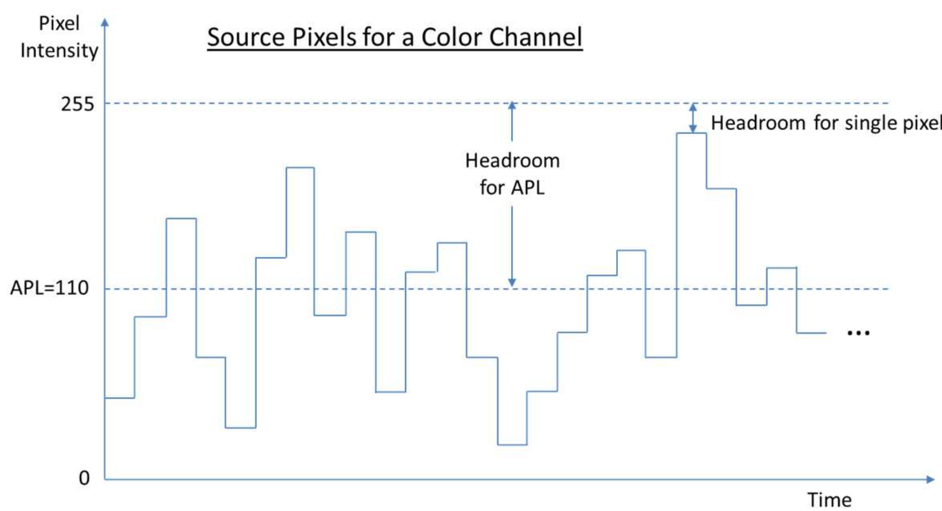


Figure 24. Input Pixels Example

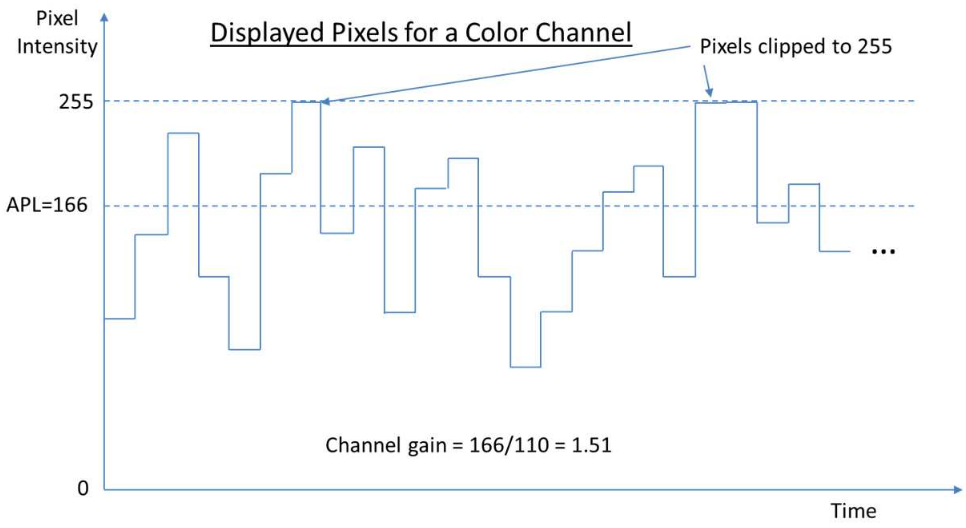


Figure 25. Displayed Pixels After CAIC Processing

Figure 25 shows the gain that is applied to a color processing channel inside the device. CAIC also adjusts the power for the R, G, and B LED. For each color channel of an individual frame, CAIC determines the optimal combination of digital gain and LED power. The decision regarding how much digital gain to apply to a color channel and how much to adjust the LED power for that color is heavily influenced by the software command settings sent to the device for configuring CAIC.

As CAIC applies a digital gain to each color channel independently, and adjusts each LED's power independently, CAIC also makes sure that the resulting color balance in the final image matches the target color balance for the projector system. Thus, the effective displayed white point of images is held constant by CAIC from frame to frame.

Because the R, G, and B channels can be gained up by CAIC inside the device, the LED power can be turned down for any color channel until the brightness of the color on the screen is unchanged. Thus, CAIC can achieve an overall LED power reduction while maintaining the same overall image brightness as if CAIC was not used. Figure 26 shows an example of LED power reduction by CAIC for an image where the R and B LEDs can be turned down in power.

CAIC can alternatively be used to increase the overall brightness of an image while holding the total power for all LEDs constant. In summary, when CAIC is enabled CAIC can operate in one of two distinct modes:

- Power Reduction Mode – holds overall image brightness constant while reducing LED power
- Enhanced Brightness Mode – holds overall LED power constant while enhancing image brightness

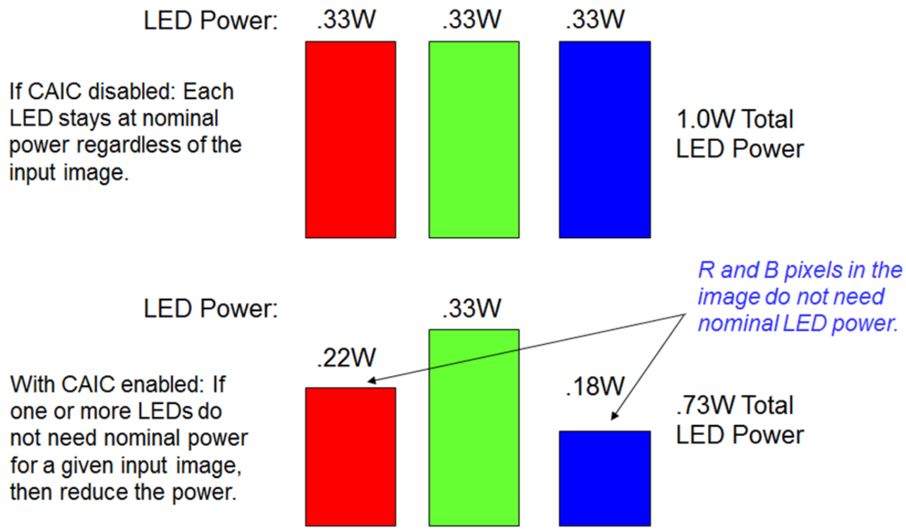


Figure 26. CAIC Power Reduction Mode (for Constant Brightness)

8.4.5 Local Area Brightness Boost

Local area brightness boost (LABB), is an image processing algorithm that adaptively gains up regions of an image that are dim relative to the average picture level. Some regions of the image have significant gain applied, and some regions have little or no gain applied. LABB evaluates images frame by frame and derives the local area gains to be used uniquely for each image. Because many images have a net overall boost in gain even if some areas of the image get no gain, the overall perceived brightness of the image is boosted.

Figure 27 shows a split screen example of the impact of the LABB algorithm for an image that includes dark areas.

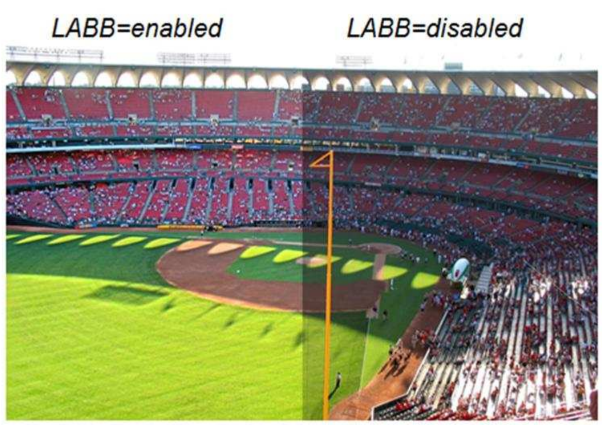


Figure 27. Boosting Brightness in Local Areas of an Image

LABB works best when the decision about the strength of gains used is determined by ambient light conditions. For this reason, there is an option to add an ambient light sensor which can be read by the DLPC3478 device during each frame. Based on the sensor readings, LABB applies higher gains for bright rooms to help overcome any washing out of images. LABB applies lower gains in dark rooms to prevent over-punching of images.

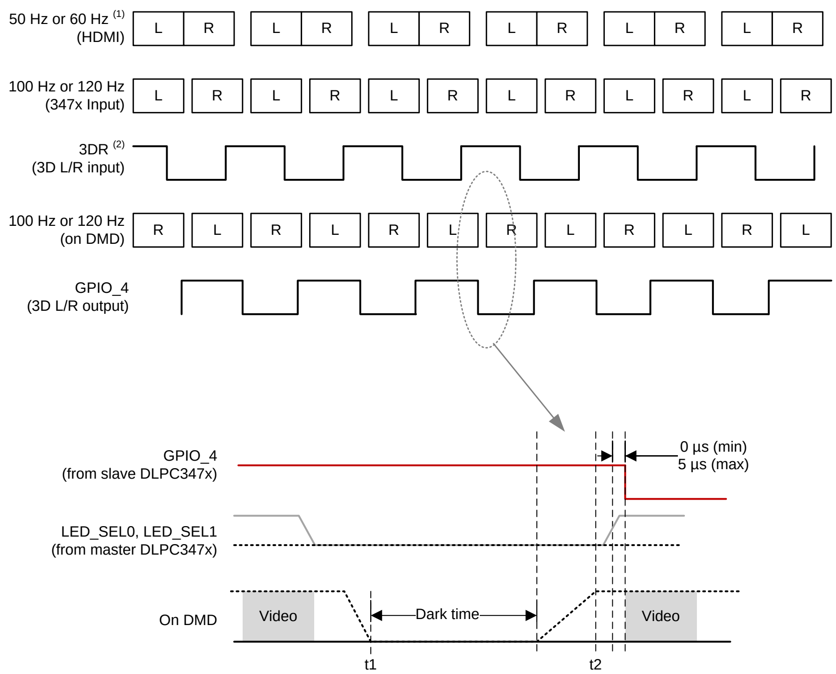
8.4.6 3-D Glasses Operation

For supporting 3D glasses, the DLPC3478 device-based chip set outputs sync information to synchronize the Left eye/Right eye shuttering in the glasses with the displayed DMD image frames.

Two different types of glasses are often used to achieve synchronization. One relies on an infrared (IR) transmitter on the system PCB to send an IR sync signal to an IR receiver in the glasses. In this case device output signal GPIO_04 can be used to cause the IR transmitter to send an IR sync signal to the glasses. The timing for signal GPIO_04 is shown in Figure 9.

The second type of glasses relies on sync information that is encoded into the light being outputted from the projection lens. This is referred to as the DLP Link approach for 3D, and many 3D glasses from different suppliers have been built using this method. This demonstrates that the DLP Link method can work reliable. The advantage of the DLP Link approach is that it takes advantage of existing projector hardware to transmit the sync information to the glasses. This can save cost, size and power in the projector.

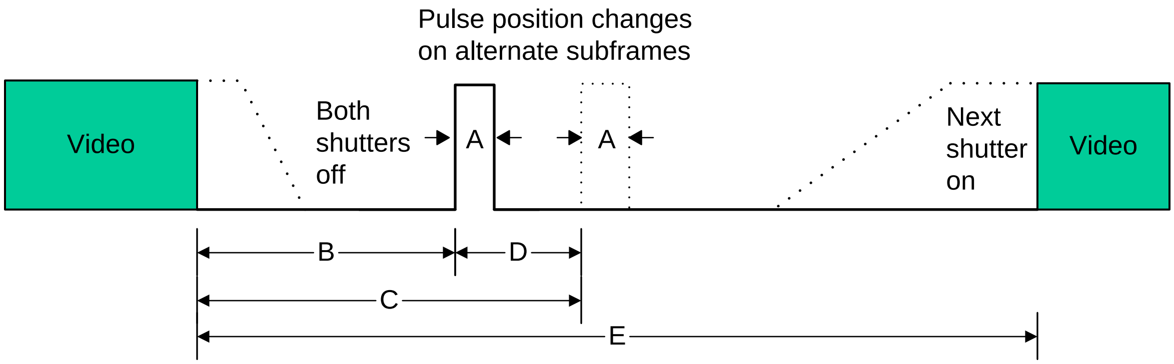
For generating the DLP Link sync information, one light pulse per DMD frame is outputted from the projection lens while the glasses have both shutters closed. To achieve this, the device signals the DLPA200x device or DLPA300x device when to enable the illumination source (typically LEDs or lasers) so that an encoded light pulse is output once per DMD frame. Because the shutters in the glasses are both off when the DLP Link pulse is sent, the projector illumination source is also disabled except when the device sends light to create the DLP Link pulse. Figure 28 and Figure 29 show the timing for the light pulses for DLP Link 3D operation.



(1) Left = 1, Right = 0

(2) 3DR must toggle 1 ms before VSYNC

Figure 28. Controller L/R Frame and Signal Timing for DLP Link



NOTE: The period between DLPLink pulses alternates between the subframe period =D and the subframe period -D, where D is the delta period.

Figure 29. 3D DLP Link Pulse Timing

Table 9. 3D Link Nominal Timing Table

HDMI Source Reference	3D DMD SEQUENCE RATE (Hz)	A	B	C	D	E
23.6	94.5	25	500	628	128	>2000
24.0	96	25	500	628	128	>2000
49.0	98	25	500	628	128	>2000
50.0	100	25	500	628	128	>2000
51.0	102	25	500	628	128	>2000
59.0	118	25	500	628	128	>2000
60.0	120	25	500	628	128	>2000
61.0	122	25	500	628	128	>2000

8.4.7 DMD (Sub-LVDS) Interface

The DLPC3478 ASIC DMD interface consists of a HS 1.8-V sub-LVDS output only interface with a maximum clock speed of 600-MHz DDR and a LS SDR (1.8-V LVCMOS) interface with a fixed clock speed of 120 MHz. The device sub-LVDS interface supports a number of DMD display sizes, and as a function of resolution, not all output data lanes are needed as DMD display resolutions decrease in size. With internal software selection, the device also supports a limited number of DMD interface swap configurations that can help board layout by remapping specific combinations of DMD interface lines to other DMD interface lines as needed. Table 10 shows the four options available for the DLP3010 (.3 720p) DMD specifically.

Table 10. DLP3010 (.3720p) DMD – ASIC to 8-Lane DMD Pin Mapping Options

DLPC3478 ASIC 8 LANE DMD ROUTING OPTIONS		DMD PINS
OPTION 1 Swap Control = x0	OPTION 2 Swap Control = x2	
HS_WDATA_D_P HS_WDATA_D_N	HS_WDATA_E_P HS_WDATA_E_N	Input DATA_p_0 Input DATA_n_0
HS_WDATA_C_P HS_WDATA_C_N	HS_WDATA_F_P HS_WDATA_F_N	Input DATA_p_1 Input DATA_n_1
HS_WDATA_B_P HS_WDATA_B_N	HS_WDATA_G_P HS_WDATA_G_N	Input DATA_p_2 Input DATA_n_2
HS_WDATA_A_P HS_WDATA_A_N	HS_WDATA_H_P HS_WDATA_H_N	Input DATA_p_3 Input DATA_n_3
HS_WDATA_H_P HS_WDATA_H_N	HS_WDATA_A_P HS_WDATA_A_N	Input DATA_p_4 Input DATA_n_4
HS_WDATA_G_P HS_WDATA_G_N	HS_WDATA_B_P HS_WDATA_B_N	Input DATA_p_5 Input DATA_n_5

Table 10. DLP3010 (.3720p) DMD – ASIC to 8-Lane DMD Pin Mapping Options (continued)

DLPC3478 ASIC 8 LANE DMD ROUTING OPTIONS		DMD PINS
OPTION 1 Swap Control = x0	OPTION 2 Swap Control = x2	
HS_WDATA_F_P HS_WDATA_F_N	HS_WDATA_C_P HS_WDATA_C_N	Input DATA_p_6 Input DATA_n_6
HS_WDATA_E_P HS_WDATA_E_N	HS_WDATA_D_P HS_WDATA_D_N	Input DATA_p_7 Input DATA_n_7

8.4.8 Calibration and Debug Support

The DLPC3478 device contains a test point output port, TSTPT_(7:0), which provides selected system calibration support as well as ASIC debug support. These test points are inputs while reset is applied and switch to outputs when reset is released. The state of these signals is sampled upon the release of system reset and the captured value configures the test mode until the next time reset is applied. Each test point includes an internal pulldown resistor, thus external pullups must be used to modify the default test configuration. The default configuration (x000) corresponds to the TSTPT_(7:0) outputs remaining tri-stated to reduce switching activity during normal operation. For maximum flexibility, an option to jumper to an external pullup is recommended for TSTPT_(2:0). Pullups on TSTPT_(6:3) are used to configure the ASIC for a specific mode or option. TI does not recommend adding pullups to TSTPT_(7:3) because this has adverse affects for normal operation. This external pullup value is sampled only during a 0-to-1 transition on the RESETZ input, thus changing the configuration after reset is released and has no effect until the next time reset is asserted and released. Table 11 defines the test mode selection for one programmable scenario defined by TSTPT(2:0).

Table 11. Test Mode Selection Scenario Defined by TSTPT(2:0)(1)

TSTPT(2:0) CAPTURE VALUE	NO SWITCHING ACTIVITY	CLOCK DEBUG OUTPUT
	x000	x010
TSTPT(0)	HI-Z	60 MHz
TSTPT(1)	HI-Z	30 MHz
TSTPT(2)	HI-Z	0.7 to 22.5 MHz
TSTPT(3)	HI-Z	HIGH
TSTPT(4)	HI-Z	LOW
TSTPT(5)	HI-Z	HIGH
TSTPT(6)	HI-Z	HIGH
TSTPT(7)	HI-Z	7.5 MHz

(1) These are only the default output selections. Software can reprogram the selection at any time.

8.4.9 DMD Interface Considerations

The sub-LVDS HS interface waveform quality and timing on the DLPC3478 device ASIC is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

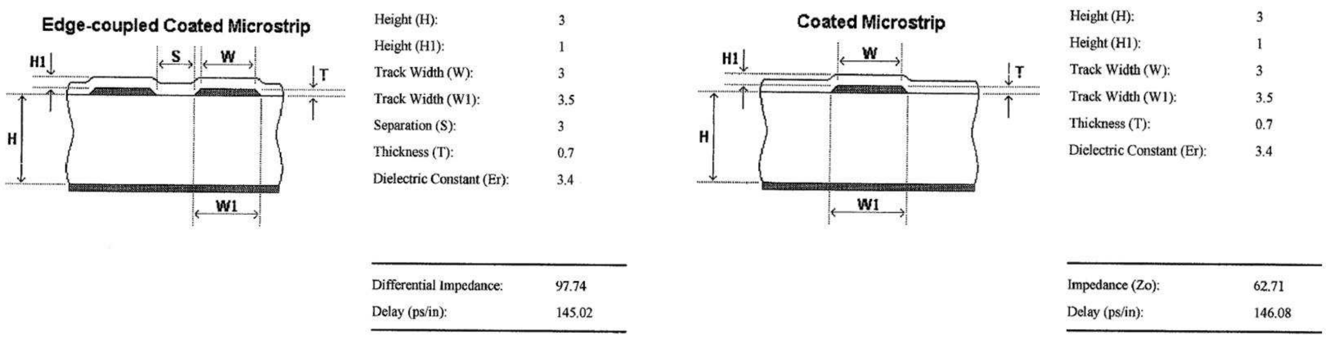
Setup Margin = (DLPC3478 output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation) (2)

Hold-time Margin = (DLPC3478 output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

where PCB SI degradation is signal integrity degradation due to PCB affects which includes such things as Simultaneously Switching Output (SSO) noise, cross-talk and Inter-symbol Interference (ISI) noise. (3)

The data sheets for the DMD devices include I/O timing parameters and DMD I/O timing parameters. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. However, PCB SI degradation is a more complicated adjustment.

In an attempt to minimize the signal integrity analysis that would otherwise be required, use these PCB design guidelines as a reference of an interconnect system to satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Be sure to compare any variation from these recommendations with PCB signal integrity analysis or lab measurements.



DMD_HS Differential Signals DMD_LS Signals

Figure 30. DMD Interface Board Stack-Up Details

8.4.10 Device Functional Modes

DLPC3478 device has two functional modes (ON/OFF) controlled by a single pin PROJ_ON:

- When pin PROJ_ON is set high, the projector automatically powers up and an image is projected from the DMD.
- When pin PROJ_ON is set low, the projector automatically powers down and only microwatts of power are consumed.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DLPC3478 device controller is required to be coupled with DLP3010 DMD to provide a reliable display solution for various data and video display applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the device. Applications of interest include accessory projectors, projectors embedded in display devices like notebooks, laptops, tablets, and hot spots. Other applications include wearable (near-eye or head mounted) displays, interactive display, low latency gaming display, and digital signage.

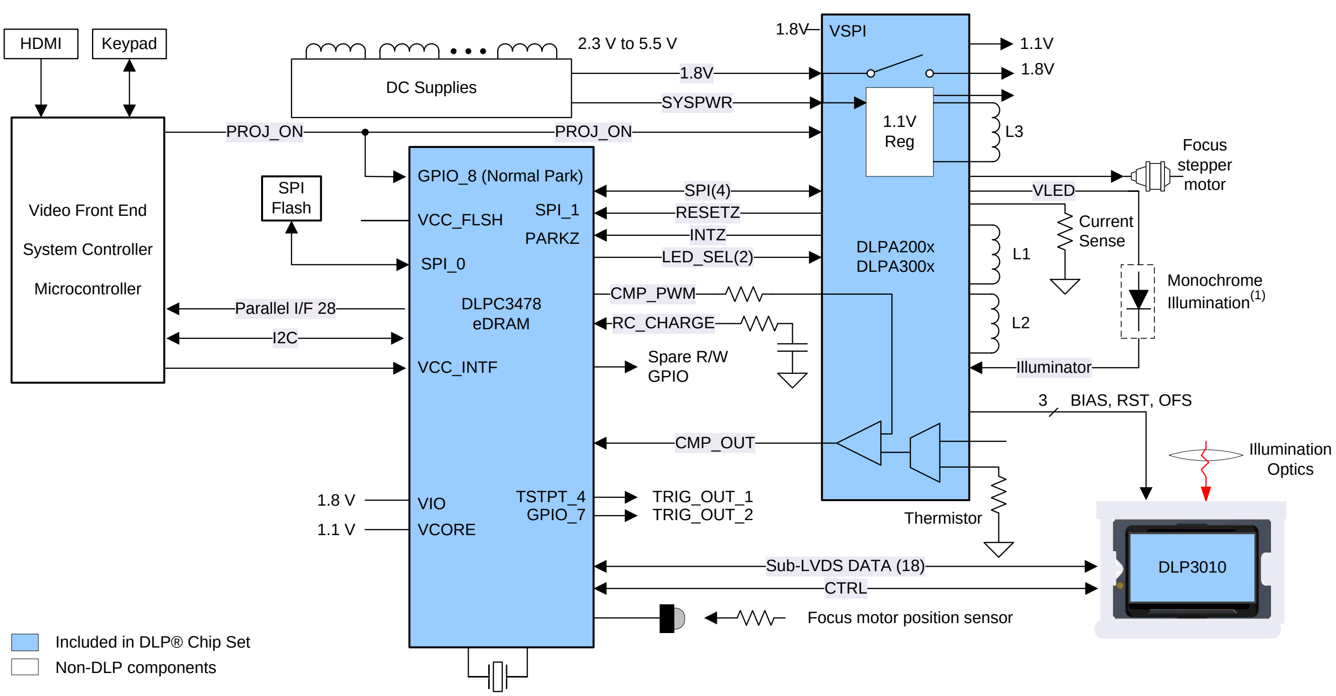
9.1.1 DLPC3478 System Design Consideration

System power regulation: It is acceptable for VDD_PLLD and VDD_PLLM to be derived from the same regulator as the core VDD, but to minimize the AC noise component are typically filtered as recommended in the *PCB Layout Guidelines for Internal ASIC PLL Power*.

9.2 Typical Application

9.2.1 3D Depth Scanner with DLP Using External Pattern Streaming Mode

The DLPC3478 controller with DLP3010 DMD enables high accuracy and very small form factor 3D Depth scanner products. Figure 31 shows a typical 3D depth capture scanner block diagrams using external pattern streaming mode.



(1) Options to elect different LEDs, but only 1 channel used at a time

Figure 31. External Pattern Streaming Mode

Typical Application (continued)

9.2.1.1 Design Requirements

A high-accuracy, 3D depth scanner product is created by using a DLP chipset comprised of DLP3010 DMD, DLPC3478 controller and DLPA200x or DLPA300x PMIC and LED driver. The DLPC3478 simplifies the pattern generation, the DLPA200x or DLPA300x provides the needed analog functions and DMD displays the required patterns for accurate 3D depth capture.

In addition to the three DLP devices in the chipset, other components may be required to complete the application. Minimally, a flash component is required to store patterns, the software, and the firmware in order to control the DLPC3478 controller.

DLPC3478 controller supports any illumination source including IR light source (LEDs or VCSE), UV light source or visible light source (Red, Green or Blue LEDs or lasers).

For connecting the DLPC3478 controller to the host processing for receiving patterns or video data parallel interface is used. Connect an I^2C iinterface to the host processor to send commands to the DLPC3478 controller. The only power supplies needed external to the projector are the battery (SYSPWR) and a regulated 1.8-V supply. A single signal (PROJ_ON) controls the entire DLP system power. When PROJ_ON is high, the DLP system turns on and when PROJ_ON is low, the DLPC3478 turns off and draws only a few microamperes of current on SYSPWR. When PROJ_ON is low, the 1.8-V power supply can remain at 1.8 V for use by other sub systems. When PROJ_ON is low, the DLPA200x or DLPA300x 000 draws no current on the 1.8-V supply.

9.2.1.2 Detailed Design Procedure

For connecting the DLP3010 DMD, the DLPC3478 controller and the DLPA200x or DLPA300x PMIC/LED driver see the reference design schematic. An example board layout is included in the reference design data base. Follow the layout guidelines shown in to achieve reliable DLP system results.

9.2.1.3 Application Curve

As the LED currents that are driven through the red, green or blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is shown in Figure 32. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs. For mono-chrome use case with a single LED or a different light source, this curve will be different and the specific light source documentation needs to be referred for similar information.

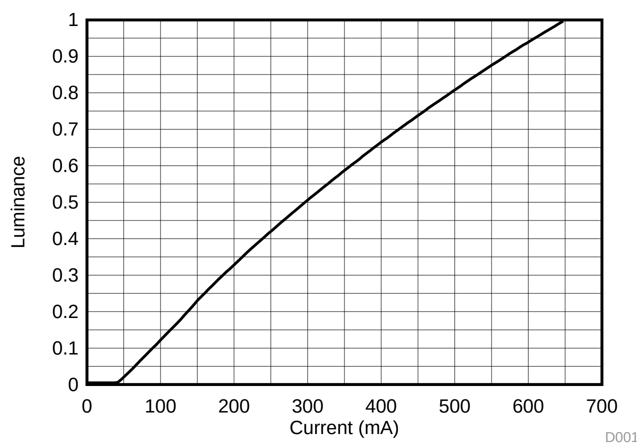
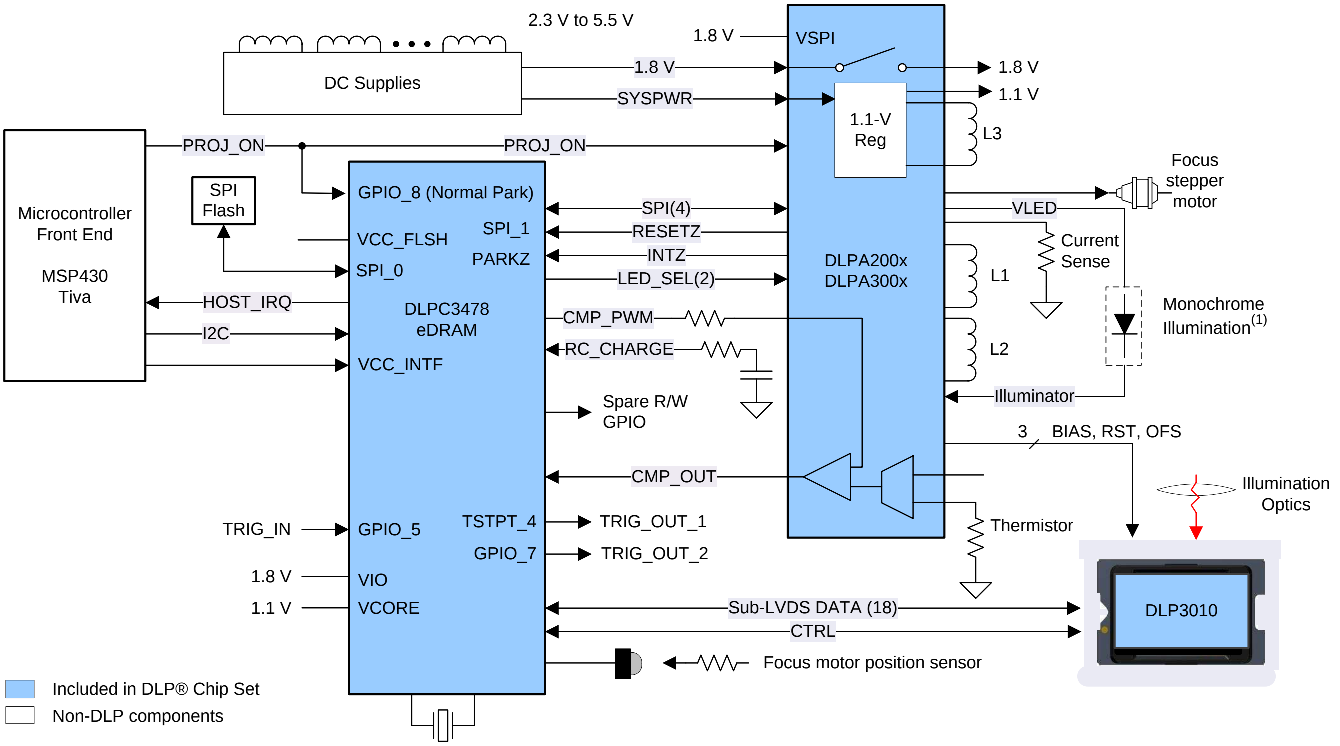


Figure 32. Luminance vs Current

9.2.2 3D Depth Scanner Using Internal Pattern Streaming Mode

Figure 33 shows a typical 3D depth scanner system block diagrams using internal pattern streaming mode.

Typical Application (continued)



(1) Options to elect different LEDs, but only 1 channel used at a time

Figure 33. Internal Pattern Streaming Mode

9.2.2.1 Design Requirements

The design requirements for the 3D Depth scanner system using Internal Pattern Streaming Mode is identical to the design procedure for the 3D Depth scanner system External Pattern Streaming Mode. (See the Design Requirements section.)

9.2.2.2 Detailed Design Procedure

The design procedure for the 3D Depth Sensor DLP Using Internal Pattern Streaming Mode is identical to the design procedure for the 3D Depth Sensor DLP Using External Pattern Streaming Mode. (See the Detailed Design Procedure section.)

9.2.2.3 Application Curve

See the Application Curve as the brightness considerations are similar in both external and internal pattern streaming modes.

10 Power Supply Recommendations

10.1 System Power-Up and Power-Down Sequence

Although the DLPC3478 requires an array of power supply voltages, (for example, VDD, VDDLP12, VDD_PLLM/D, VCC18, VCC_FLSH, VCC_INTF), if VDDLP12 is tied to the 1.1-V VDD supply (which is assumed to be the typical configuration), then there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC3478. (This is true for both power-up and power-down scenarios). Similarly, there is no minimum time between powering-up or powering-down the different supplies if VDDLP12 is tied to the 1.1-V VDD supply.

If however VDDLP12 is not tied to the VDD supply, then VDDLP12 must be powered-on after the VDD supply is powered-on, and powered-off before the VDD supply is powered-off. In addition, if VDDLP12 is not tied to VDD, then VDDLP12 and VDD supplies are typically powered on or powered off within 100 ms of each other.

Although there is no risk of damaging the DLPC3478 if the above power sequencing rules are followed, the following additional power sequencing recommendations must be considered to ensure proper system operation.

- To ensure that DLPC3478 output signal states behave as expected, ensure that all DLPC3478 I/O supplies remain applied while VDD core power is applied. If VDD core power is removed while the I/O supply (VCC_INTF) is applied, then the output signal state associated with the inactive I/O supply enters into a high impedance state.
- Additional power sequencing rules may exist for devices that share the supplies with the DLPC3478, and thus these devices may force additional system power sequencing requirements.

Note that when VDD core power is applied, but I/O power is not applied, additional leakage current may be drawn. This added leakage does not affect normal DLPC3478 operation or reliability.

Figure 34 and Figure 35 show the DLPC3478 power-up and power-down sequence for both the normal PARK and fast PARK operations of the DLPC3478 ASIC.

System Power-Up and Power-Down Sequence (continued)

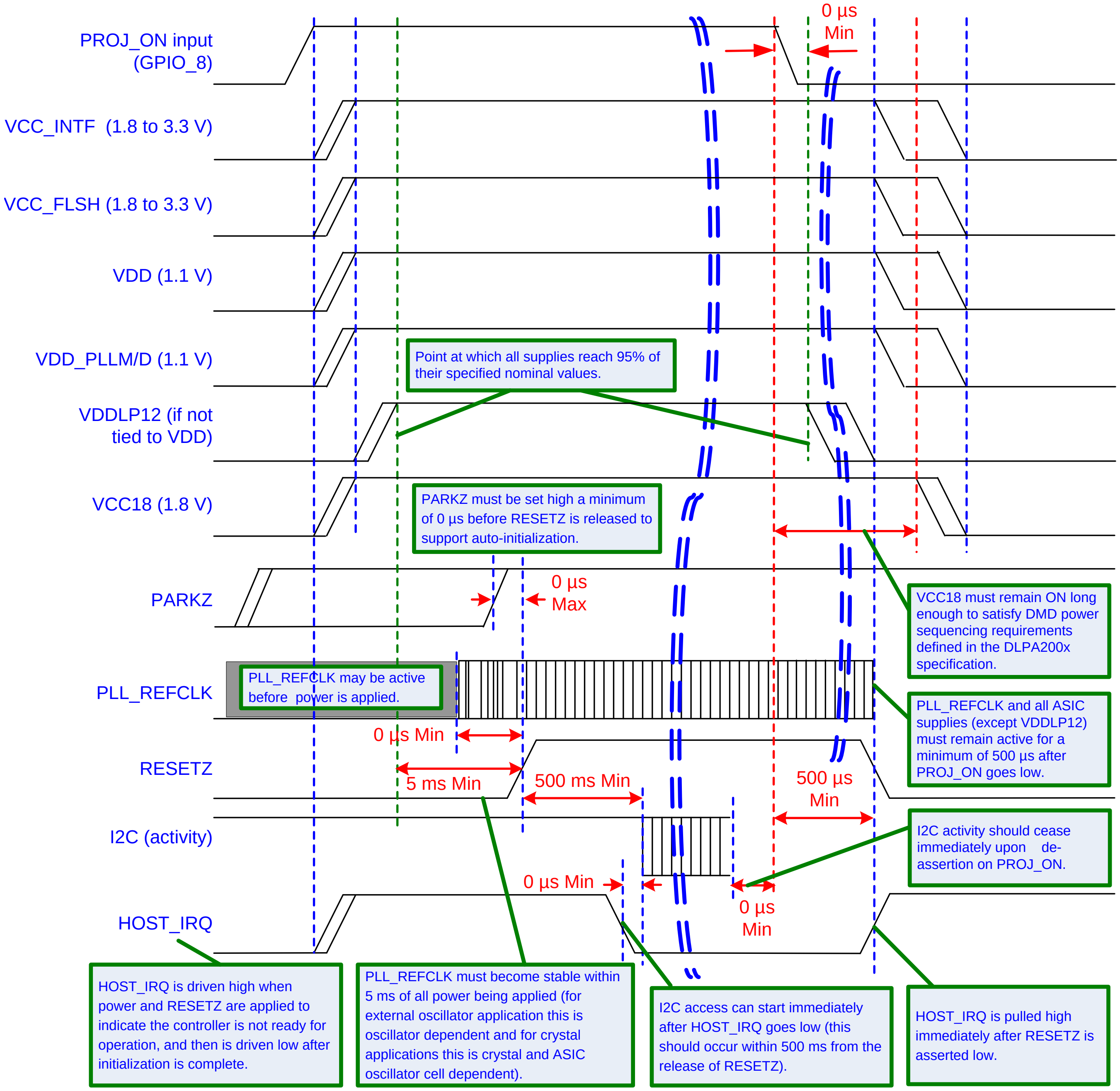


Figure 34. DLPC3478 Power-Up / PROJ_ON = 0 Initiated Normal PARK and Power-Down

System Power-Up and Power-Down Sequence (continued)

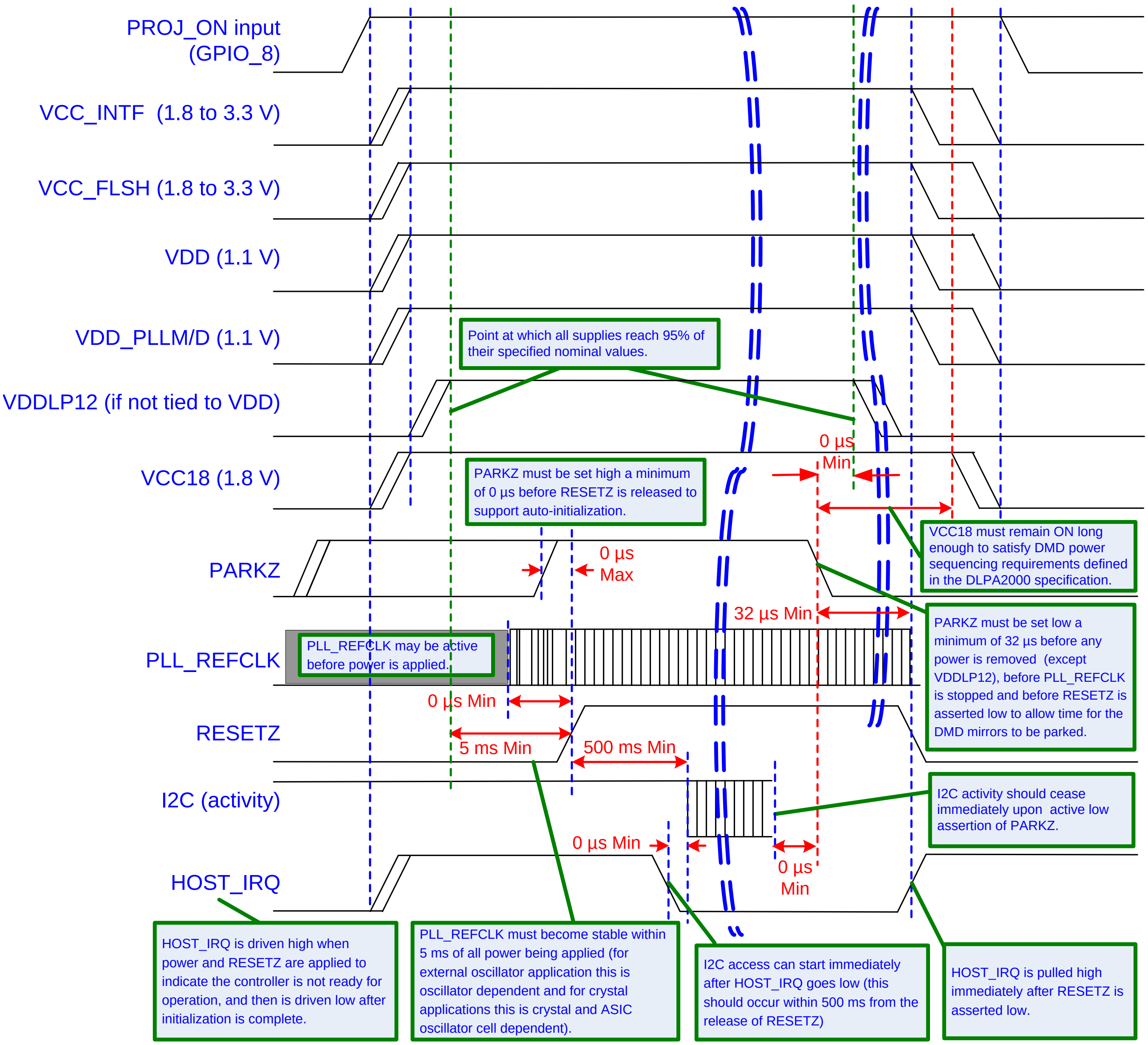


Figure 35. DLPC3478 Power-Up / PARKZ = 0 Initiated Fast PARK and Power-Down

10.2 DLPC3478 Power-Up Initialization Sequence

An external power monitor holds the DLPC3478 device in a system reset state during power-up by driving RESETZ to a logic low state. It continues to assert system reset until all ASIC voltages have reached minimum specified voltage levels, PARKZ is asserted high, and input clocks are stable. During this time, the device drives most ASIC outputs to an inactive state and configures all bidirectional signals as inputs to avoid contention. ASIC outputs that are not driven to an inactive state are tri-stated. These include LED_SEL_0, LED_SEL_1, SPICLK, SPIDOUT, and SPICSZ0 (see RESETZ pin description for full signal descriptions in *Pin Configuration and Functions*. After power is stable and the PLL_REFCLK_I clock input to the DLPC3478 is stable, then RESETZ is typically deactivated (set to a logic high). The DLPC3478 then performs a power-up initialization routine that first locks its PLL followed by loading self configuration data from the external flash. Upon release of RESETZ all

DLPC3478 Power-Up Initialization Sequence (continued)

DLPC3478 I/Os become active. Immediately following the release of RESETZ, the device drives the HOST_IRQ signal high to indicate that the auto initialization routine is in progress. However, because a pullup resistor connects the signal HOST_IRQ, this signal goes high before the DLPC3478 device actively drives it high. Upon completion of the auto-initialization routine, the DLPC3478 drives HOST_IRQ low to indicate the initialization done state of the DLPC3478 device has been reached.

NOTE

The host processor can start sending I^2C commands after HOST_IRQ goes low.

10.3 DMD Fast PARK Control (PARKZ)

The PARKZ signal acts as an early warning signal that alerts the ASIC 40 µs before DC supply voltages have dropped below specifications in fast PARK operation. This alert allows the ASIC time to park the DMD, ensuring the integrity of future operation. Typically, the reference clock continues to run and RESETZ remains deactivated for at least 40 µs after PARKZ has been deactivated (set to a logic low) to allow the park operation to complete.

10.4 Hot Plug Usage

The DLPC3478 device provides fail-safe I/O on all host interface signals (signals powered by VCC_INTF). This protection allows these inputs to be driven high even when no I/O power is applied. Under this condition, the device does not load the input signal nor draw excessive current that could degrade ASIC reliability. For example, the I^2C bus from the host to other components is not affected by powering off VCC_INTF to the DLPC3478 device. TI recommends the application include weak pullup or pulldown components on signals feeding back to the host to avoid floating inputs.

If the I/O supply (VCC_INTF) is powered off, but the core supply (VDD) is powered on, then the corresponding input buffer may experience added leakage current, but this does not damage the DLPC3478.

10.5 Maximum Signal Transition Time

Unless otherwise noted, 10 ns is the maximum recommended 20 to 80% rise or fall time to avoid input buffer oscillation. This applies to all DLPC3478 input signals. However, the PARKZ input signal includes an additional small digital filter that ignores any input buffer transitions caused by a slower rise or fall time for up to 150 ns.

11 Layout

11.1 Layout Guidelines

11.1.1 PCB Layout Guidelines for Internal ASIC PLL Power

The following guidelines are recommended to achieve desired ASIC performance relative to the internal PLL. The DLPC3478 contains 2 internal PLLs which have dedicated analog supplies (VDD_PLLM , VSS_PLLM, VDD_PLLD, VSS_PLLD). As a minimum, isolate VDD_PLLx power and VSS_PLLx ground pins using a simple passive filter consisting of two series Ferrites and two shunt capacitors (to widen the spectrum of noise absorption). The recommended values are for one 0.1-µf capacitor and one 0.01-µf capacitor. Place all four components as close to the ASIC as possible. It is critical to keep the leads of the high frequency capacitors as short as possible. Connect both capacitors across VDD_PLLM and VSS_PLLM / VDD_PLLD and VSS_PLLD respectfully on the ASIC side of the Ferrites.

Ferrite bead specification recommendations:

- DC resistance less than 0.40 Ω
- Impedance at 10 MHz equal to or greater than 180 Ω
- Impedance at 100 MHz equal to or greater than 600 Ω

The PCB layout is critical to PLL performance. It is vital to treat the quiet ground and power as analog signals. Therefore, VDD_PLLM and VDD_PLLD must be a single trace from the DLPC3478 to both capacitors and then through the series ferrites to the power source. Make the power and ground traces as short as possible, parallel to each other, and as close as possible to each other.

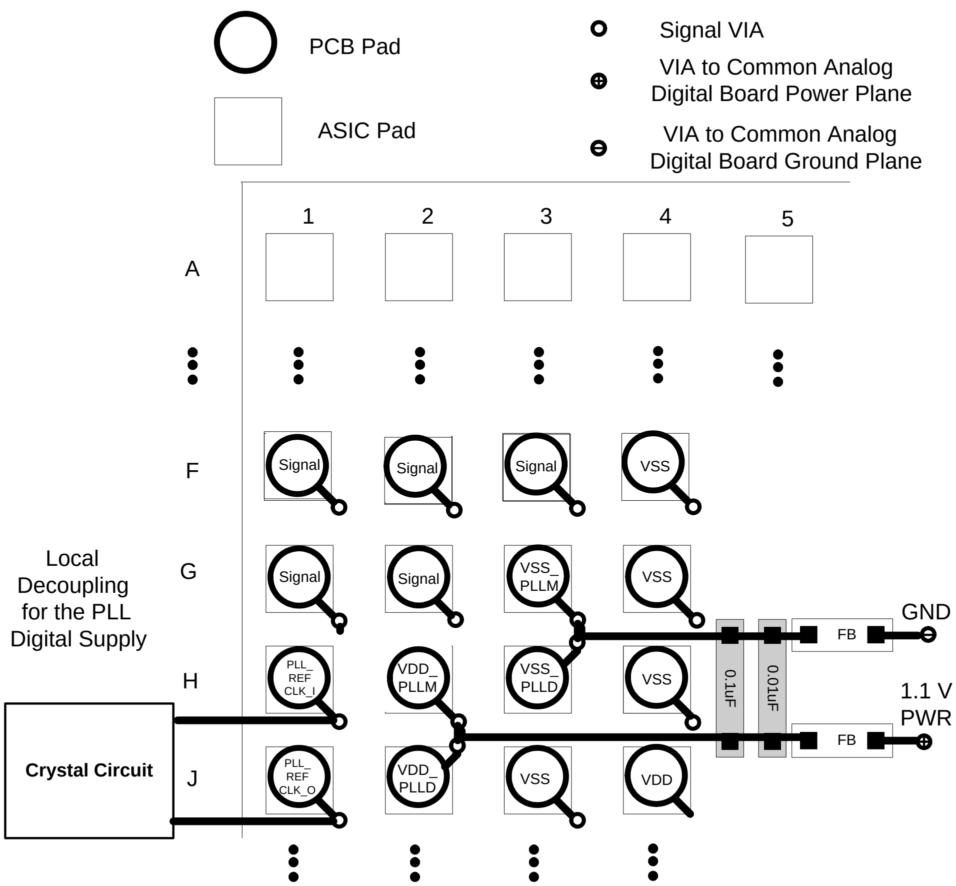
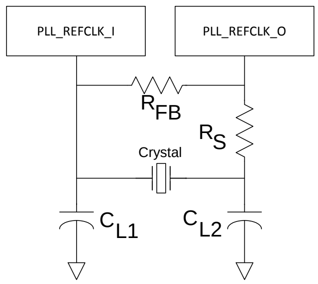


Figure 36. PLL Filter Layout

Layout Guidelines (continued)

11.1.2 DLPC3478 Reference Clock

The DLPC3478 requires an external reference clock to feed its internal PLL. A crystal or oscillator can supply this reference. For flexibility, the DLPC3478 accepts either of two reference clock frequencies (see Table 13), but both must have a maximum frequency variation of ±200 ppm (including aging, temperature, and trim component variation). When a crystal is used, several discrete components are also required as shown in Figure 37.



A. CL = Crystal load capacitance (farads)

B. CL1 = 2 × (CL – Cstray_pll_refclk_i)

C. CL2 = 2 × (CL – Cstray_pll_refclk_o)

D. Where: Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_i. Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_o.

Figure 37. Reference Crystal Connections

11.1.2.1 Recommended Crystal Oscillator Configuration

Table 12. Crystal Port Characteristics

PARAMETER	NOM	UNIT
PLL_REFCLK_I TO GND capacitance	1.5	pF
PLL_REFCLK_O TO GND capacitance	1.5	pF

Table 13. Recommended Crystal Configuration(1)(2)

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	24 or 16	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±200	PPM
Maximum startup time	1.0	ms
Crystal equivalent series resistance (ESR)	120 max	Ω
Crystal load	6	pF
RS drive resistor (nominal)	100	Ω
RFB feedback resistor (nominal)	1Meg	Ω
CL1 external crystal load capacitor	See equation in Figure 37 notes	pF
CL2 external crystal load capacitor	See equation in Figure 37 notes	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) Temperature range of –30°C to +85°C
(2) The crystal bias is determined by the ASIC's VCC_INTF voltage rail, which is variable (not the VCC18 rail).

If the application uses an external oscillator, the oscillator output must drive the PLL_REFCLK_I pin on the DLPC3478 ASIC and the PLL_REFCLK_O pins must remain unconnected.

Table 14. DLPC3478 Recommended Crystal Parts(1)(2)(3)

PASSED DVT	MANUFACTURER	PART NUMBER	SPEED	TEMPERATURE AND AGING	ESR	LOAD CAPACITANCE
Yes	KDS	DSX211G-24.000M-8pF-50-50	24 MHz	±50 ppm	120-Ω max	8 pF
Yes	Murata	XRCGB24M000F0L11R0	24 MHz	±100 ppm	120-Ω max	6 pF
Yes	NDK	NX2016SA 24M EXS00A-CS05733	24 MHz	±145 ppm	120-Ω max	6 pF

(1) These crystal devices appear compatible with the DLPC3478, but only those marked with yes in the DVT column have been validated.
(2) Crystal package sizes: 2.0 × 1.6 mm for both crystals.
(3) Operating temperature range: –30°C to +85°C for all crystals.

11.1.3 General PCB Recommendations

TI recommends 1-oz. copper planes in the PCB design to achieve needed thermal connectivity.

11.1.4 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused ASIC input pins be tied through a pullup resistor to its associated power supply or a pulldown to ground. For ASIC inputs with an internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Internal pullup and pulldown resistors are weak. Do not expect them to drive the external line. The DLPC3478 device implements very few internal resistors and these are noted in the pin list. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value 8 kΩ (max).

Never tie unused output-only pins directly to power or ground. Instead leave them open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they are typically pulled-up (or pulled-down) using an appropriate, dedicated resistor.

11.1.5 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

Table 15. Max Pin-to-Pin PCB Interconnect Recommendations

DMD BUS SIGNAL	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 152.4	See	inch (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 152.4	See	inch (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 165.1	See	inch (mm)
DMD_LS_WDATA	6.5 165.1	See	inch (mm)
DMD_LS_RDATA	6.5 165.1	See [(1)]	inch (mm)
DMD_DEN_ARSTZ	7.0 177.8	See [(1)]	inch (mm)

(1) Due to board variations, these are impossible to define. Any board designs simulate using SPICE with the ASIC IBIS models to ensure single routing lengths do not exceed requirements.

Table 16. High Speed PCB Signal Routing Matching Requirements (1)(2)(3)(4)

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH (5)	UNIT
DMD	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	inch (mm)
DMD	DMD_HS_WDATA_x_P	DMD_HS_WDATA_x_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_HS_CLK_P	DMD_HS_CLK_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	inch (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

(1) These values apply to PCB routing only. They do not include any internal package routing mismatch associated with the DLPC3478 or the DMD.
(2) DMD HS data lines are differential, thus these specifications are pair-to-pair.
(3) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
(4) DMD LS signals are single ended.
(5) Mismatch variance for a signal group is always with respect to reference signal.

11.1.6 Number of Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers, but ensure that the signals of a given pair do not change layers.

11.1.7 Stubs

- Avoid using stubs.

11.1.8 Terminations

- DMD_HS differential signals require no external termination resistors.
- The DMD_LS_CLK and DMD_LS_WDATA signal paths typically include a 43-Ω series termination resistor located as close as possible to the corresponding ASIC pins.
- The DMD_LS_RDATA signal path typically include a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- DMD_DEN_ARSTZ does not require a series resistor.

11.1.9 Routing Vias

- Be sure to minimize the number of vias on DMD_HS signals and do not exceed two.
- Any and all vias on DMD_HS signals are typically located as close to the ASIC as possible.
- The number of vias on the DMD_LS_CLK and DMD_LS_WDATA signals are typically minimized and do not exceed two.
- Locate any and all vias on the DMD_LS_CLK and DMD_LS_WDATA signals as close to the ASIC as

possible.

11.2 Layout Example

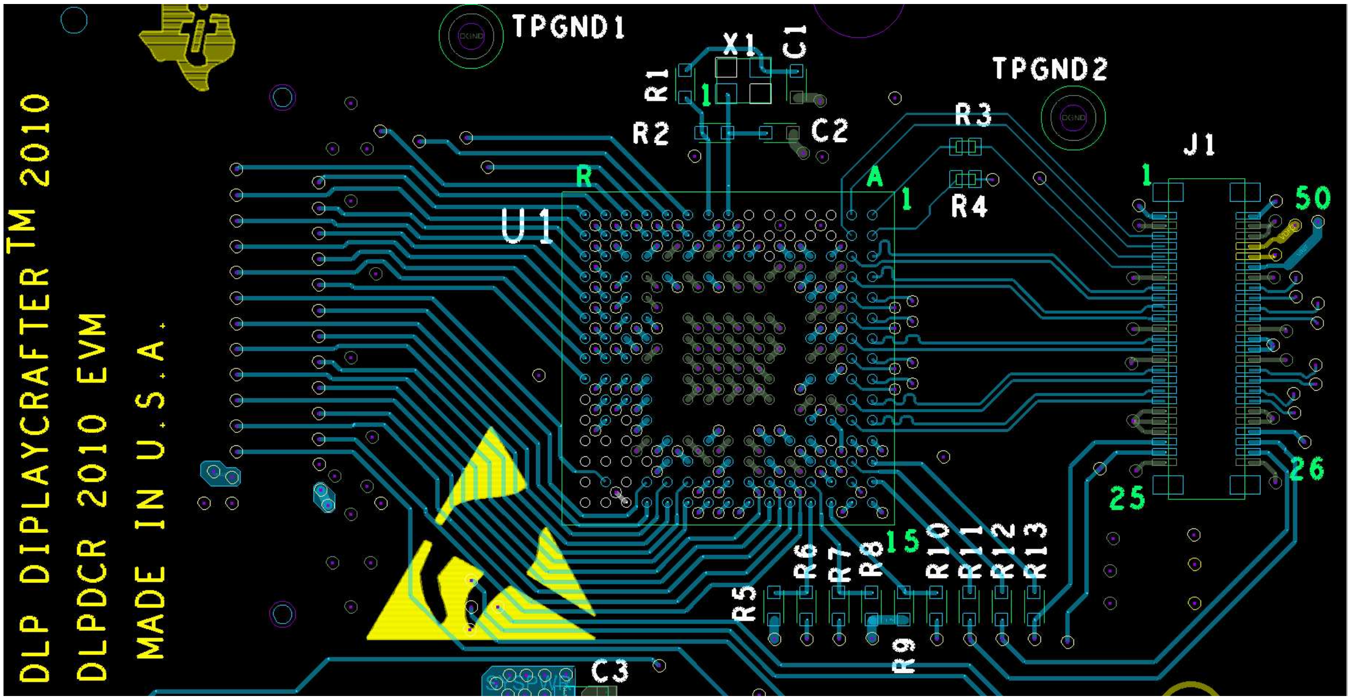


Figure 38. Example Layout

11.3 Thermal Considerations

The underlying thermal limitation for the DLPC3478 is that the maximum operating junction temperature (T_J) not be exceeded (this is defined in the). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC3478, and power dissipation of surrounding components. The DLPC3478's package is designed primarily to extract heat through the power and ground planes of the PCB. Thus, copper content and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on maximum DLPC3478 power dissipation and $R_{\theta JA}$ at 0 m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC standard high-k 2s2p PCB with two, 1-oz. power planes. This JEDEC test PCB is not necessarily representative of the DLPC3478 PCB; the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. However, after the PCB is designed and the product is built, TI highly recommended that thermal performance be measured and validated.

To do this, measure the top center case temperature under the worse case product scenario (max power dissipation, max voltage, max ambient temperature) and validated not to exceed the maximum recommended case temperature (T_C). This specification is based on the measured φ_{JT} for the DLPC3478 package and provides a relatively accurate correlation to junction temperature. Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. The bead and thermocouple wire typically contact the top of the package and are covered with a minimal amount of thermally conductive epoxy. Route the wires closely along the package and the board surface to avoid cooling the bead through the wires.

12 Device and Documentation Support

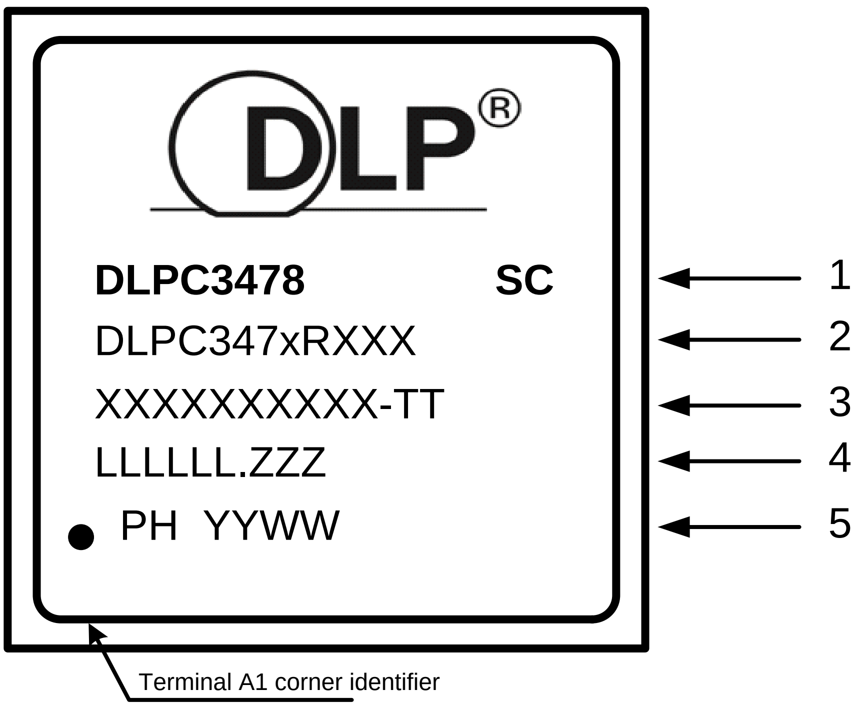
12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Device Nomenclature

12.1.2.1 Device Markings



Marking Definitions:

Line 1: DLP® Device Name: DLPC3478 device name ID.
SC: Solder ball composition
e1: Indicates lead-free solder balls consisting of SnAgCu
G8: Indicates lead-free solder balls consisting of tin-silver-copper (SnAgCu) with silver content less than or equal to 1.5% and that the mold compound meets TI's definition of green.

Line 2: TI Part Number
DLP® Device Name: DLPC347x = **x** indicates 8 device name ID.
R corresponds to the TI device revision letter for example A, B or C
XXX corresponds to the device package designator.

Line 3: XXXXXXXXXX-TT Manufacturer part number

Line 4: LLLLLL.ZZZ Foundry lot code for semiconductor wafers and lead-free solder ball marking
LLLLLL: Fab lot number
ZZZ: Lot split number

Device Support (continued)

Line 5: PH YYWW: Package assembly information
PH: Manufacturing site
YYWW: Date code (YY = Year :: WW = Week)

NOTE

1. Engineering prototype samples are marked with an **X** suffix appended to the TI part number. For example, 2512737-0001X.
2. See Table 3, for DLPC347x resolutions on the DMD supported per part number.

12.1.3 Video Timing Parameter Definitions

Active Lines Per Frame (ALPF) Defines the number of lines in a frame containing displayable data: ALPF is a subset of the TLPF.

Active Pixels Per Line (APPL) Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL.

Horizontal Back Porch (HBP) Blanking Number of blank pixel clocks after horizontal sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal.

Horizontal Front Porch (HFP) Blanking Number of blank pixel clocks after the last active pixel but before Horizontal Sync.

Horizontal Sync (HS) Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.

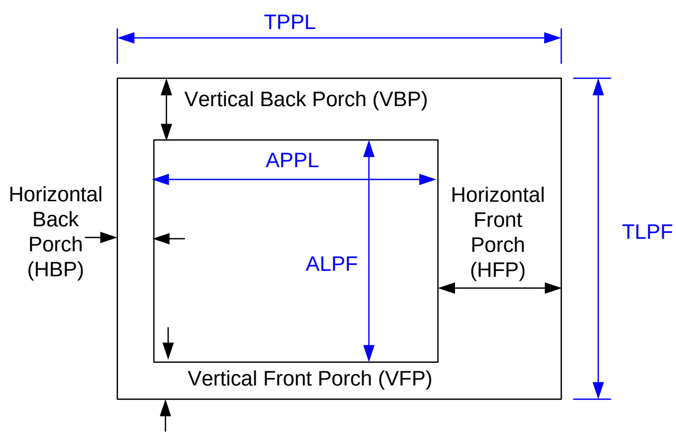
Total Lines Per Frame (TLPF) Defines the vertical period (or frame time) in lines: TLPF = Total number of lines per frame (active and inactive).

Total Pixel Per Line (TPPL) Defines the horizontal line period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).

Vertical Sync (VS) Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.

Vertical Back Porch (VBP) Blanking Number of blank lines after the leading edge of vertical sync but before the first active line.

Vertical Front Porch (VFP) Blanking Number of blank lines after the leading edge of the last active line but before vertical sync.



12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 17. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLPA2000	Click here	Click here	Click here	Click here	Click here
DLPA2005	Click here	Click here	Click here	Click here	Click here
DLPA3000	Click here	Click here	Click her	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

IntelliBright, E2E are trademarks of Texas Instruments.
DLP is a registered trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC3478CZEZ	ACTIVE	NFBGA	ZEZ	201	160	TBD	Call TI	Call TI	-30 to 85		Samples
XDLPC3478CZEZ	ACTIVE	NFBGA	ZEZ	201	160	TBD	Call TI	Call TI	-30 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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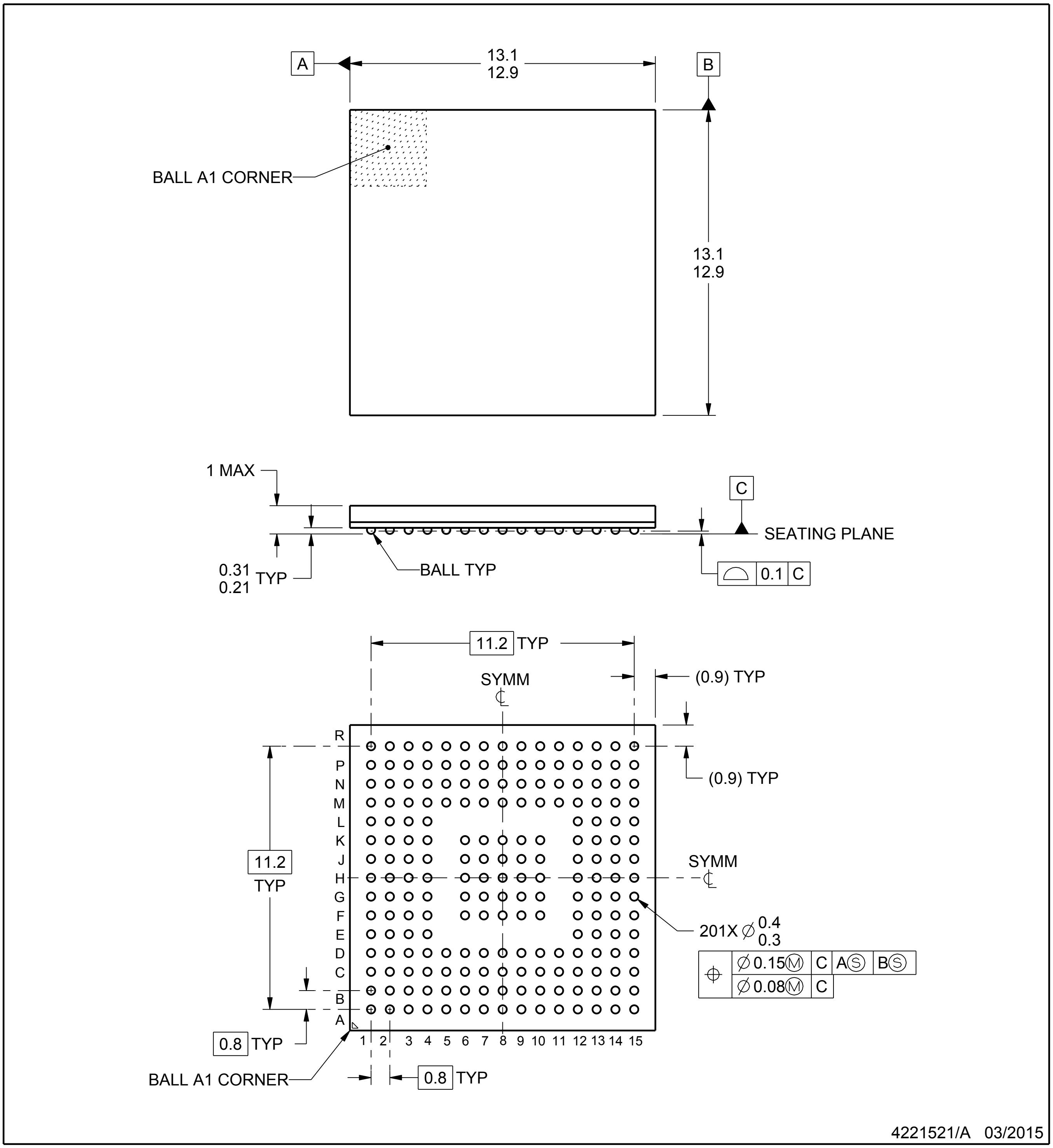
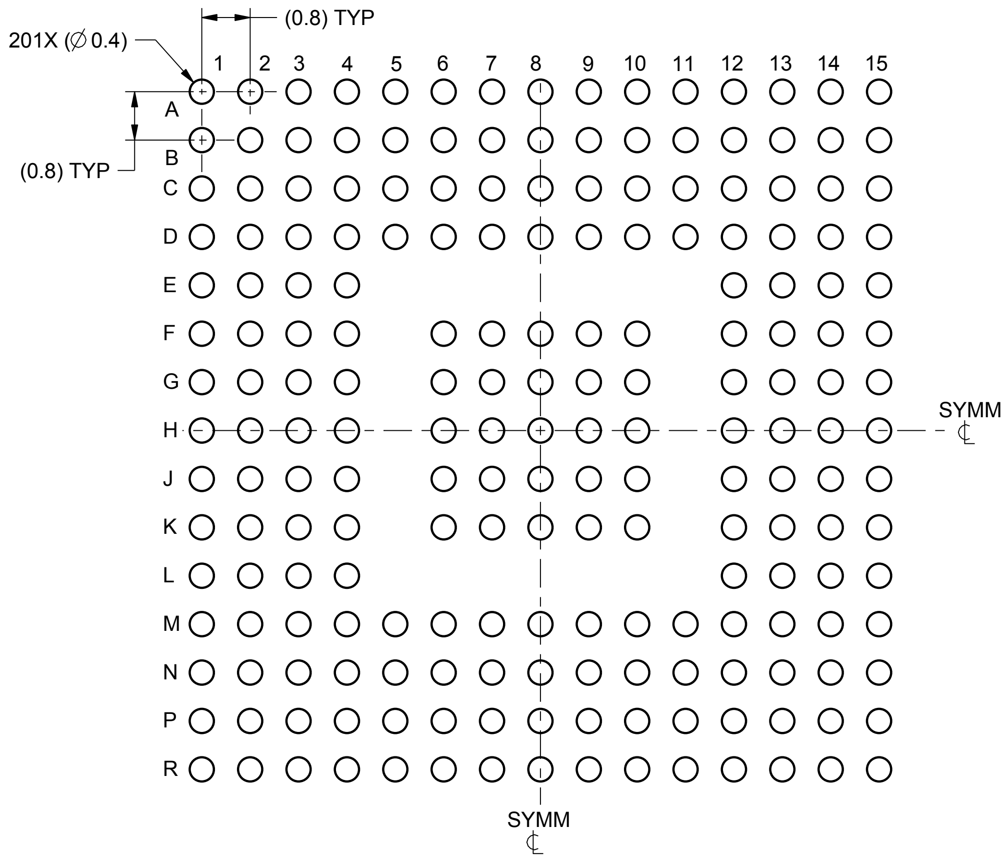
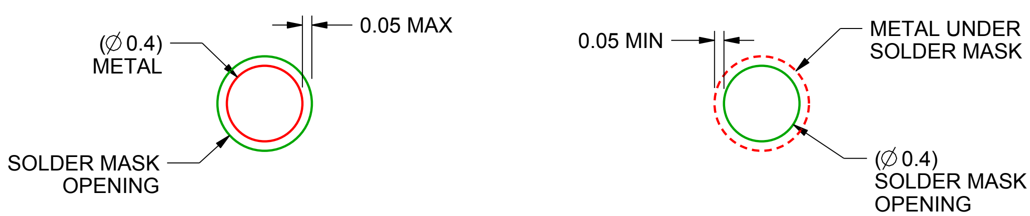


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X



NON-SOLDER MASK DEFINED (PREFERRED)

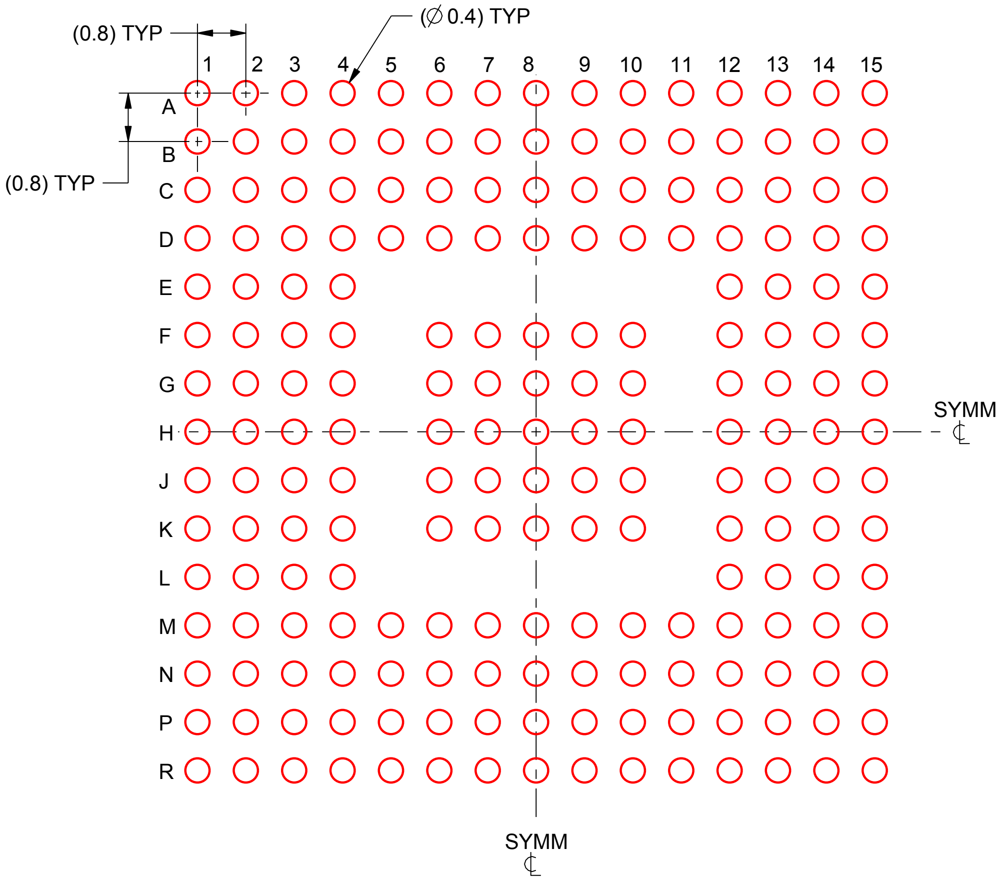
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221521/A 03/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4221521/A 03/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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