National Semiconductor

54LS169/DM54LS169A/DM74LS169A Synchronous 4-Bit Up/Down Binary Counter

General Description

This synchronous presettable counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs all change at the same time when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising edge of the clock waveform.

This counter is fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry outputs. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up, and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

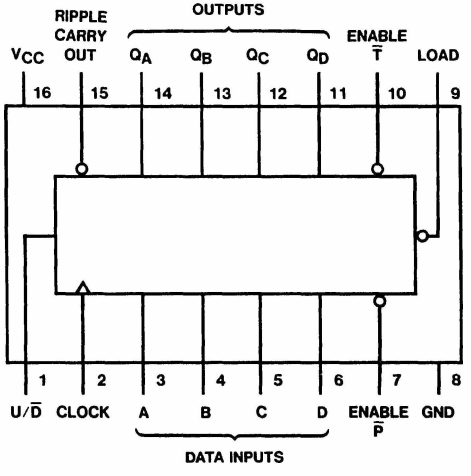
This counter features a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down), which modify the operating mode, have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Fully synchronous operation for counting and programming.
- Internal look-ahead for fast counting.
- Carry output for n-bit cascading.
- Fully independent clock circuit
- Alternate Military/Aerospace device (54LS169) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6401–1

Order Number 54LS169DMQB, 54LS169FMQB, 54LS169LMQB, DM54LS169AJ, DM54LS169AW, DM74LS169AM or DM74LS169AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS169A			DM74LS169A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Clock Pulse Width (Note 3)		25			25			ns
t_{SU}	Setup Time (Note 3)	Data	20			20			ns
		Enable $\overline{T}$ or $\overline{P}$	20			20			
		Load	25			25			
		U/D	30			30			
t_H	Hold Time (Note 3)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable $\overline{T}$			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable $\overline{T}$			40	μA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable $\overline{T}$			−0.8	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			20	34	mA

Note 4: All typicals are at V_{CC} = 5V and T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

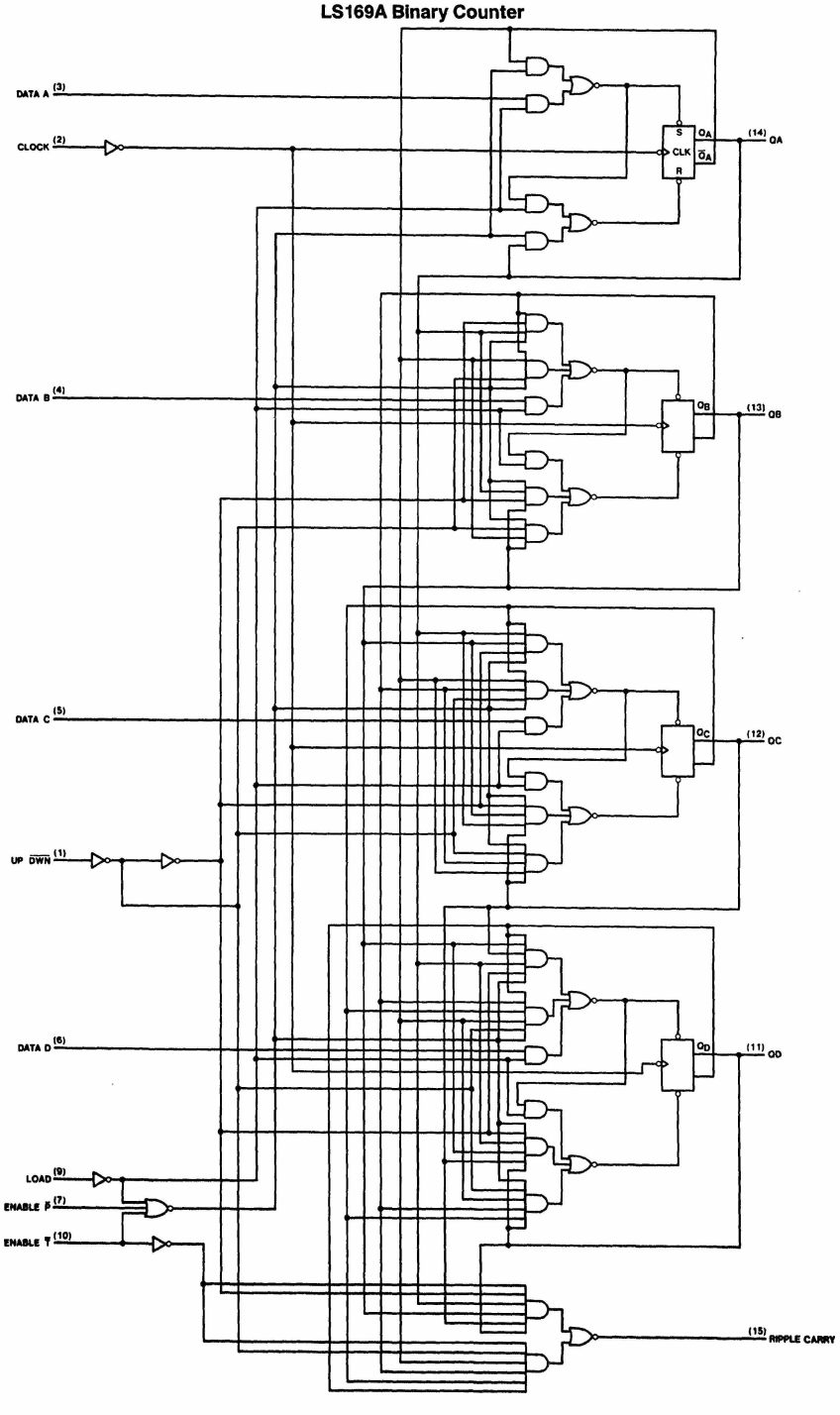
Note 6: I_{CC} is measured after a momentary 4.5V, then ground, is applied to the CLOCK with all other inputs grounded and all the outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		35		39	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		23		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable $\overline{T}$ to Ripple Carry		18		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable $\overline{T}$ to Ripple Carry		18		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Up/Down to Ripple Carry (Note 1)		25		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Up/Down to Ripple Carry (Note 1)		29		38	ns

Note 1: The propagation delay from UP/DOWN to RIPPLE CARRY must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum, the ripple carry output transition will be in phase. If the count is maximum, the ripple carry output will be out of phase.

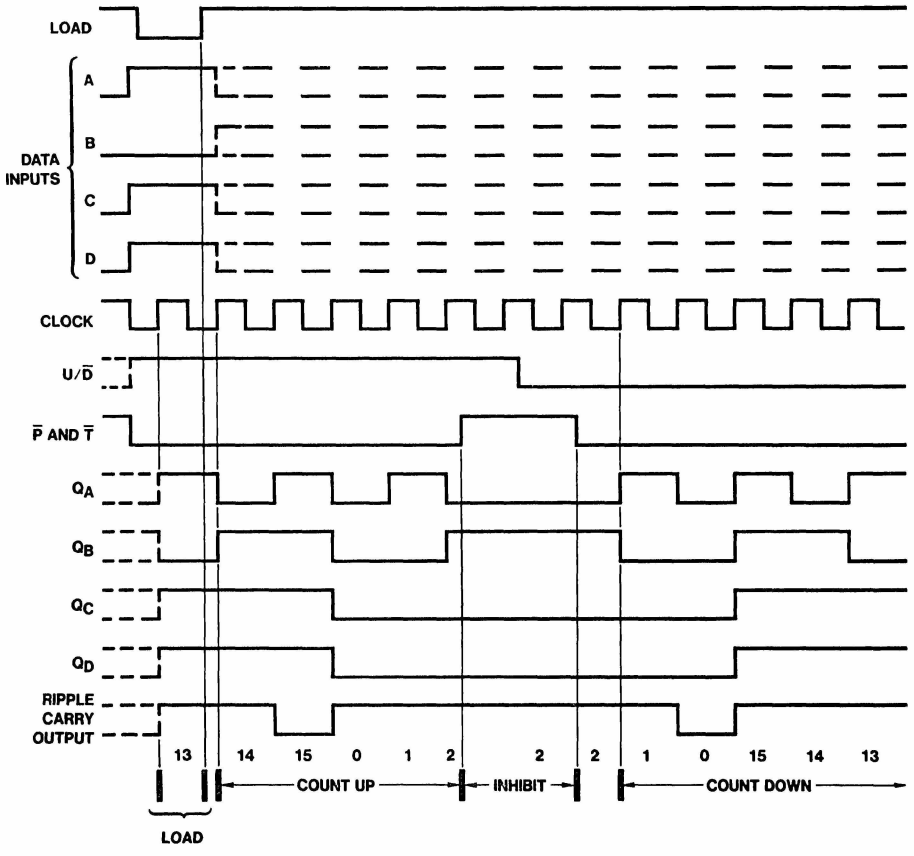
Logic Diagram



TL/F/6401–2

Timing Diagram

LS169A Binary Counters
Typical Load, Count, and Inhibit Sequences



TL/F/6401–3