National Semiconductor

54LS193/DM54LS193/DM74LS193 Synchronous 4-Bit Up/Down Binary Counters with Dual Clock

General Description

This circuit is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is held high.

The counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows.

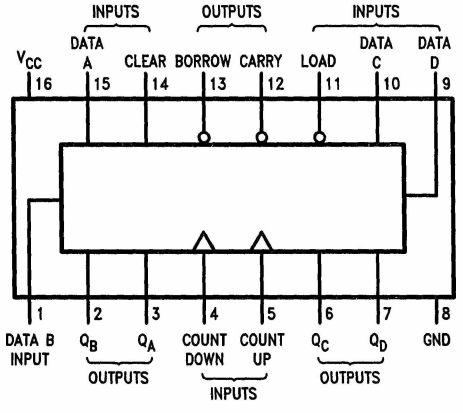
Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop
- Alternate Military/Aerospace device (54LS193) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



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Order Number 54LS193DMQB, 54LS193FMQB, 54LS193LMQB, DM54LS193J, DM54LS193W, DM74LS193M or DM74LS193N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65° C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS193			DM74LS193			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
f_{CLK}	Clock Frequency (Note 1)	0		25	0		25	MHz
	Clock Frequency (Note 2)	0		20	0		20	MHz
t_W	Pulse Width of Any Input (Note 6)	20			20			ns
t_{SU}	Data Setup Time (Note 6)	20			20			ns
t_H	Data Hold Time (Note 6)	0			0			ns
t_{REL}	Release Time (Note 6)	40			40			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			19	34	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, I_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, I_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

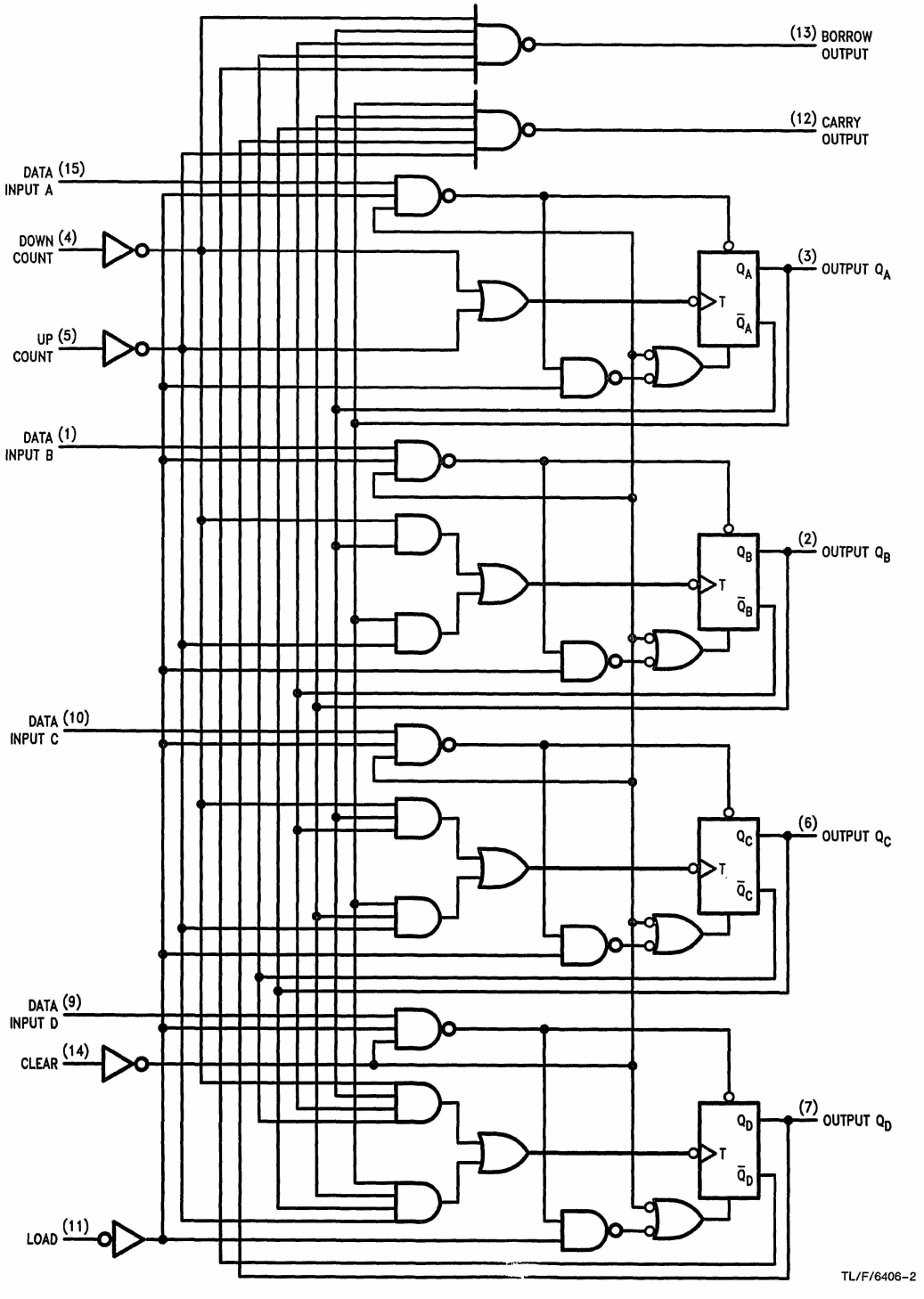
Note 5: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

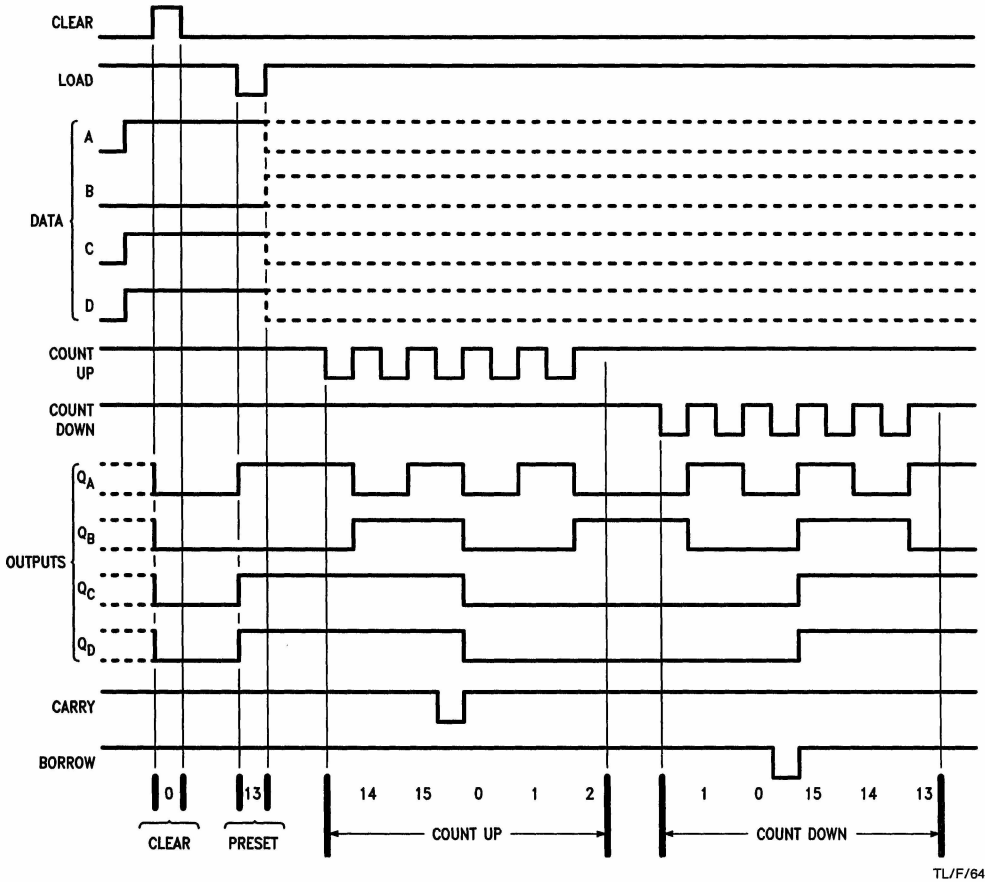
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Up to Carry		26		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Up to Carry		24		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Down to Borrow		24		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Down to Borrow		24		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Either Count to Any Q		38		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Either Count to Any Q		47		54	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		40		41	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		40		47	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		35		44	ns

Logic Diagram



Timing Diagrams

Typical Clear, Load, and Count Sequences



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Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.