National Semiconductor

DM54LS75/DM74LS75 Quad Latches

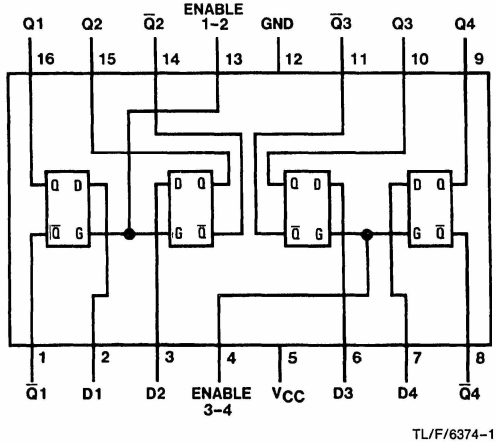
General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occured) is retained at the Q output until the enable is permitted to go high.

These latches feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in 16-pin packages.

Connection Diagram

Dual-In-Line Package



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Order Number DM54LS75J, DM54LS75W, DM74LS75M or DM74LS75N
See NS Package Number J16A, M16A, N16A or W16A

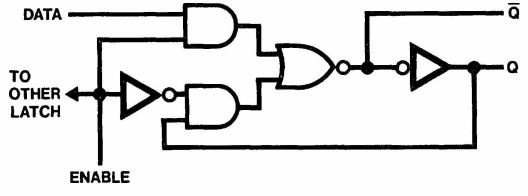
Function Table (Each Latch)

Inputs		Outputs	
D	Enable	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level, L = Low Level, X = Don't Care

Q_0 = The Level of Q Before the High-to-Low Transition of ENABLE

Logic Diagram (Each Latch)



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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS75			DM74LS75			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
t_W	Enable Pulse Width (Note 4)	20			20			ns
t_{SU}	Setup Time (Note 4)	20			20			ns
t_H	Hold Time (Note 4)	0			0			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.5		V
			DM74	2.7	3.5		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	D			0.1	mA
			Enable			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	D			20	μA
			Enable			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	D			−0.4	mA
			Enable			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.3	12	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Q		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Q		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to $\overline{Q}$		20		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to $\overline{Q}$		15		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Q		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Q		25		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to $\overline{Q}$		30		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to $\overline{Q}$		15		20	ns