National Semiconductor

DM54S181/DM74S181 Arithmetic Logic Unit/Function Generators

General Description

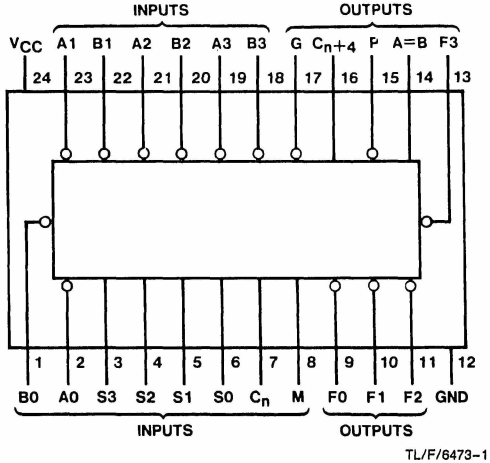
These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM54S182/DM74S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading 182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54S182/DM74S182. (Continued)

Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words

Connection Diagram

Dual-In-Line Package



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Order Number DM54S181J or DM74S181N
See NS Package Number J24A or N24A

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
C_n+4	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

General Description (Continued)

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to provide A—B.

The S181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requriements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The DM54S181/DM74S181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table I; those obtained with the signal designations of *Figure 2* are given in Table II.

Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table I)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_n+4$	X	Y
Active-Low Data (Table II)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_n+4	$\overline{P}$	$\overline{G}$

Input C_n	Output C_n+4	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A ≤ B	A ≤ B
H	L	A ≤ B	A ≤ B
L	H	A ≤ B	A ≤ B
L	L	A ≤ B	A ≤ B

General Description (Continued)

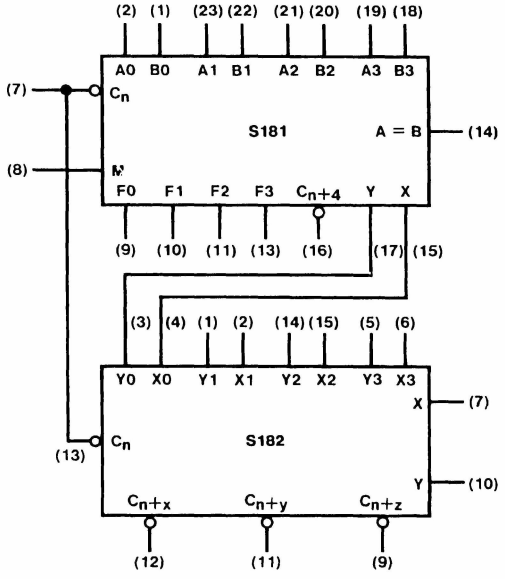

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FIGURE 1

TABLE I

Selection				Active High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A Plus 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	F = $\overline{AB}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F = A ⊕ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

General Description (Continued)

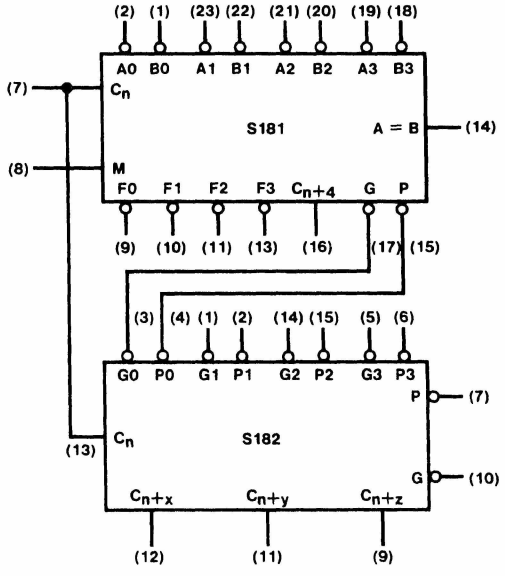

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FIGURE 2

TABLE II

Selection				Active Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A ⊕ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage (A = B Output)	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S181			DM74S181			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (A = B Output)			5.5			5.5	V
I_{OH}	High Level Output Current (All Except A = B)			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{CEX}	High Level Output Current (A = B Output)	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OH}	High Level Output Voltage (All Except A = B)	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Mode			50	μA
			A or B			150	
			S			200	
			Carry			250	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	Mode			−2	mA
			A or B			−6	
			S			−8	
			Carry			−10	
I_{OS}	Short Circuit Output Current (Any Output Except A = B)	V_{CC} = Max (Note 2)		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			120	220	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured for the following conditions: A. S0 through S3, M, and A inputs at 4.5V, all other inputs grounded and all outputs open. B. S0 through S3 and M inputs at 4.5V, all other inputs grounded and all outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM54/74 S181				Units
					R_L = 280Ω, C_L = 15 pF		R_L = 280Ω, C_L = 50 pF		
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		C_n	C_n+4		10.5		14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					10.5		14	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any A or B	C_n+4		18.5		22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					18.5		22	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	C_n+4		23		27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					23		27	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V ($\overline{SUM}$ or $\overline{DIFF}$ mode)	C_n	Any F		12		14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12		14	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any A or B	G		12		15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12		15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	G		15		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					15		20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any A or B	P		12		15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12		15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	P		15		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					15		20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	A_i or B_i	F_i		16.5		20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					16.5		20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	A_i or B_i	F_i		20		24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					22		24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 4.5V (logic mode)	A_i or B_i	F_i		20		24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					22		24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	A = B		23		26	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					30		33	

Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase

$\overline{SUM}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

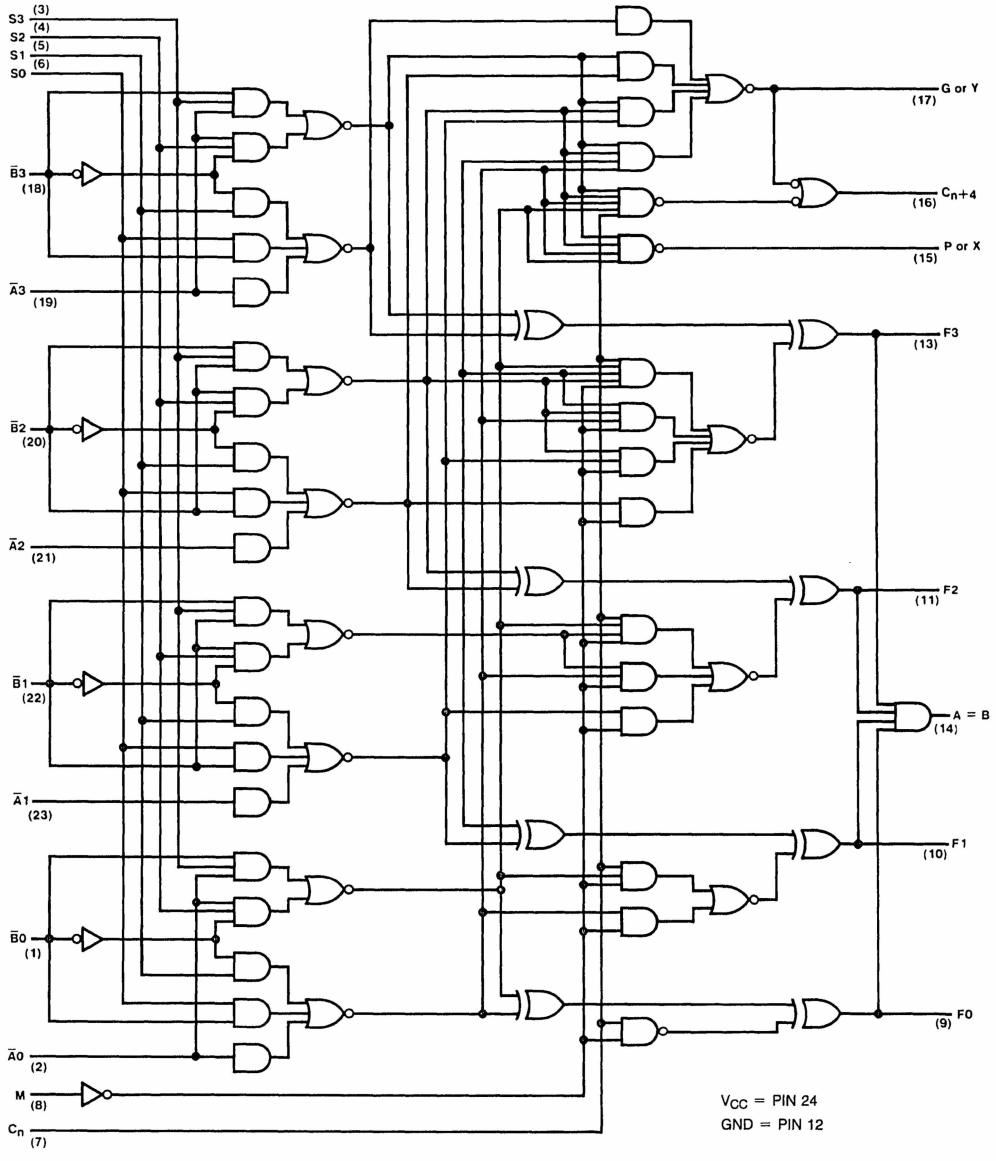
Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A	All B	Any F or C_n+4	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase

Parameter Measurement Information (Continued)

$\overline{DIFF}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A and B	None	C_n+4 or any F	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_n+4	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_n+4	In-Phase

Logic Diagram



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