National Semiconductor

DM7136 6-Bit Unified Bus Comparator with Open-Collector Outputs

General Description

The DM7136 compares two binary words of two-to-six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high-impedance receivers driven by a terminated data bus. These bus inputs include 0.65V typical hysteresis which provides 1.4V noise immunity. The DM7136 has open-collector outputs which go to the high state upon equality and is expandable to n bits by collector-ORing. The device has an output latch which is strobe controlled.

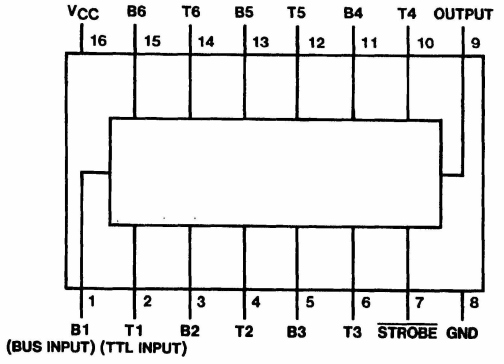
The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logic "1" to a logic "0" state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logic "1" level, without affecting the state of the output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

Features

- Low bus input current 15 μA typ
- High bus input noise immunity 1.4V typ
- Bus inputs comply with IEEE 488-1975
- TTL-compatible output
- Output latch provision

Connection Diagram

Dual-In-Line Package



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Order Number DM7136J or DM7136W
See NS Package Number J16A or W16A

Function Table

Condition	$\overline{\text{STROBE}}$	Output
		DM71/8136
T = B, T ≠ B	H	Q_{N-1}*
T = B	L	H
T ≠ B	L	L

*Latched in previous state.

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM71	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7136			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{T+}	Positive-Going Input Threshold Voltage for Bus Inputs (Note 1)	1.4	1.75	2	V
V_{T-}	Negative-Going Input Threshold Voltage for Bus Inputs (Note 1)	0.9	1.1	1.35	V
V_{IH}	High Level Input Voltage for TTL and Strobe Inputs	2			V
V_{IL}	Low Level Input Voltage for TTL and Strobe Inputs			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	TTL			1	mA
			Strobe			2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	TTL			40	μA
			Strobe			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	TTL			−1.6	mA
			Strobe			−2.4	
I_{IN}	Bus Input Current	V_I = 4V	V_{CC} = Max		15	50	μA
			V_{CC} = 0V		1	50	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	74	mA

Note 1: V_{CC} = 5V.

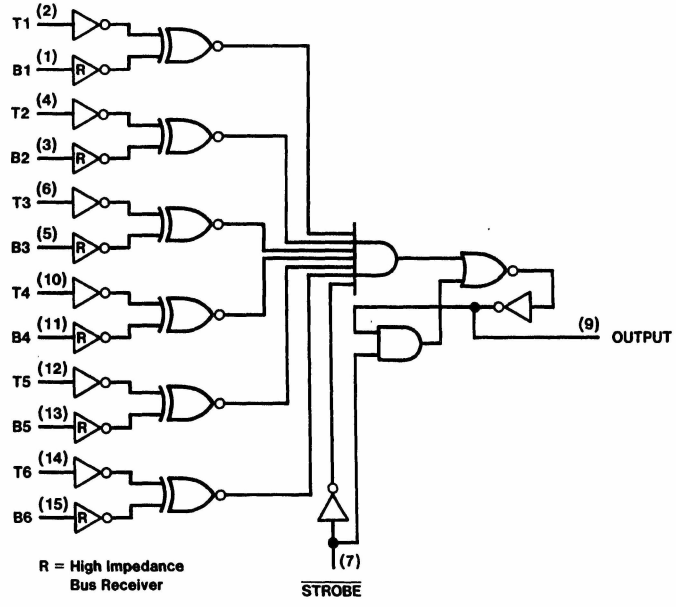
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	TTL to Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	TTL to Output		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Bus to Output		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Bus to Output		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		30	ns

Logic Diagram



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