



54165/DM74165

8-Bit Parallel-to-Serial Converter

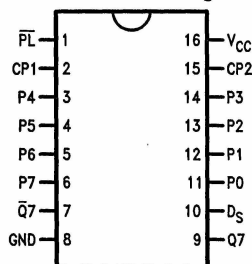
General Description

The '165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputting occurs asynchronously when the Parallel Load ($\overline{PL}$) input is LOW. With $\overline{PL}$ HIGH, serial shifting occurs on

the rising edge of the clock; new data enters via the Serial Data (D_S) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

Connection Diagram

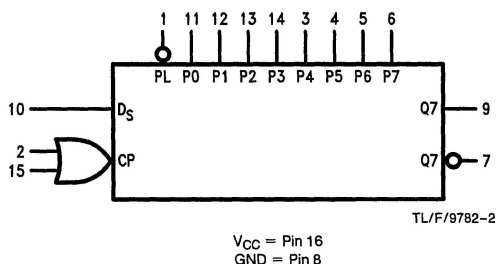
Dual-In-Line-Package



TL/F/9782-1

Order Number 54165DMQB, 54165FMQB or DM74165N
See NS Package Number J16A, N16E or W16A

Logic Symbol



Pin Names	Description
CP1, CP2	Clock Pulse Inputs (Active Rising Edge)
D_S	Serial Data Input
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P0-P7	Parallel Data Inputs
Q7	Serial Output from Last Stage
$\overline{Q7}$	Complementary Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54165			DM74165			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.8			0.8	V
I _{OH}	High Level Output Current			−0.8			−0.8	mA
I _{OL}	Low Level Output Current			16			16	mA
T _A	Free Air Operating Temperature	−55		125	0		70	°C
t _s (H) t _s (L)	Setup Time HIGH or LOW P _n to PL	10 10			10 10			ns
t _h (H) t _h (L)	Hold Time HIGH or LOW P _n to PL	10 10			0 0			ns
t _s (H) t _s (L)	Setup Time HIGH or LOW D _S to CP _n	20 20			20 20			ns
t _h (H) t _h (L)	Hold Time HIGH or LOW D _S to CP _n	0 0			0 0			ns
t _s (H)	Setup Time HIGH CP1 to CP2 or CP2 to CP1	30			30			ns
t _w (H)	CP _n Pulse Width HIGH	25			25			ns
t _w (L)	PL Pulse Width LOW	15			15			ns
t _{rec}	Recovery Time, PL to CP _n	45			45			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = −12 mA			−1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max, V _{IL} = Max	2.4	3.4		V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, V _{IH} = Min		0.2	0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.4V	PL		80	μA
			Inputs		40	
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V	PL		−3.2	mA
			Inputs		−1.6	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	54	−20	−55	mA
			DM74	−18	−55	
I _{CC}	Supply Current	V _{CC} = Max, PL =  P _n =  , CP ₁ , CP ₂ = 4.5V			63	mA

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25^{\circ}C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C _L = 15 pF R _L = 400Ω		Units
		Min	Max	
f _{max}	Maximum Clock Frequency	20		MHz
t _{PLH} t _{PHL}	Propagation Delay P _L to Q7 or $\overline{Q}$ 7		31 40	ns
t _{PLH} t _{PHL}	Propagation Delay CP1 to Q7 or $\overline{Q}$ 7		24 31	ns
t _{PLH} t _{PHL}	Propagation Delay P7 to Q7		17 36	ns
t _{PLH} t _{PHL}	Propagation Delay P7 to $\overline{Q}$ 7		27 27	ns

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Note 2: Not more than one output should be shorted at a time.

Functional Description

The '165 contains eight clocked master/slave RS flip-flops connected as a shift register with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the $\overline{PL}$ signal is LOW. The parallel data can change while $\overline{PL}$ is LOW provided that the recommended setup and hold times are observed.

For clocked operation, $\overline{PL}$ must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit.

by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

Truth Table

$\overline{\text{PL}}$	CP		Contents								Response
	1	2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	X	X	P0	P1	P2	P3	P4	P5	P6	P7	Parallel Entry
H	L		D _S	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Right Shift
H	H		Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	No Change
H		L	D _S	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Right Shift
H		H	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	No Change

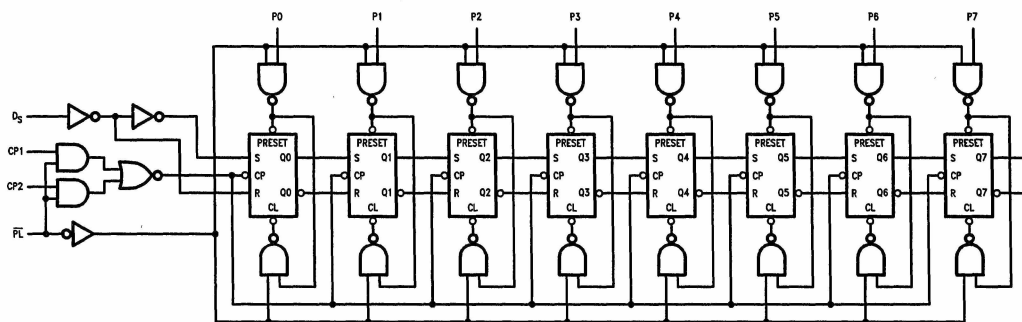
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

 = Positive Rising Edge

Logic Diagram



TL/F/9782-3