



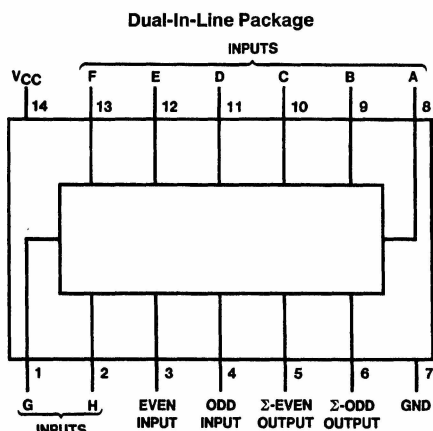
DM54180/DM74180 9-Bit Parity Generators/Checkers

General Description

These universal 9-bit (8 data bits plus 1 parity bit) parity generators/checkers feature odd/even outputs and control inputs to facilitate operation in either odd or even parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd input can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs.

Connection Diagram



TL/F/6559-1

Order Number DM54180J, DM54180W or DM74180N
See NS Package Number J14A, N14A or W14B

Function Table

Inputs			Outputs	
Σ of H's at A thru H	Even	Odd	Σ Even	Σ Odd
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 7V

Input Voltage 5.5V

Operating Free Air Temperature Range

DM54 -55°C to +125°C

DM74 0°C to +70°C

Storage Temperature Range -65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54180			DM74180			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.8			0.8	V
I _{OH}	High Level Output Current			-0.8			-0.8	mA
I _{OL}	Low Level Output Current			16			16	mA
T _A	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -12 mA			-1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min	2.4			V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min, V _{IL} = Max			0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max V _I = 2.4V	Odd or Even		80	μA
			Data		40	
I _{IL}	Low Level Input Current	V _{CC} = Max V _I = 0.4V	Odd or Even		-3.2	mA
			Data		-1.6	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	DM54	-20	-55	mA
			DM74	-18	-55	
I _{CC}	Supply Current	V _{CC} = Max (Note 3)	DM54		34	mA
			DM74		34	
					56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

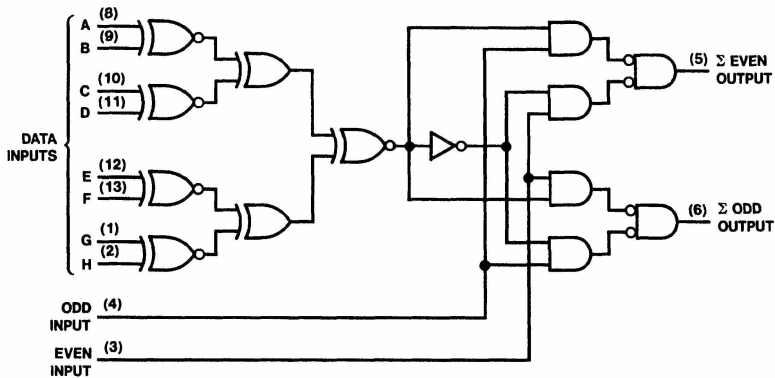
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with EVEN and ODD inputs at 4.5V, all other inputs and outputs open.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Even	$C_L = 15\text{ pF}$ $R_L = 400\Omega$ Odd Input Low		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Even			68	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Odd			48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Odd			38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Even	$C_L = 15\text{ pF}$ $R_L = 400\Omega$ Odd Input High		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Even			38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Odd			60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Odd			68	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Even or Odd to Σ Even or Σ Odd	$C_L = 15\text{ pF}$ $R_L = 400\Omega$		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Even or Odd to Σ Even or Σ Odd			10	ns

Logic Diagram



TL/F/6559-2