National Semiconductor

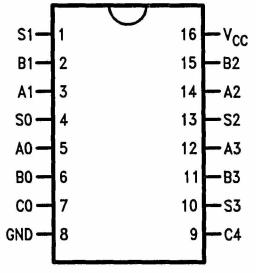
54283/DM74283
4-Bit Binary Full Adder (with Fast Carry)

General Description

The '283 high speed 4-bit binary full adders with internal carry lookahead accept two 4-bit binary words (A0–A3, B0–B3) and a Carry input (C0). They generate the binary Sum outputs (S0–S3) and the Carry output (C4) from the most significant bit. They operate with either active HIGH or active LOW operands (positive or negative logic).

Connection Diagram

Dual-In-Line Package



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Order Number 54283DMQB, 54283FMQB or DM74283N
See NS Package Number J16A, N16E or W16A

Pin Names	Description
A0–A3	A Operand Inputs
B0–B3	B Operand Inputs
C0	Carry Input
S0–S3	Sum Outputs
C4	Carry Output

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54283			DM74283			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current at S_n	V_{CC} = Max (Note 2)	54	−20		−55	mA
			DM74	−20		−55	
I_{OS}	Short Circuit Output Current at C4	V_{CC} = Max (Note 2)	54	−20		−70	mA
			DM74	−18		−70	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max	54			99	mA
			DM74			110	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF, R_L = 400Ω		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C0 or S_n		21 21	ns
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to S_n		24 24	ns
t_{PLH} t_{PHL}	Propagation Delay C0 to C4		14 16	ns
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C4		14 16	ns

Functional Description

The '283 adds two 4-bit binary words (A plus B) plus the incoming carry C0. The binary sum appears on the Sum (S0–S3) and outgoing carry (C4 outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

2^0 (A0 + B0 + C0) + 2^1 (A1 + B1) + 2^2 (A2 + B2) + 2^3 (A3 + B3) = S0 + 2S1 + 4S2 + 8S3 + 16C4

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C0, A0, B0 can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the '283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that if C0 is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Example:

	C0	A0	A1	A2	A3	B0	B1	B2	B3	S0	S1	S2	S3	C4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16 Active LOW: 1 + 5 + 6 = 12 + 0

Due to pin limitations, the intermediate carries of the '283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. *Figure a* shows a way of making a 3-bit adder. Tying the operand inputs of the fourth adder (A3, B3) LOW makes S3 dependent ony on, and equal to, the carry from the third adder. Using somewhat the same principle,*Figure b* shows a way of dividing the '283 into a 2-bit and a 1-bit adder. The third stage adder (A2, B2, S2) is used merely as a means of getting a carry (C10) signal into the fourth stage (via A2 and B2) and bringing out the carry from the second stage on S2. Note that as long as A2 and B2 are the same, whether HIGH or LOW, they do not infuence S2. Similarly, when A2 and B2 are the same the carry into the third stage does not influence they carry out of the third stage. *Figure c* shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S0, S1 and S2 present a binary number equal to the number of inputs I1–I5 that are true. *Figure d* shows one method of implementing a 5-input majority gate. When three or more of the inputs I1–I5 are true, the output M5 is true.

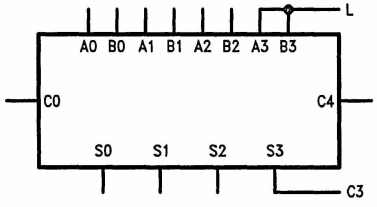

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FIGURE a. 3-Bit Adder

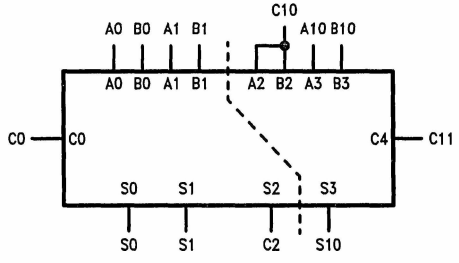

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FIGURE b. 2-Bit and 1-Bit Adders

Functional Description (Continued)

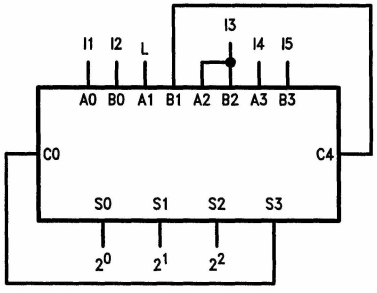

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FIGURE c. 5-Input Encoder

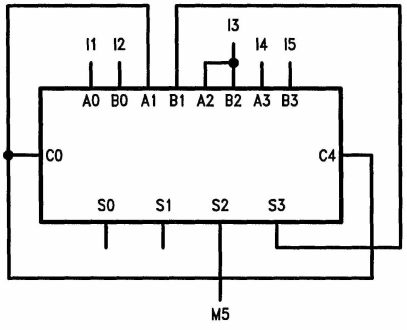

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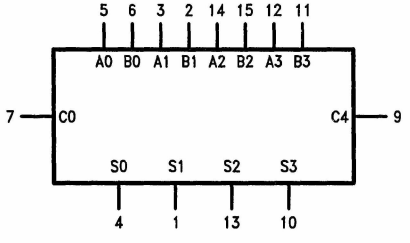
FIGURE d. 5-Input Majority Gate

Logic Symbol



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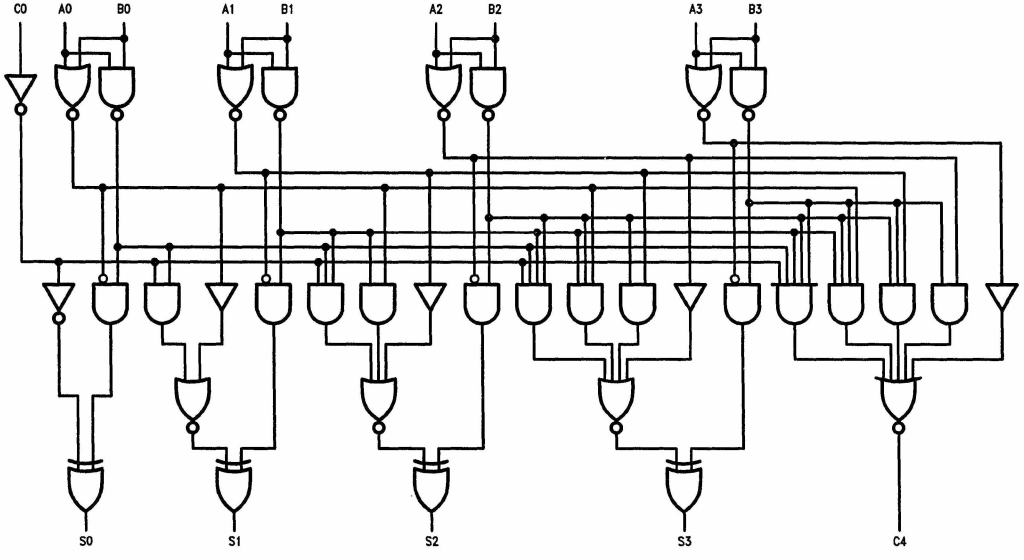
V_{CC} = Pin 16
GND = Pin 8

Logic Diagram



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