TTL MSI

DM5495/DM7495(SN5495/SN7495)
4-bit right-shift left-shift register

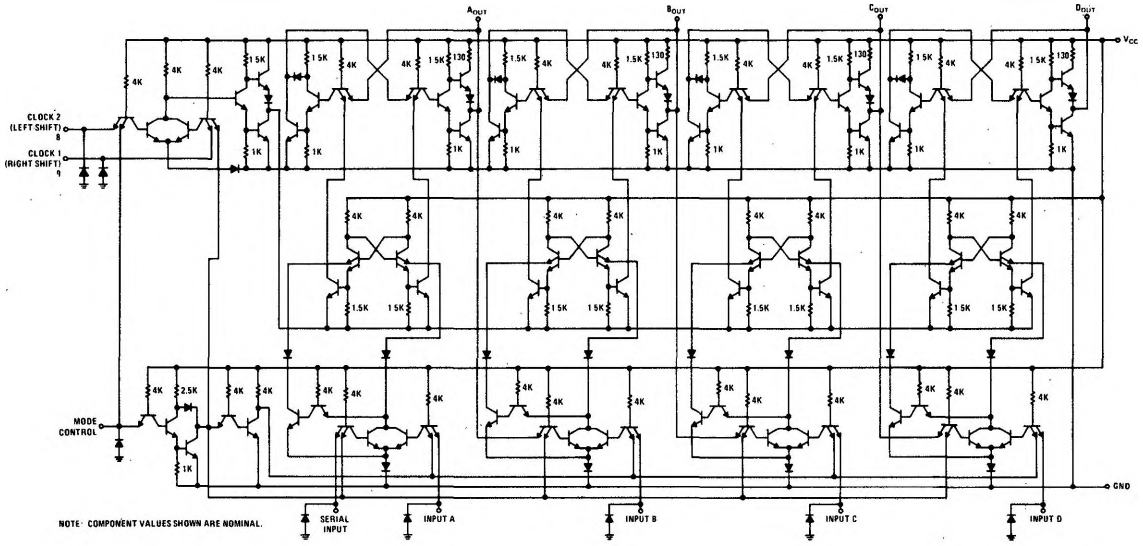
general description

The DM5495/DM7495 is a TTL (Transistor-Transistor Logic) monolithic four-bit parallel-in parallel-out shift register employing four R-S master-slave flip flops, internal clock buffers and control gating for either right-shift or left-shift operation. Separate clocks are provided for right-shift and left-shift operation. A mode control input enables right-shift or left-shift operation, depending on whether its input is a zero or one respectively. Data transfer occurs on the negative transition of the clock pulse. The three modes of operation are explained on page 4.

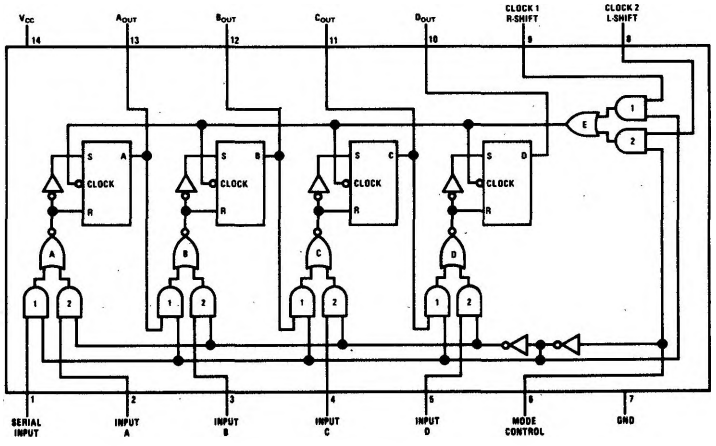
Features include:

- Input Clamping Diodes
- Typical Noise Immunity 1.0V
- High Clock Rate 35 MHz

schematic diagram



logic and connection diagram



absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Operating Temperature Range	DM5495	−55°C to +125°C
	DM7495	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5495	V_{CC} = 4.5V	2			V
	DM7495	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM5495	V_{CC} = 4.5V			0.8	V
	DM7495	V_{CC} = 4.75				
Logical "1" Output Voltage	DM5495	V_{CC} = 4.5V	2.4			V
	DM7495	V_{CC} = 4.75V, I_{load} = −400 μA				
Logical "0" Output Voltage	DM5495	V_{CC} = 4.5V			0.4	V
	DM7495	V_{CC} = 4.75V, I_{sink} = 16 mA				
Logical "0" Input Current (at any Input Except Mode Control)	DM5495	V_{CC} = 5.5V			−1.6	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 0.4V				
Logical "0" Input Current at Mode Control	DM5495	V_{CC} = 5.5V			−3.2	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 0.4V				
Logical "1" Input Current (at any Input Except Mode Control)	DM5495	V_{CC} = 5.5V			40	μA
	DM7495	V_{CC} = 5.25V, V_{IN} = 2.4V				
	DM5495	V_{CC} = 5.5V			1	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 5.5V				
Logical "1" Input Current at Mode Control	DM5495	V_{CC} = 5.5V			80	μA
	DM7495	V_{CC} = 5.25V, V_{IN} = 2.4V				
	DM5495	V_{CC} = 5.5V			1	mA
	DM7495	V_{CC} = 5.25V, V_{IN} = 5.5V				
Short-Circuit Output Current (Note 2)	DM5495	V_{CC} = 5.5V	−18		−57	mA
	DM7495	V_{CC} = 5.25V				
Supply Current	DM5495	V_{CC} = 5.5V		50	80	mA
	DM7495	V_{CC} = 5.25V				
Input Diode Clamp Voltage		T_A = 25°C, I_{IN} = −12 mA, V_{CC} = 5.0V			−1.5	V

switching characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Shift Frequency	C_L = 50 pF, R_L = 400Ω	20	35		MHz
Propagation Delay Time to Logical "1" Level from Clock 1 or 2 to Outputs	C_L = 50 pF, R_L = 400Ω		26	35	ns
Propagation Delay Time to Logical "0" from Clock 1 or 2 to Outputs	C_L = 50 pF, R_L = 400Ω		24	35	ns

Note 1: Min/Max limits apply across the guaranteed operating temperature range of −55°C to +125°C for the DM5495 and 0°C to 70°C for the DM7495 unless otherwise specified. All typicals are given for T_A = 25°C and V_{CC} = 5.0V.

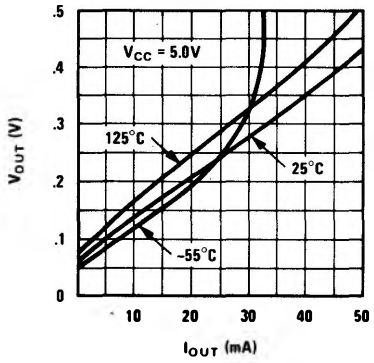
Note 2: Not more than one output should be shorted at a time.

recommended operating conditions

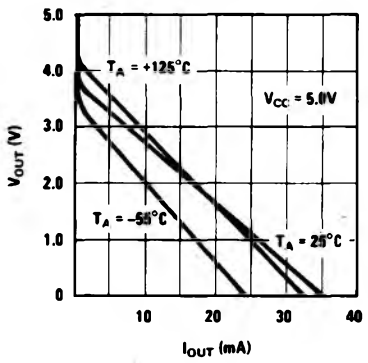
OPERATING CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	DM5495	4.5	5	5.5	V
	DM7495	4.75	5	5.25	V
Clock Pulse Width, $t_{p\ (clock)}$		15	10		ns
Setup Time Required at Serial, A,B,C, or D Inputs, t_{setup}		20	10		ns
Hold Time Required at Serial, A,B,C, or D Inputs, t_{hold}		0	-10		ns
Logical "0" Level Setup Time Required at Mode Control $t_{A(0)}$ (With Respect to Clock 1 Input)		20			ns
Logical "1" Level Setup Time Required at Mode Control $t_{B(1)}$ (With Respect to Clock 2 Input)		15			ns
Logical "0" Level Setup Time Required at Mode Control $t_{C(0)}$ (With Respect to Clock 2 Input)		10			ns
Logical "1" Level Setup Time Required at Mode Control $t_{D(1)}$ (With Respect to Clock 1 Input)		10			ns

typical performance characteristics

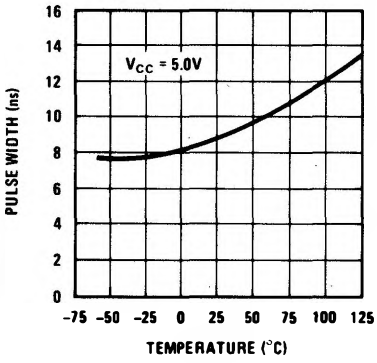
Logical "0" Output Voltage vs Sink Current



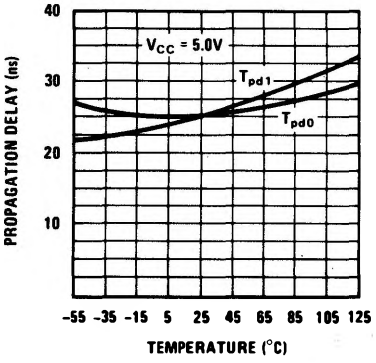
Logical "1" Output Voltage vs Source Current



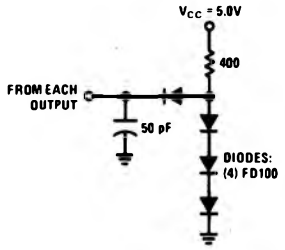
Minimum Clock Pulse Width vs Temperature



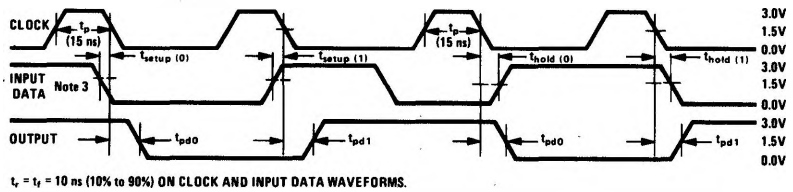
Propagation Delay Times vs Temperature



ac test circuit



switching time waveforms



$t_r = t_f$ = 10 ns (10% to 90%) ON CLOCK AND INPUT DATA WAVEFORMS.

Note 3: Input data is applied to serial input when mode control equals a logical zero. Input data is applied to input A, B, C, or D, when mode control equals a logical one.