National Semiconductor

54LS192/DM74LS192 Up/Down Decade Counter with Separate Up/Down Clocks

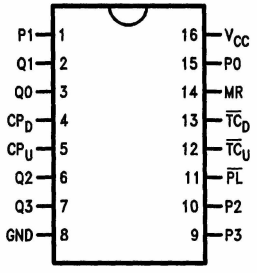
General Description

The 'LS192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

Connection Diagram

Dual-In-Line Package



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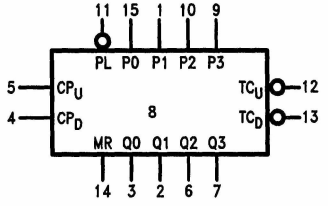
Order Number 54LS192DMQB, 54LS192FMQB, 54LS192LMQB, DM74LS192M or DM74LS192N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
CP_U	Count Up Clock Input (Active Rising Edge)
CP_D	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset Input (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P0–P3	Parallel Data Inputs
Q0–Q3	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

Mode Select Table

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↑	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS192			DM74LS192			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Voltage			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW Pn to $\overline{PL}$	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW Pn to $\overline{PL}$	3 3			3 3			ns
t_w (L)	CP Pulse Width LOW	17			17			ns
t_w (L)	$\overline{PL}$ Pulse Width LOW	20			20			ns
t_w (H)	MR Pulse Width HIGH	15			15			ns
t_{rec}	Recovery Time, MR to CP	3			3			ns
t_{rec}	Recovery Time, $\overline{PL}$ to CP	10			10			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max,	54LS			0.4	V
		V_{IH} = Min	DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, MR, $\overline{PL}$ = GND, Other Inputs = 4.5V				31	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characterisitcs

V_{CC} = +0.5V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	R_L = 2k, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Count Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		31 28	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U to $\overline{TC}_U$		16 21	ns
t_{PLH} t_{PHL}	Propagation Delay CP_D to $\overline{TC}_D$		16 24	
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		20 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		32 30	ns
t_{PHL}	Propagation Delay, MR to Q_n		25	

Functional Description

The '192 is an asynchronously presettable decade and 4-bit binary synchronous up/down (reversible) counter. The operating modes of the '192 decade counter and the '193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagram. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up, and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

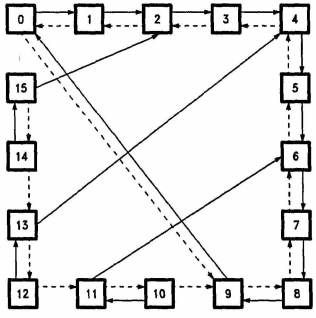
The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the '192, 15 for the '193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q0 \bullet Q3 \bullet \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}0 \bullet \overline{Q}1 \bullet \overline{Q}2 \bullet \overline{Q}3 \bullet \overline{CP}_D$$

Each circuit has an asynchronous parallel load capability permitting the counter to be reset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P0–P3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

State Diagram



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Logic Diagram