

DM54LS240,DM54LS241,DM74LS240,DM74LS241

DM54LS240 DM54LS241 DM74LS240 DM74LS241 Octal TRI-STATE(RM) Buffers/Line Drivers/Line Receivers



Literature Number: SNOS292A

DM54LS240/DM74LS240, DM54LS241/DM74LS241 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

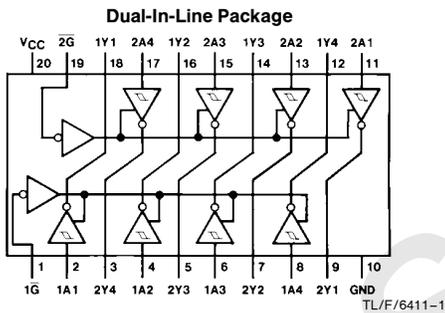
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

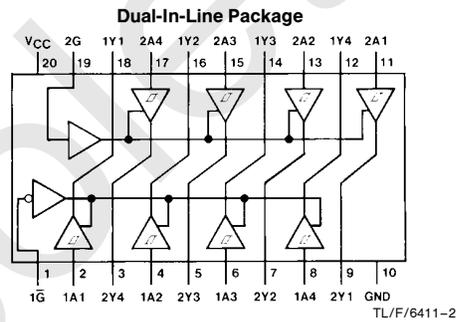
- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins

- Typical I_{OL} (sink current)
 - 54LS 12 mA
 - 74LS 24 mA
- Typical I_{OH} (source current)
 - 54LS -12 mA
 - 74LS -15 mA
- Typical propagation delay times
 - Inverting 10.5 ns
 - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
 - Inverting 130 mW
 - Noninverting 135 mW

Connection Diagrams



Order Number DM54LS240J,
DM54LS240W, DM54LS240E,
DM74LS240WM or DM74LS240N
See NS Package Number E20A, J20A,
M20B, N20A or W20A



Order Number DM54LS241J,
DM54LS241W, DM54LS241E,
DM74LS241WM or DM74LS241N
See NS Package Number E20A, J20A,
M20B, N20A or W20A

Function Tables

LS240

Inputs		Output
\bar{G}	A	Y
L	L	H
L	H	L
H	X	Z

LS241

Inputs				Outputs	
G	\bar{G}	1A	2A	1Y	2Y
X	L	L	X	L	
X	L	H	X	H	
X	H	X	X	Z	
H	X	X	L		L
H	X	X	H		H
L	X	X	X		Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS, 54LS	–55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54LS240, 241			DM74LS240, 241			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			–12			–15	mA
I _{OL}	Low Level Output Current			12			24	mA
T _A	Free Air Operating Temperature	–55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units		
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = –18 mA			–1.5	V		
HYS	Hysteresis (V _{T+} – V _{T–}) Data Inputs Only	V _{CC} = Min	0.2	0.4		V		
V _{OH}	High Level Output Voltage	V _{CC} = Min, V _{IH} = Min V _{IL} = Max, I _{OH} = –1 mA	DM74	2.7		V		
		V _{CC} = Min, V _{IH} = Min V _{IL} = Max, I _{OH} = –3 mA	DM54/DM74	2.4	3.4			
		V _{CC} = Min, V _{IH} = Min V _{IL} = 0.5V, I _{OH} = Max	DM54/DM74	2				
V _{OL}	Low Level Output Voltage	V _{CC} = Min V _{IL} = Max V _{IH} = Min	I _{OL} = 12 mA I _{OL} = Max	DM74 DM54 DM74		0.4 0.4 0.5	V	
		V _{CC} = Max V _{IL} = Max V _{IH} = Min	V _O = 2.7V			20		μA
		V _{CC} = Max V _{IL} = Max V _{IH} = Min	V _O = 0.4V			–20		μA
I _I	Input Current at Maximum Input Voltage	V _{CC} = Max, V _I = 7V (DM74) V _I = 10V (DM54)			0.1	mA		
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.7V			20	μA		
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			–0.2	mA		
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	–40		–225	mA		
I _{CC}	Supply Current	V _{CC} = Max, Outputs Open	Outputs High	LS240, LS241	13	23	mA	
			Outputs Low	LS240	26	44		
				LS241	27	46		
			Outputs Disabled	LS240	29	50		
				LS241	32	54		

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

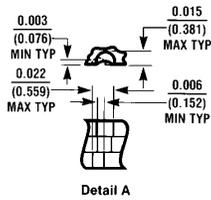
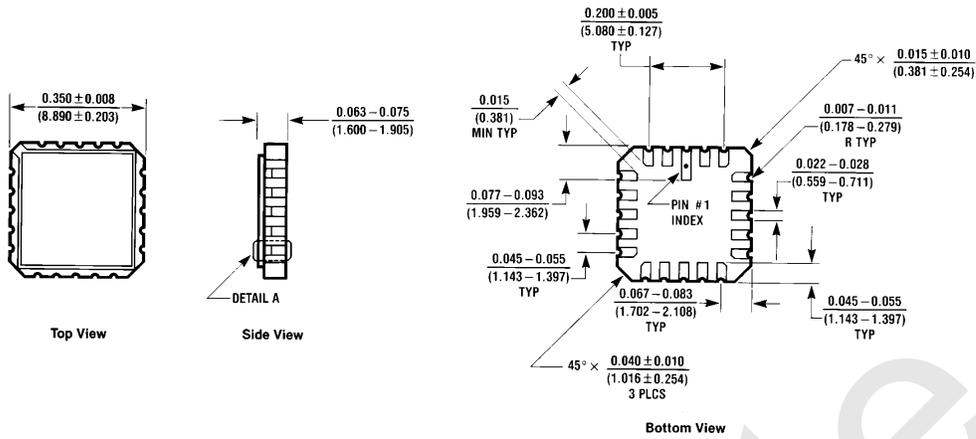
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$

Symbol	Parameter	Conditions		DM54LS	DM74LS	Units
				Max	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 45 \text{ pF}$ $R_L = 667\Omega$	LS240	18	14	ns
			LS241	18	18	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 45 \text{ pF}$ $R_L = 667\Omega$	LS240	18	18	ns
			LS241	18	18	
t_{PZL}	Output Enable Time to Low Level	$C_L = 45 \text{ pF}$ $R_L = 667\Omega$	LS240	30	30	ns
			LS241	30	30	
t_{PZH}	Output Enable Time to High Level	$C_L = 45 \text{ pF}$ $R_L = 667\Omega$	LS240	23	23	ns
			LS241	23	23	
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5 \text{ pF}$ $R_L = 667\Omega$	LS240	25	25	ns
			LS241	25	25	
t_{PHZ}	Output Disable Time from High Level	$C_L = 5 \text{ pF}$ $R_L = 667\Omega$	LS240	18	18	ns
			LS241	18	18	
t_{PLH}	Propagation Delay Time Low to High Level Output	$C_L = 150 \text{ pF}$ $R_L = 667\Omega$	LS240		18	ns
			LS241		21	
t_{PHL}	Propagation Delay Time High to Low Level Output	$C_L = 150 \text{ pF}$ $R_L = 667\Omega$	LS240		22	ns
			LS241		22	
t_{PZL}	Output Enable Time to Low Level	$C_L = 150 \text{ pF}$ $R_L = 667\Omega$	LS240		33	ns
			LS241		33	
t_{PZH}	Output Enable Time to High Level	$C_L = 150 \text{ pF}$ $R_L = 667\Omega$	LS240		26	ns
			LS241		26	

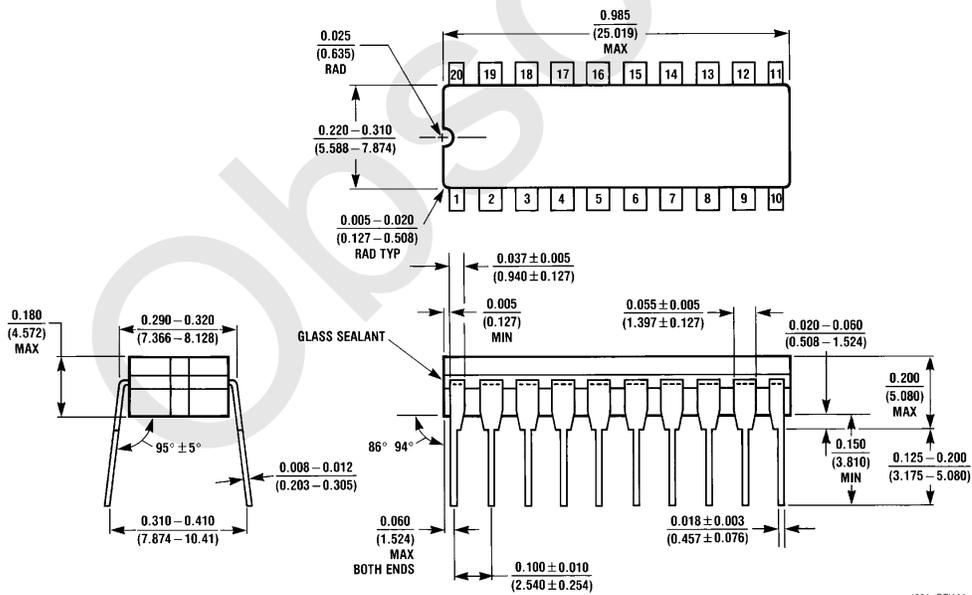
Note: 54LS Output load is $C_L = 50 \text{ pF}$ for t_{PLH} , t_{PHL} , t_{PZL} and t_{PZH} .

Physical Dimensions inches (millimeters)



Ceramic Leadless Chip Carrier Package (E)
 Order Number DM54LS240E or DM54LS241E
 NS Package Number E20A

E20A (REV D)

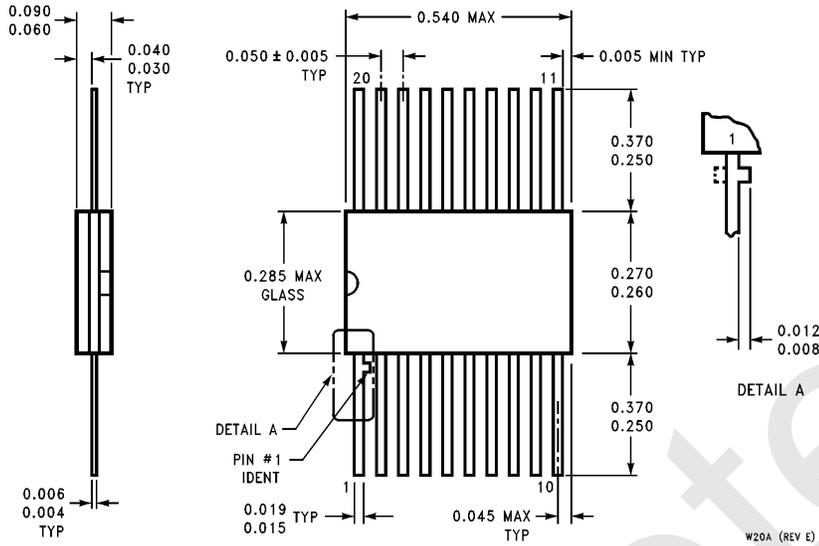


20-Lead Ceramic Dual-In-Line Package (J)
 Order Number DM54LS240J or DM54LS241J
 NS Package Number J20A

J20A (REV M)

**DM54LS240/DM74LS240, DM54LS241/DM74LS241
Octal TRI-STATE Buffers/Line Drivers/Line Receivers**

Physical Dimensions inches (millimeters) (Continued)



20-Lead Ceramic Flat Package (W)
Order Number DM54LS240W or DM54LS241W
NS Package Number W20A

W20A (REV E)

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National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: onjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 19th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

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