



54LS322/DM74LS322

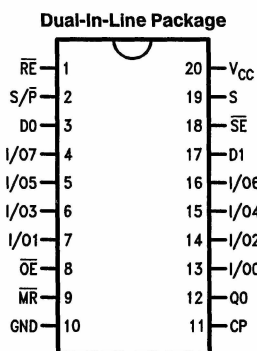
8-Bit Serial/Parallel Register with Sign Extend

General Description

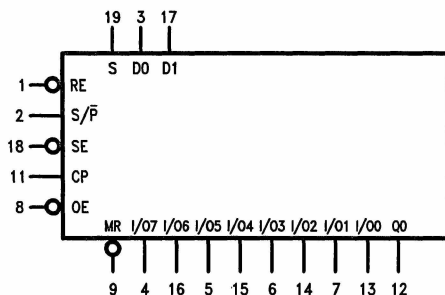
The 'LS322 is an 8-bit shift register with provision for either serial or parallel loading and with TRI-STATE® parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store),

shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register. The '322 is specifically designed for operation with the '384 Multiplier and provides the sign extend function required for the '384.

Connection Diagram



Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

TL/F/9828-2

TL/F/9828-1

Order Number 54LS322DMQB, 54LS322FMQB,
DM74LS322WM or DM74LS322N
See NS Package Number J20A, M20B, N20A or W20A

Pin Names	Description
$\overline{RE}$	Register Enable Input (Active LOW)
$S/\overline{P}$	Serial (HIGH) or Parallel (LOW) Mode Control Input
$\overline{SE}$	Sign Extend Input (Active LOW)
S	Serial Data Select Input
D0, D1	Serial Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
Q0	Bi-State Serial Output
I/O0-I/O7	Multiplexed Parallel Inputs or TRI-STATE Parallel Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	54LS322			DM74LS322			Units
		Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			2			V
V _{IL}	Low Level Input Voltage			0.7			0.8	V
I _{OH}	High Level Output Current			−0.4			−0.4	mA
I _{OL}	Low Level Output Current			4			8	mA
T _A	Free Air Operating Temperature	−55		125	0		70	°C
t _s (H) t _s (L)	Setup Time HIGH or LOW RE to CP	24 24			24 24			ns
t _h (H) t _h (L)	Hold Time HIGH or LOW RE to CP	5 5			0 0			ns
t _s (H) t _s (L)	Setup Time HIGH or LOW D0, D1 or I/O _n to CP	15 15			10 10			ns
t _h (H) t _h (L)	Hold Time HIGH or LOW D0, D1 or I/O _n to CP	5 5			0 0			ns
t _s (H) t _s (L)	Setup Time HIGH or LOW SE to CP	15 15			15 15			ns
t _h (H) t _h (L)	Hold Time HIGH or LOW SE to CP	0 0			0 0			ns
t _s (H) t _s (L)	Setup Time HIGH or LOW SP to CP	24 24			24 24			ns
t _s (H) t _s (L)	Setup Time HIGH or LOW S to CP	15 15			15 15			ns
t _h (H) t _h (L)	Hold Time HIGH or LOW S or SP to CP	0 0			0 0			ns
t _w (H)	CP Pulse Width HIGH	15			15			ns
t _w (L)	MR Pulse Width LOW	15			15			ns
t _{rec}	Recovery Time MR to CP	15			15			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$	54LS 2.5 DM74 2.7	3.4		V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IH} = \text{Min}$	54LS DM74	0.35	0.4 0.5	V
		$I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$	DM74	0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 10 \text{ V}$			0.1	mA
		S Input			0.2	
		SE Input			0.3	
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7 \text{ V}$			20	μA
		S Input			40	
		SE Input			60	
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4 \text{ V}$			-0.4	mA
		$V_{CC} = \text{Max}, V_I = 0.4 \text{ V}$ S Input			-0.8	
		$V_{CC} = \text{Max}, V_I = 0.4 \text{ V}$ SE Input			-1.2	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	54LS I/On Qn DM74	-30 -20 -20	-130 -100 -100	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$			60	mA
I_{OZH}	TRI-STATE Output Off Current HIGH	$V_{CC} = V_{CCH}$ $V_{OZH} = 2.7 \text{ V}$			40	μA
I_{OZL}	TRI-STATE Output Off Current LOW	$V_{CC} = V_{CCH}$ $V_{OZL} = 0.4 \text{ V}$			-0.4	mA

Note 1: All typicals are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0 \text{ V}, T_A = +25^\circ\text{C}$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$R_L = 2\text{ k}\Omega, C_L = 15\text{ pF}$				Units
		54LS		DM74LS		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	35		35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to I/O _n **	25 35		25 34		ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q0	26 28		26 29		ns
t_{PHL}	Propagation Delay MR to I/O _n **	35		34.1		ns
t_{PHL}	Propagation Delay MR to Q0	28		28		ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{\text{OE}}$ to I/O _n **	18 25		21.5 23.9		ns

** $C_L = 50 \text{ pF}$

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25^\circ C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C _L = 15 pF				Units
		54LS		DM74LS		
		Min	Max	Min	Max	
t _{PHZ} t _{PLZ}	Output Disable Time OE to I/O _n *		15 20		15 15	ns
t _{PZH} t _{PZL}	Output Enable Time S/P to I/O _n **		22 30		25.2 25.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time SP to I/O _n *		23 23		40.2 26.8	ns

* $C_L = 5\text{ pF}$

** $C_L = 50\text{ pF}$

Functional Description

The LS322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on $S/\overline{P}$ enables shift right, while a LOW signal disables the TRI-STATE output buffers and enables parallel loading. In the shift right mode a HIGH signal

on $\overline{SE}$ enables serial entry from either D0 or D1, as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q7 reloads its contents, thus performing the sign extend function required for the '384 Twos Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the TRI-STATE output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

Mode Table

Mode	Inputs							Outputs								Q0
	$\overline{MR}$	$\overline{RE}$	$S/\overline{P}$	$\overline{SE}$	S	$\overline{OE}^*$	CP	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	
Clear	L L	X X	X X	X X	X X	L H	X X	L Z	L Z	L Z	L Z	L Z	L Z	L Z	L Z	L L
Parallel Load	H	L	L	X	X	X		I7	I6	I5	I4	I3	I2	I1	I0	I0
Shift Right	H H	L L	H H	H H	L H	L L	 	D0 D1	O7 O7	O6 O6	O5 O5	O4 O4	O3 O3	O2 O2	O1 O1	O1 O1
Sign Extend	H	L	H	L	X	L		O7	O7	O6	O5	O4	O3	O2	O1	O1
Hold	H	H	X	X	X	L		NC	NC	NC	NC	NC	NC	NC	NC	NC

*When the $\overline{OE}$ input is HIGH, all I/O_n terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

Note 1: I7–I0 = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q0) are isolated from the I/O terminal.

Note 2: D0, D1 = The level of the steady-state inputs to the serial multiplexer input.

Note 3: O7–O0 = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

NC = No Change Z = High-Impedance Output State H = HIGH Voltage Level L = LOW Voltage Level

Logic Diagram

