

## DM54LS460A/DM74LS460A 10-Bit Comparator

### General Description

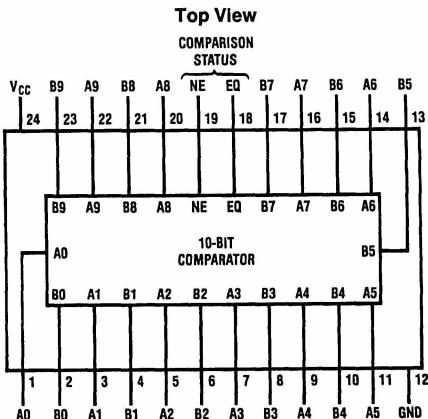
The 'LS460A is a 10-bit comparator with true complement comparison status outputs. The device compares two 10-bit data strings ( $A_g - A_0$  and  $B_g - B_0$ ) to establish if this data is Equivalent (EQ = HIGH and NE = LOW) or Not Equivalent (EQ = LOW and NE = HIGH).

Outputs conform to the usual 8 mA LS totem-pole drive standard.

### Features

- True and complement comparison status outputs
- 24-pin SKINNYDIP saves space
- Low current PNP inputs reduce loading
- Expandable in 10-bit increments
- 15 ns typical propagation delay

### Connection Diagram



TL/L/10225-1

Order Number **DM54LS460AJ**, **DM74LS460AJ**, **DM74LS460AN** or **DM74LS460AV**  
See NS Package Number **J24F**, **N24C** or **V28A**

### Function Table

<b>A9 - A0</b>	<b>B9 - B0</b>	<b>EQ</b>	<b>NE</b>	<b>Operation</b>
A	A	H	L	}
B	B	H	L	
A	B	L	H	

Equivalent (A = B)  
Not Equivalent (A ≠ B)

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	−0.5 to +7V (Note 2)
Input Voltage	−1.5 to +5.5V (Note 2)
Off-State Output Voltage	−1.5 to +5.5V (Note 2)
Input Current	−30.0 mA to +5.0 mA (Note 2)
Output Current ( $I_{OL}$ )	+100 mA
Storage Temperature	−65°C to +150°C

Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature with Power Applied	−65°C to +150°C
ESD Tolerance CZAP = 100 pF RZAP = 1500Ω	2000V
Test Method: Human Body Model	
Test Specification: NSC SOP-5-028	

**Recommended Operating Conditions**

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
$T_A$	Operating Free-Air Temperature	−55		125	0		75	°C

**Electrical Characteristics** Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
$V_{IL}$	Low Level Input Voltage (Note 3)						0.8	V
$V_{IH}$	High Level Input Voltage (Note 3)				2			V
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min}, I = -18 \text{ mA}$					−1.5	V
$I_{IL}$	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4V$					−0.25	mA
$I_{IH}$	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4V$					25	μA
$I_I$	Maximum Input Current	$V_{CC} = \text{Max}, V_I = 5.5V$					1	mA
$V_{OL}$	Low Level Output Voltage	$V_{CC} = \text{Min}$	$I_{OL} = 8 \text{ mA}$				0.5	V
$V_{OH}$	High Level Output Voltage	$V_{CC} = \text{Min}$	$I_{OH} = -2 \text{ mA}$	MIL	2.4			V
			$I_{OH} = -3.2 \text{ mA}$	COM				
$I_{OS}$	Output Short-Circuit Current (Note 4)	$V_{CC} = 5V, V_O = 0V$			−30		−130	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}, \text{Outputs Open}$				60	100	mA

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming operations according to the applicable specification.

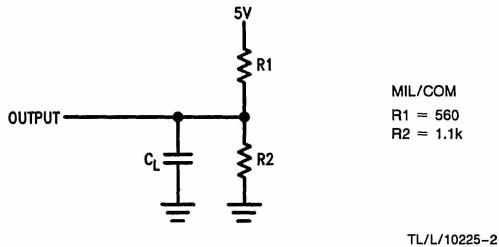
**Note 3:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

**Note 4:** To avoid invalid readings in other parameter tests, it is preferable to conduct the  $I_{OS}$  test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

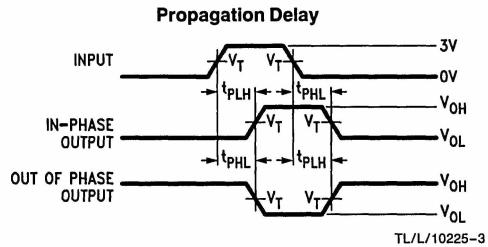
## Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
$T_{pd}$	Input to Output	$C_L = 50 \text{ pF}$			35			30	ns

## Test Load



## Test Waveform



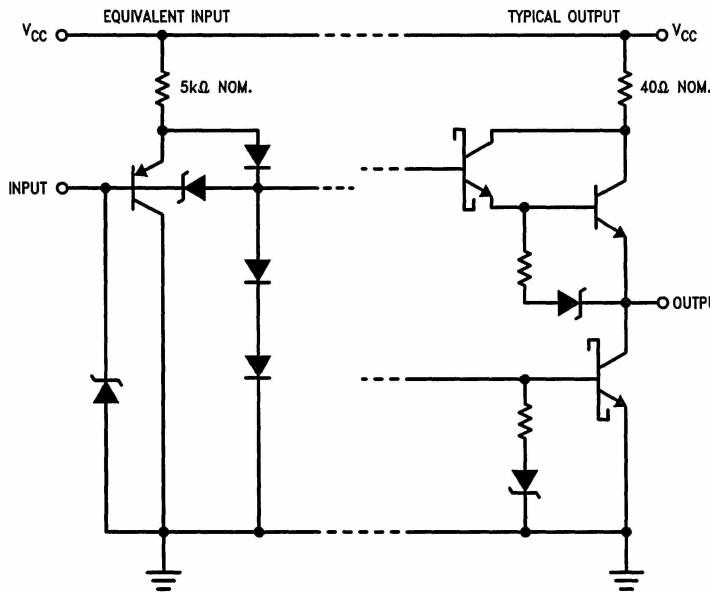
### Notes:

$V_T = 1.5V$

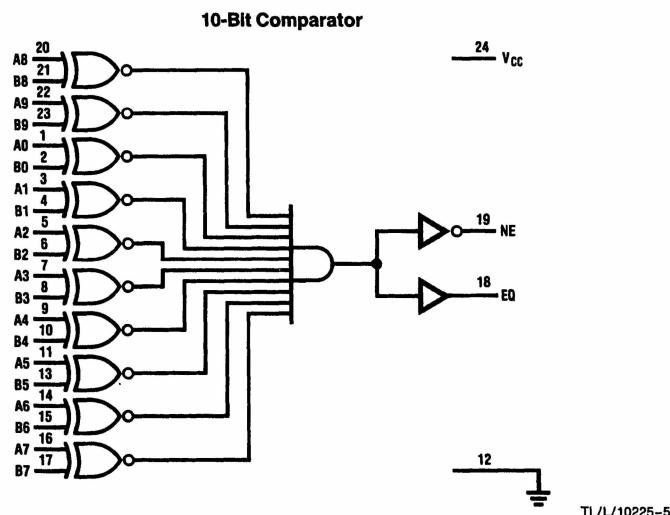
$C_L$  includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

## Schematic of Inputs and Outputs



## Logic Diagram



TL/L/10225-5